Small- and large-signal RF FET circuit models

Microwave Electronics

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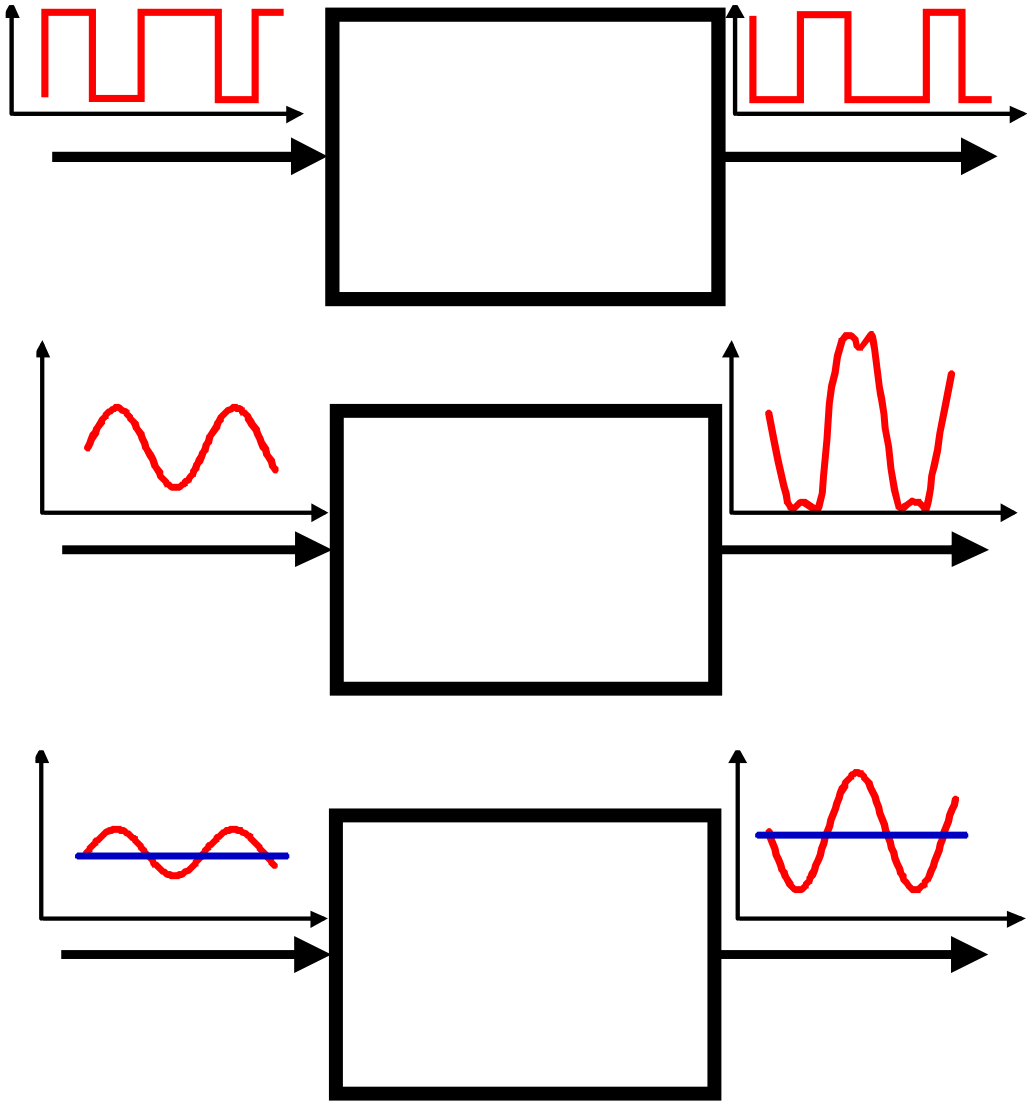
Physics-based, circuit-oriented, black-box models

- Physics-based models solve the transport and Poisson equations at a microscopic level (analytically-approximately or numerically-exactly); cons: computational intensity
- Equivalent circuit models are approximate but efficient, can be based on analytical PB models or fitted on measured data
- Black-box models are mathematical models entirely derived from measured data

Linear and nonlinear models - I

- Nonlinear ("large signal") models → all possible operations, independent on the input signal magnitude**:**
  - *digital (switching) behaviour*
  - *analog large-signal behaviour, usually periodic steady state → power amplifiers, mixers, frequency multipliers etc → models output signal and signal distortion (harmonics, intermodulation etc)*
- Small signal models → small amplitude signal around a DC steady-state
  - *analog linear applications → high-gain, low noise amplifiers*
- Both large-signal and small-signal models are *dynamic* or *with memory* → include reactive effects, important at RF and beyond
  - a large-signal model in DC however is *memoriless* and is used to evaluate the DC device working point.

Linear and nonlinear models - II



- **Switching**
- **Large-signal analog**
- **Small-signal analog**

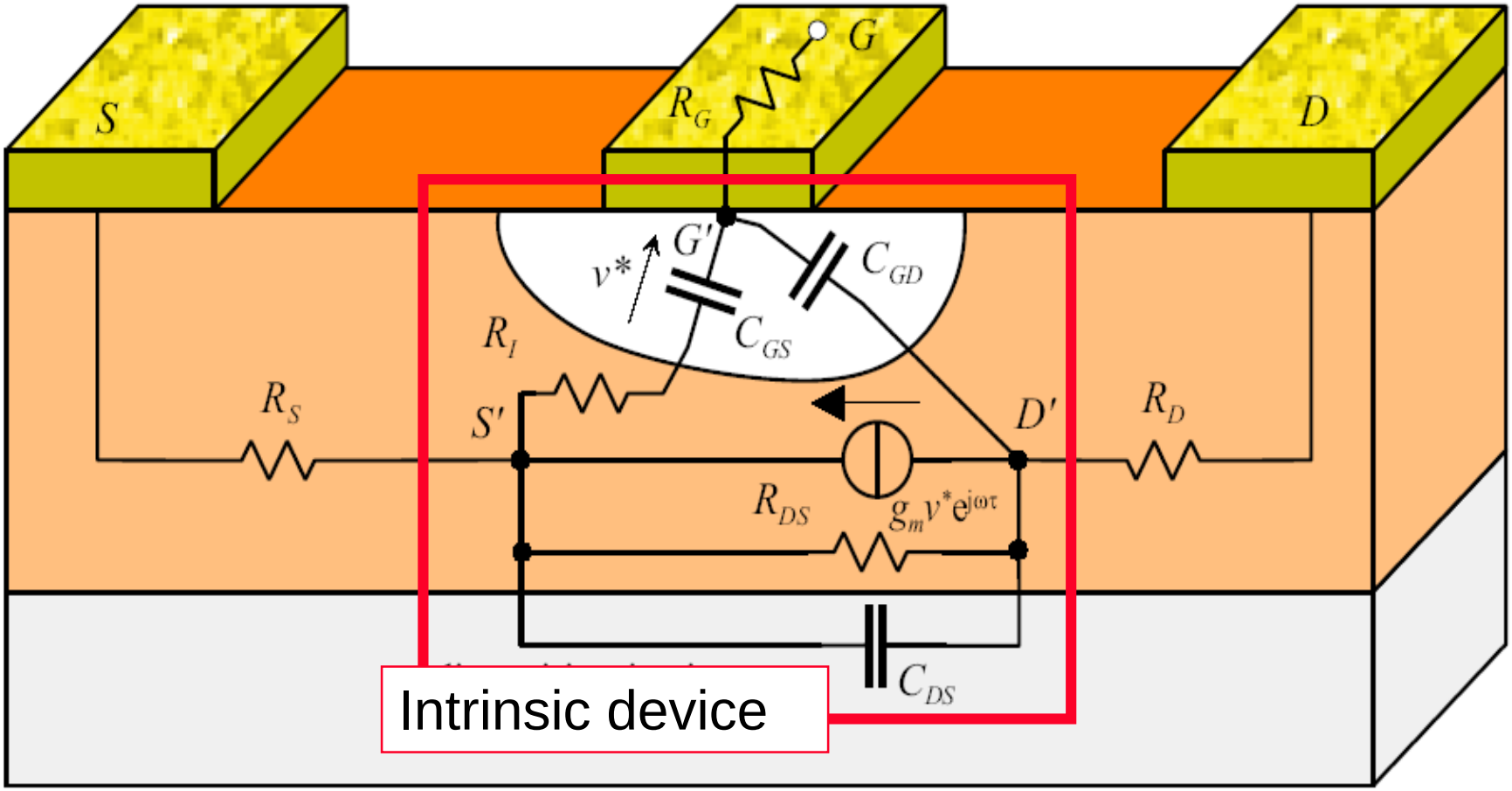
Small-signal device models

- An exact black-box small-signal model is given by the measured *scattering parameters* on the frequency band of interest
- Nevertheless, small-signal equivalent circuits are extremely popular in circuit design (even if they are approximate) because:
  - *allow for a better separation on the intrinsic device from parasitic effects*
  - *allow for an easier connection with **device physics***
  - *allow for wideband operation, even outside the measured bandwidth*
  - *allow for device periphery scaling*

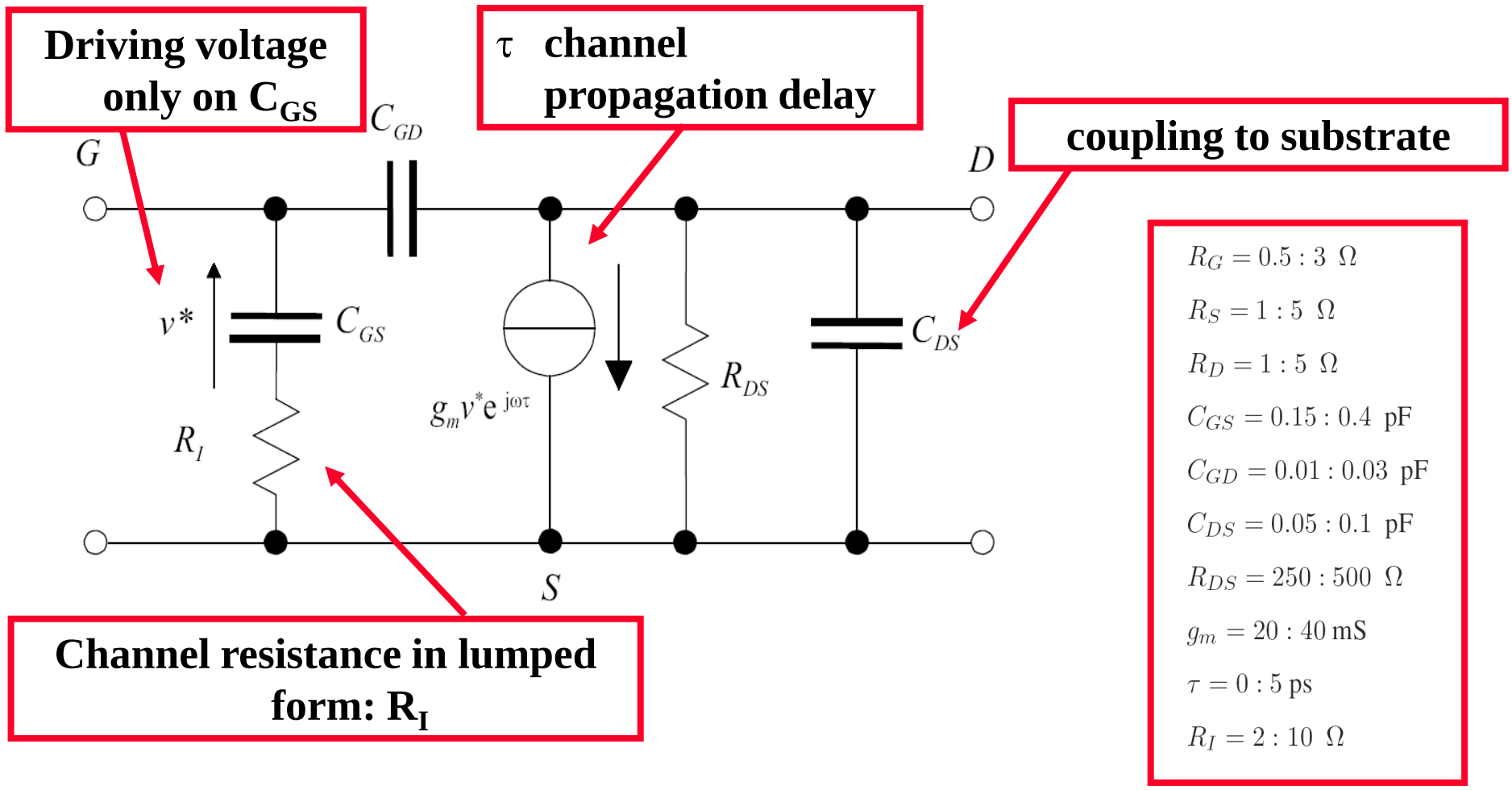
FET and bipolar equivalent circuits

- Despite the different physical structure the FET and bipolar equivalent circuits are similar in the output and parasitic part, however the input is different:
  - FETs: RC series input
  - Bipolars: RC parallel input
- We mainly focus on FETs, although during the last few years bipolars have become important in many applications
- In the CAD program we find several model specific to FET or bipolar technologies, some of those are the evolution of digital or low-frequency analog models, e.g.:
  - MEXTRAM model (bipolars), BSIM3 model (RF MOS)

Physics-based interpretation of small-signal FET circuits



Seven-parameters intrinsic equivalent circuit for FETs



$R_G = 0.5 : 3\ \Omega$

$R_S = 1 : 5\ \Omega$

$R_D = 1 : 5\ \Omega$

$C_{GS} = 0.15 : 0.4\ \text{pF}$

$C_{GD} = 0.01 : 0.03\ \text{pF}$

$C_{DS} = 0.05 : 0.1\ \text{pF}$

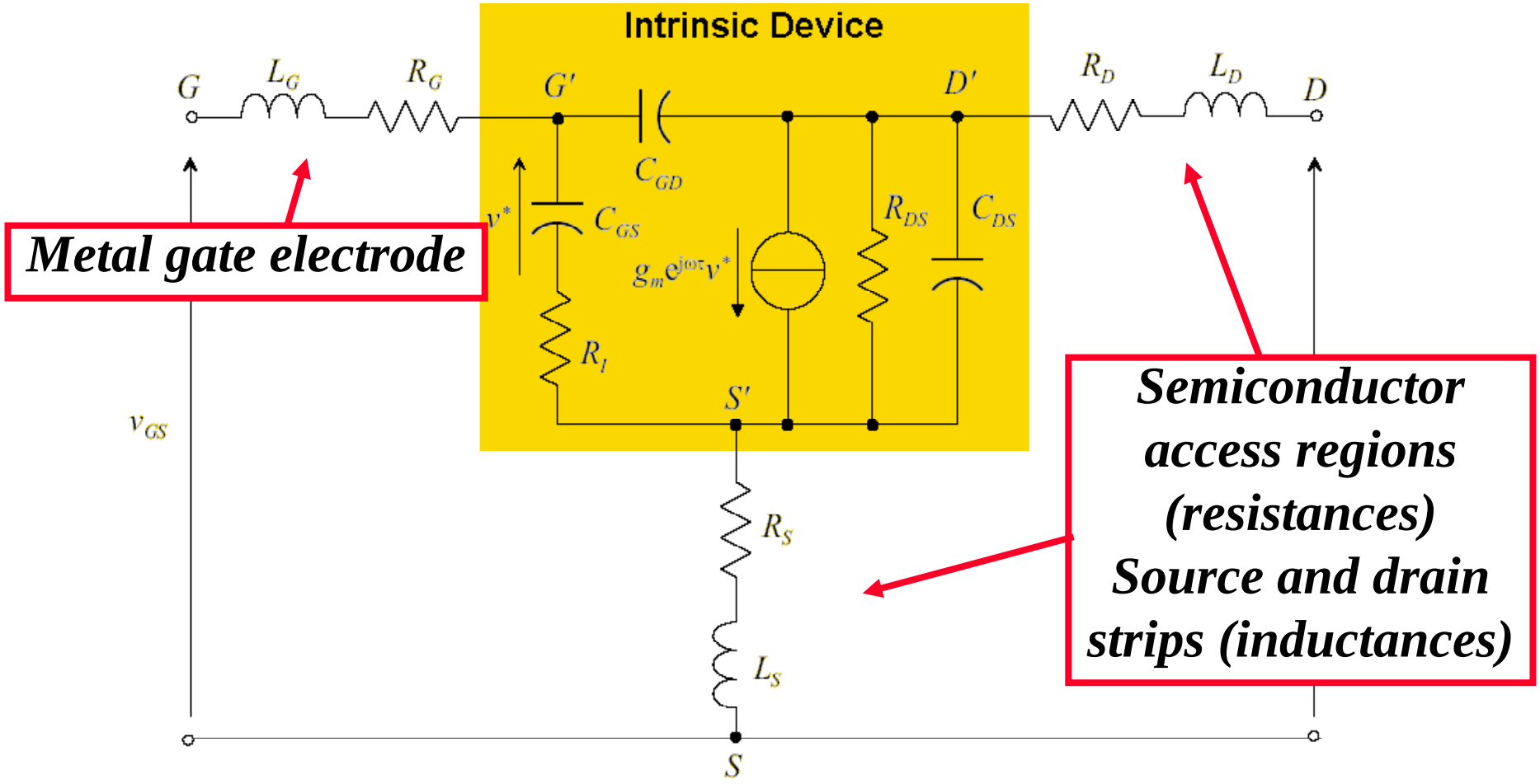
$R_{DS} = 250 : 500\ \Omega$

$g_m = 20 : 40\ \text{mS}$

$\tau = 0 : 5\ \text{ps}$

$R_I = 2 : 10\ \Omega$

Equivalent circuit with series parasitics



Scattering parameters of intrinsic device

We start from the intrinsic Y matrix ("by inspection"):

$$Y = \begin{pmatrix} \dfrac{\mathrm{j}\omega C_{GS}}{1+\mathrm{j}\omega C_{GS}R_I} + \mathrm{j}\omega C_{GD} & -\mathrm{j}\omega C_{GD} \\ \dfrac{g_m \mathrm{e}^{\mathrm{j}\omega\tau}}{1+\mathrm{j}\omega C_{GS}R_I} - \mathrm{j}\omega C_{GD} & \mathrm{j}\omega(C_{GD}+C_{DS}) + \dfrac{1}{R_{DS}} \end{pmatrix}$$

$y_{i,j} = R_0 Y_{i,j}$

$$S_{11} = \frac{y_{12}y_{21} - y_{11}y_{22} - y_{11} + y_{22} + 1}{y_{11}y_{22} + y_{11} + y_{22} + 1 - y_{12}y_{21}}$$

$$S_{12} = \frac{-2y_{12}}{y_{11}y_{22} + y_{11} + y_{22} + 1 - y_{12}y_{21}}$$

$$S_{21} = \frac{-2y_{21}}{y_{11}y_{22} + y_{11} + y_{22} + 1 - y_{12}y_{21}}$$

$$S_{22} = \frac{y_{12}y_{21} - y_{11}y_{22} - y_{22} + y_{11} + 1}{y_{11}y_{22} + y_{11} + y_{22} + 1 - y_{12}y_{21}}$$

General expressions, we discuss the unilateral case!

S-parameters of unilateral device

$$
\begin{cases}
S_{11}^U = -\dfrac{y_{11}^U - 1}{y_{11}^U + 1} = \dfrac{1 + \mathrm{j}\omega C_{GS}(R_I - R_0)}{1 + \mathrm{j}\omega C_{GS}(R_0 + R_I)} \\
S_{12}^U = 0 \\
S_{21}^U = -\dfrac{2y_{21}^U}{\left(y_{11}^U + 1\right)\left(y_{22}^U + 1\right)} = -\dfrac{2\dfrac{R_0 R_{DS}}{R_0 + R_{DS}} g_m \mathrm{e}^{\mathrm{j}\omega\tau}}{\left(1 + \mathrm{j}\omega C_{DS}\dfrac{R_0 R_{DS}}{R_0 + R_{DS}}\right)\left(1 + \mathrm{j}\omega C_{GS}(R_0 + R_I)\right)} \\
S_{22}^U = -\dfrac{y_{22}^U - 1}{y_{22}^U + 1} = -\dfrac{\dfrac{R_0 - R_{DS}}{R_0 + R_{DS}} + \mathrm{j}\omega C_{DS}\dfrac{R_0 R_{DS}}{R_0 + R_{DS}}}{1 + \mathrm{j}\omega C_{DS}\dfrac{R_0 R_{DS}}{R_0 + R_{DS}}}
\end{cases}
$$

Dominant cutoff frequency

$$
f_{T1} = \frac{1}{2\pi C_{GS}(R_0 + R_I)}
$$

Low- and high-frequency behaviour

$$\lim_{\omega \to 0} S_{11} = 1$$

$$\lim_{\omega \to 0} S_{12} = 0$$

$$\lim_{\omega \to 0} S_{21} = -\frac{2 g_m R_0 R_{DS}}{R_{DS} + R_0}$$

$$\lim_{\omega \to 0} S_{22} = \frac{R_{DS} - R_0}{R_{DS} + R_0}$$

Low frequency

$$\lim_{\omega \to \infty} S_{11} = \frac{R_I - R_0}{R_I + R_0}$$

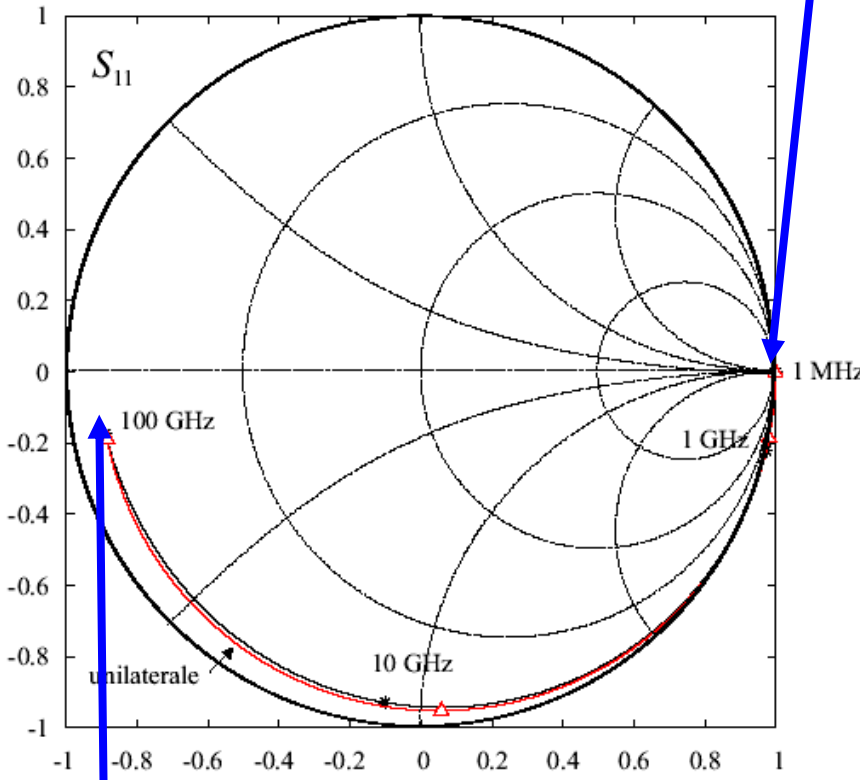
$$\lim_{\omega \to \infty} S_{12} = 0$$

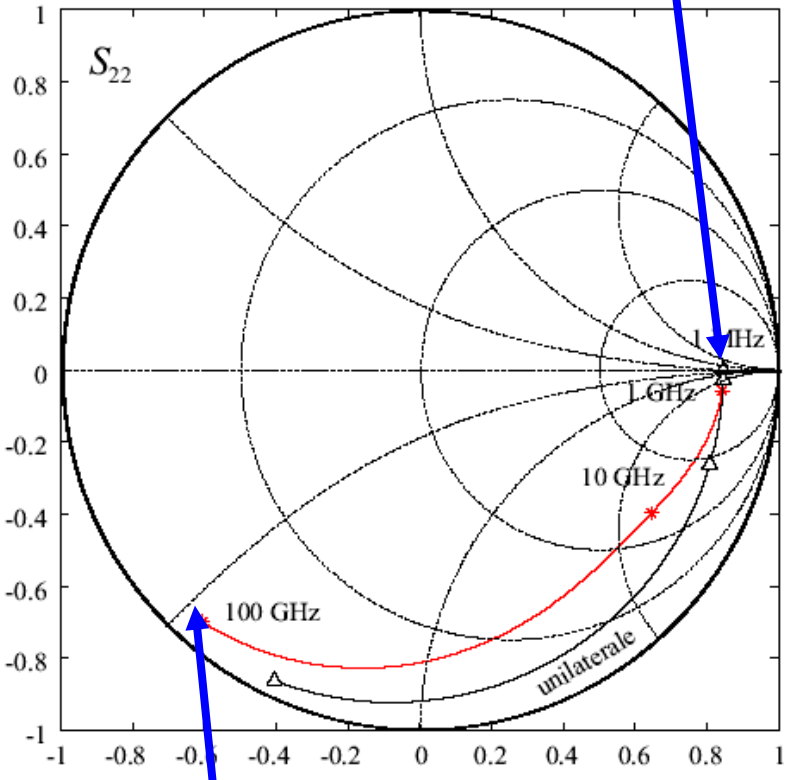
$$\lim_{\omega \to \infty} S_{21} = 0$$

$$\lim_{\omega \to \infty} S_{22} = -1$$

High frequency

Intrinsic S_{11} & S_{22}





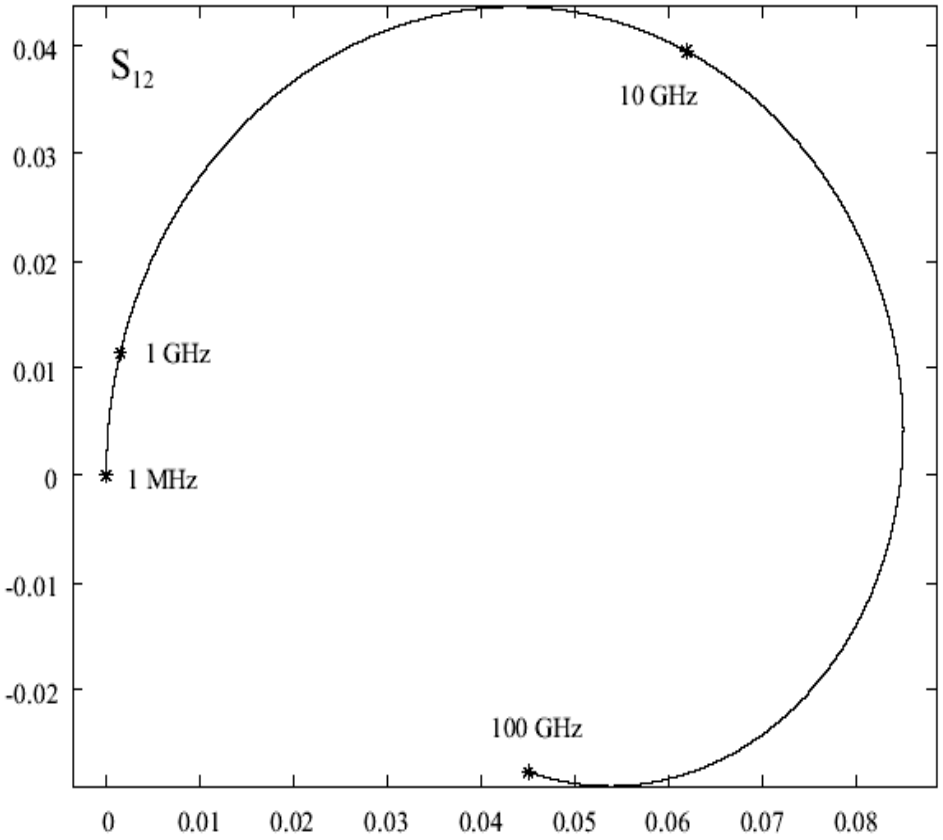
open

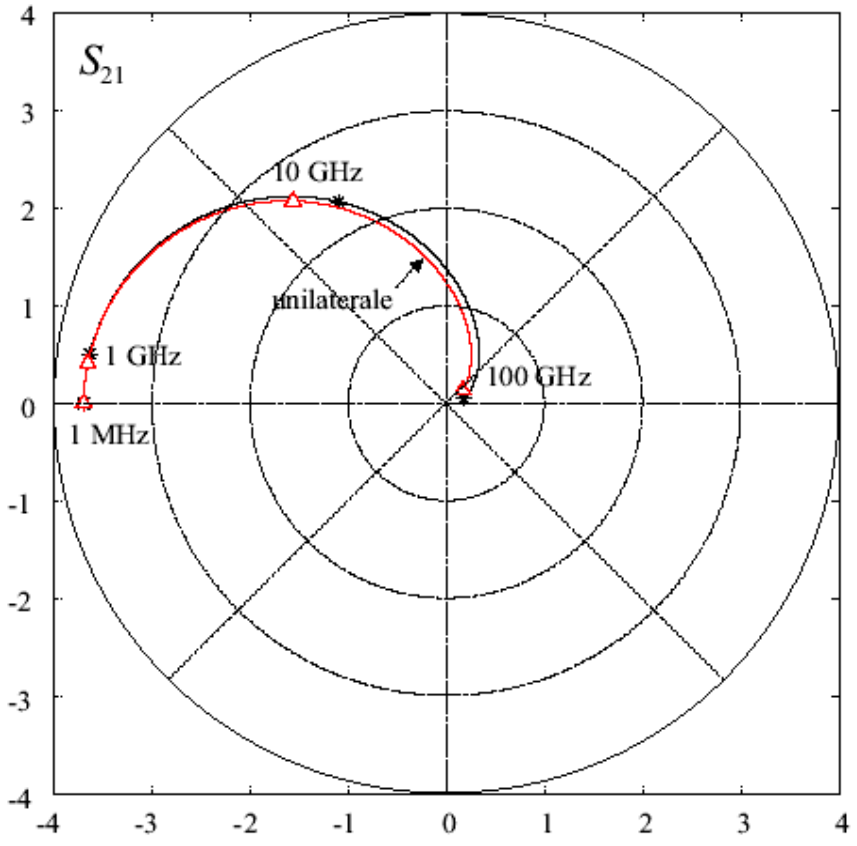
R_{ds}

towards R_I

towards short

Intrinsic S_{12} & S_{21}





- Notice that S_{11} & S_{22} → reflection coefficients (Smith chart); S_{12} & S_{21} → transmission coefficients (polar diagram)

FET figures of merit

- Several device figures of merit can be defined, related to gain, noise, operating frequency (speed)
- Very important:

cutoff frequency f_T

the short-circuit current gain is 1

maximum oscillation frequency f_{max}

the MAG is 1

- In practice: beyond f_{max} the device cannot operate, according to the application the suggested maximum operating frequency can be *lower* or *much lower* than f_T

Intrinsic FET f_T

- The short circuit current gain is $h_{21}=Y_{21}/Y_{11}$, i.e.:

$$h_{21} = \frac{g_m e^{j\omega\tau} - j\omega C_{GD}(1 + j\omega C_{GS} R_I)}{j\omega C_{GS} + j\omega C_{GD}(1 + j\omega C_{GS} R_I)} \approx \frac{g_m e^{j\omega\tau}}{j\omega(C_{GS} + C_{GD})} \approx \frac{g_m e^{j\omega\tau}}{j\omega C_{GS}}$$

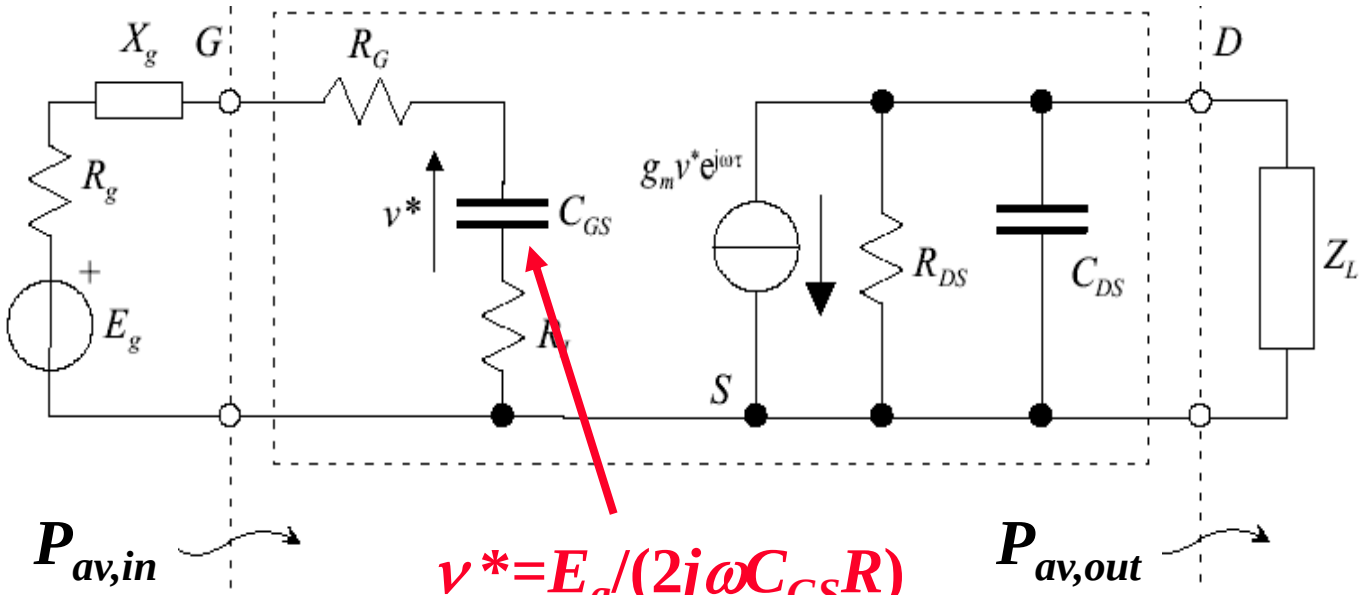
- $|h_{21}| = 1$ for:

$$f_T = \frac{g_m}{2\pi(C_{GS} + C_{GD})} \approx \frac{g_m}{2\pi C_{GS}}$$

- f_T does not depend on the gate periphery, but mainly on the gate length → grows with device scaling down
- It can be shown that, approximately:

$$f_T \approx \frac{v_{sat}}{2\pi L_g}$$

Unilateral FET (MAG→MUG) f_{max}



Power match

$R_g = R_G + R_I = R$

$jX_g = -1/j\omega C_{GS}$

$v^* = E_g/(2j\omega C_{GS}R)$

$P_{av,in} = |E_g|^2/(4R)$

$P_{av,out} = |g_m v^*|^2 R_{DS}/4$

$$\mathrm{MUG} = \frac{P_{av,out}}{P_{av,in}} = \frac{g_m^2 R_{DS}}{4\omega^2 C_{GS}^2 R}$$

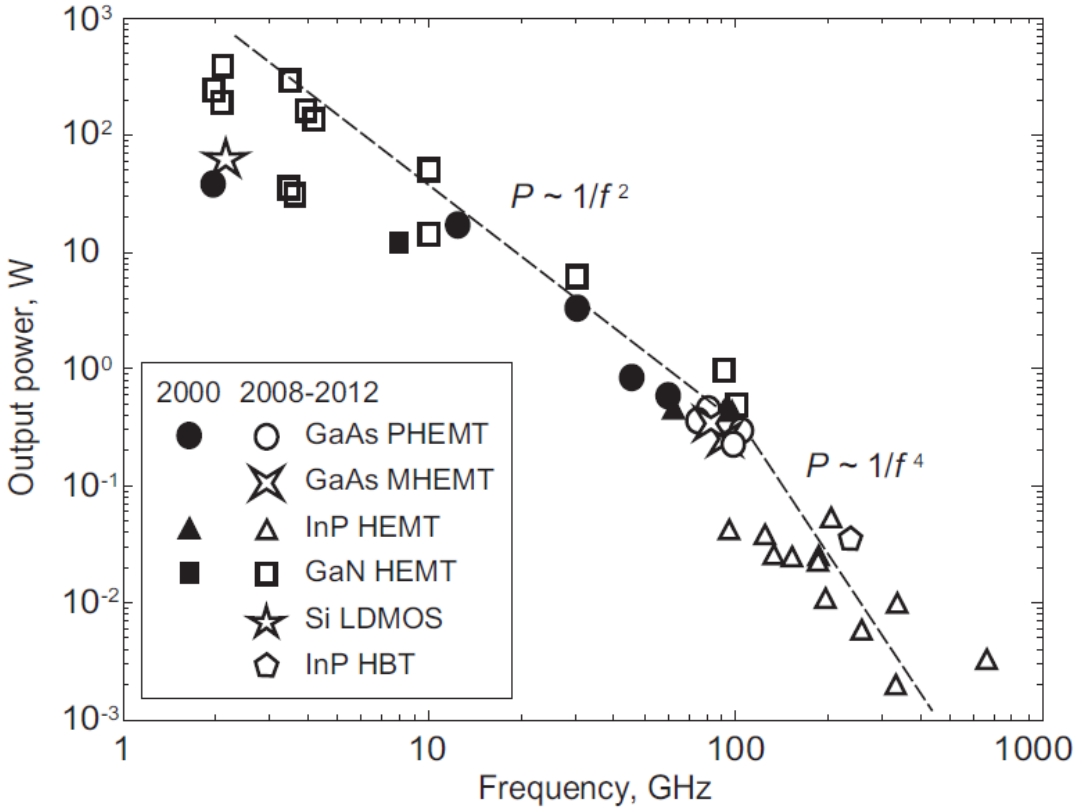
$$f_{max} = \frac{g_m}{2\pi C_{GS}} \times \frac{1}{2}\sqrt{\frac{R_{DS}}{R_I + R_G}} = \frac{f_T}{2}\sqrt{\frac{R_{DS}}{R_I + R_G}}$$

MUG=1

Still on f_{max}

- $f_{max} > f_T$ (why?)
- MUG (~MAG) frequency behaviour:

$$\mathrm{MUG} = \left(\frac{f_{max}}{f} \right)^2$$



The ability to generate RF power typically decreases as the square of frequency!

Extracting the intrinsic circuit from mesurements

- The FET intrinsic circuit has *seven* parameters, these can be exactly computed (as a function of frequency!) from the intrinsic *Y* parameters (*eight* real numbers at each *f*); typically they are **almost constant with *f***
- The instrinsic *Y* parameters can be derived from scattering parameter measurements of the whole device through *parasitic deembedding*
- Parasitic resistances and inductances can be directly measured (in small signal) on the device in which the drain-to-source bias is set to zero and the gate is in (slight) direct bias (→"cold FET measurement")
- **Numerical optimization** can be used (with care!) to maximize the agreement between "measured" and "modeled" S parameters

The deembedding procedure

S_{11} S_{12}
S_{21} S_{22}

Z_{11} Z_{12}
Z_{21} Z_{22}

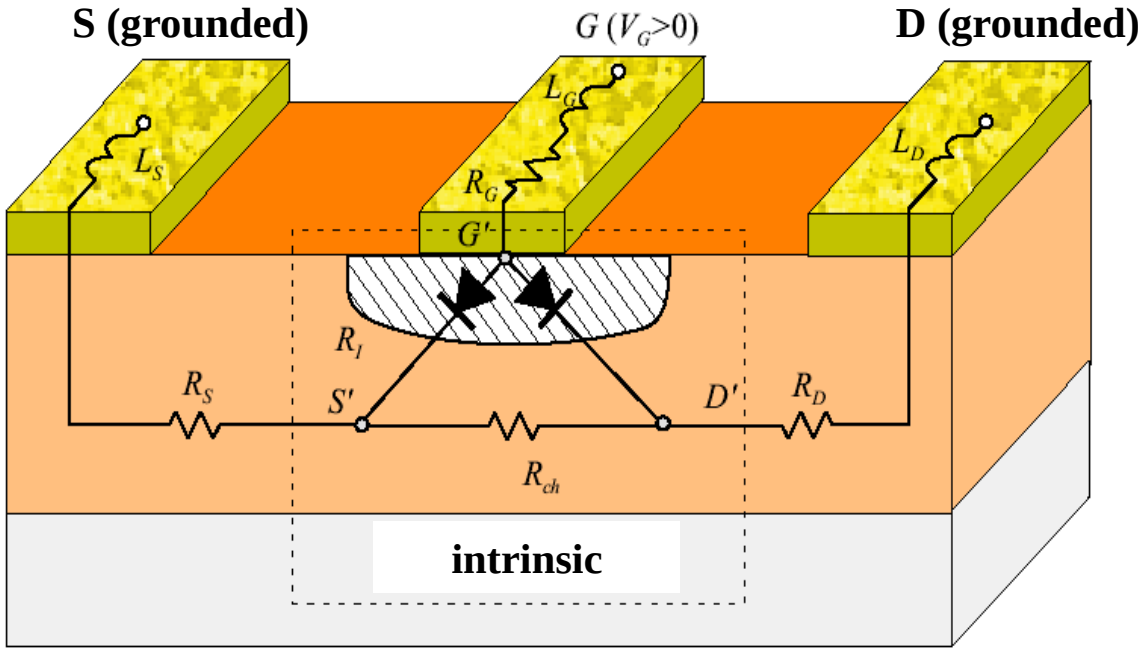
$$Z_{11,int} = Z_{11} - (R_G+R_S) - j\omega(L_G+L_S)$$
$$Z_{12,int} = Z_{12} - R_S - j\omega L_S$$
$$Z_{21,int} = Z_{21} - R_S - j\omega L_S$$
$$Z_{22,int} = Z_{22} - (R_D+R_S) - j\omega(L_D+L_S)$$

$Y_{11,int}$ $Y_{12,int}$
$Y_{21,int}$ $Y_{22,int}$

C_{GS} C_{GS} C_{DS} R_I R_{DS}
g_m τ

Cold FET measurements

- Cold FET → FET with no drain bias, no drain-to-source current flow
- The gate is in direct bias → almost a short
- Also the channel resistance is shorted, the parasitic network is a T network with 6 parameters, can be extracted from Z parameters vs. frequency



Deembedding formulae

$$C_{GD} = -\mathrm{Im}\left[Y_{12,int}\right]/\omega$$

$$C_{DS} = \mathrm{Im}\left[Y_{22,int}\right]/\omega - C_{GD}$$

$$C_{GS} = -\left\{\mathrm{Im}\left[\frac{1}{Y_{11,int} - \mathrm{j}\omega C_{GD}}\right]\omega\right\}^{-1} \approx \mathrm{Im}\left[Y_{11,int}\right]/\omega - C_{GD}$$

$$1/R_{DS} = \mathrm{Re}\left[Y_{22,int}\right]$$

$$R_I = \mathrm{Re}\left[\frac{1}{Y_{11,int} - \mathrm{j}\omega C_{GD}}\right]$$

$$g_m = \left|(Y_{21,int} + \mathrm{j}\omega C_{GD})(1 + \mathrm{j}\omega C_{GS} R_I)\right|$$

$$\tau = \arg[(Y_{21,int} + \mathrm{j}\omega C_{GD})(1 + \mathrm{j}\omega C_{GS} R_I)]/\omega$$

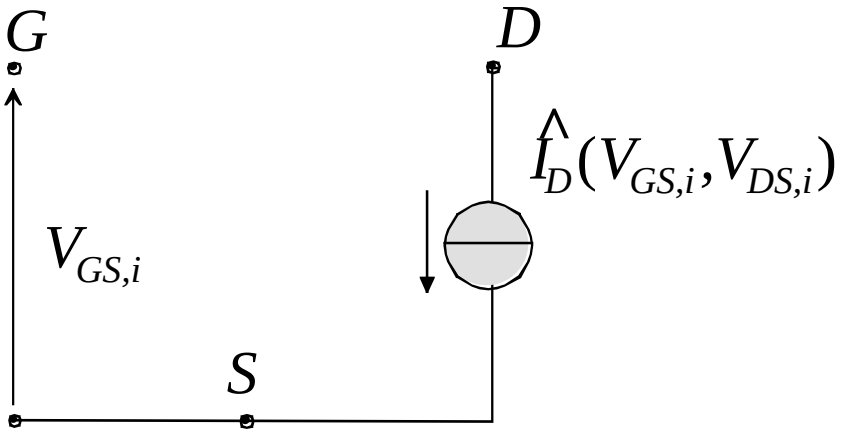
Numerical optimization

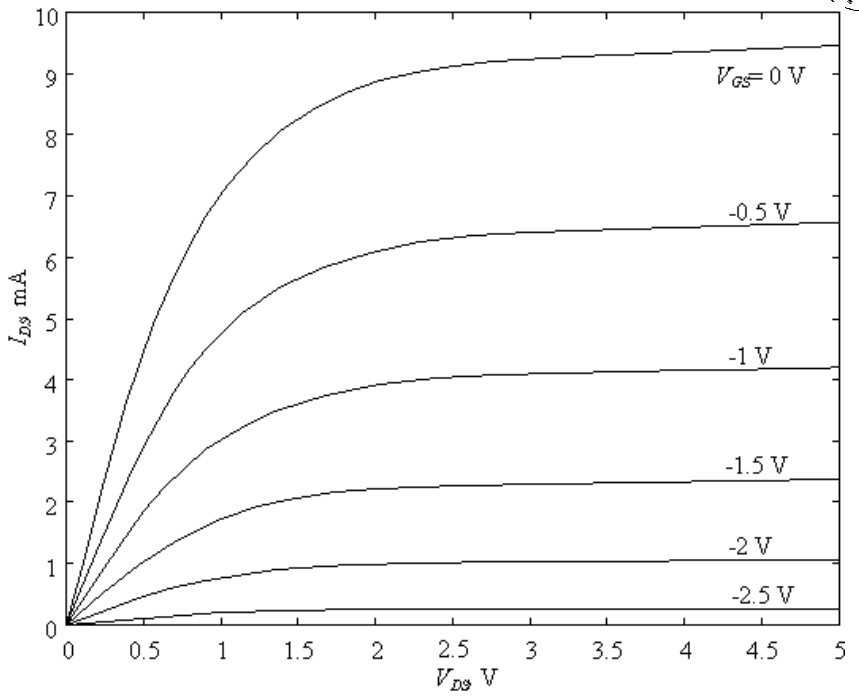
- The direct extraction of the parasitics and of the elements of the equivalent circuit can be sometimes not enough to provide accurate results as a function of frequency
- Numerical optimization often exploited to refine the model parameters
- The situation is more complex for packaged devices for which additional package parasitics are present → need to separately characterize the package
- Off the shelf models available by several foundries.

From small to large-signal equivalent circuits

- Some of the parameters of the SS equivalent circuit strongly depend on bias point → g_m, C_{GS}, C_{GD}
- According to a quasi-static approximation we can assume that P =P(V_{GS},V_{DS}) → P(t) =P(v_{GS}(t),v_{DS}(t)) where P is a circuit parameter
- In practice the large-signal model is partly derived from elements of the SS circuit, partly directly fitted on DC and SS measurements
- Some elements have to be added anew to allow for breakdown and direct gate conduction (conditions outside SS operation which however limit the maximum voltage swing on the device input and output)

Just for a start: the intrinsic large-signal equivalent circuit in DC





- In DC the device is a nonlinear voltage-driven current source yielding the DC curves but also (hopefully) consistent with the transconductance and drain resistance in small-signal
- This can be a first step towards the nonlinear circuit!

$$I_D = \hat{I}_D(V_{GS,i}, V_{DS,i})$$

$$g_m = \frac{\partial \hat{I}_D}{\partial v_{GS,i}} \qquad R_{DS}^{-1} = \frac{\partial \hat{I}_D}{\partial v_{DS,i}}$$

Managing nonlinear capacitances, breakdown etc.

- A nonlinear capacitance is defined by a nonlinear charge-voltage relationship; in small-signal conditions this relationship simply defines the capacitance as a function of the DC voltage; example for input capacitance:

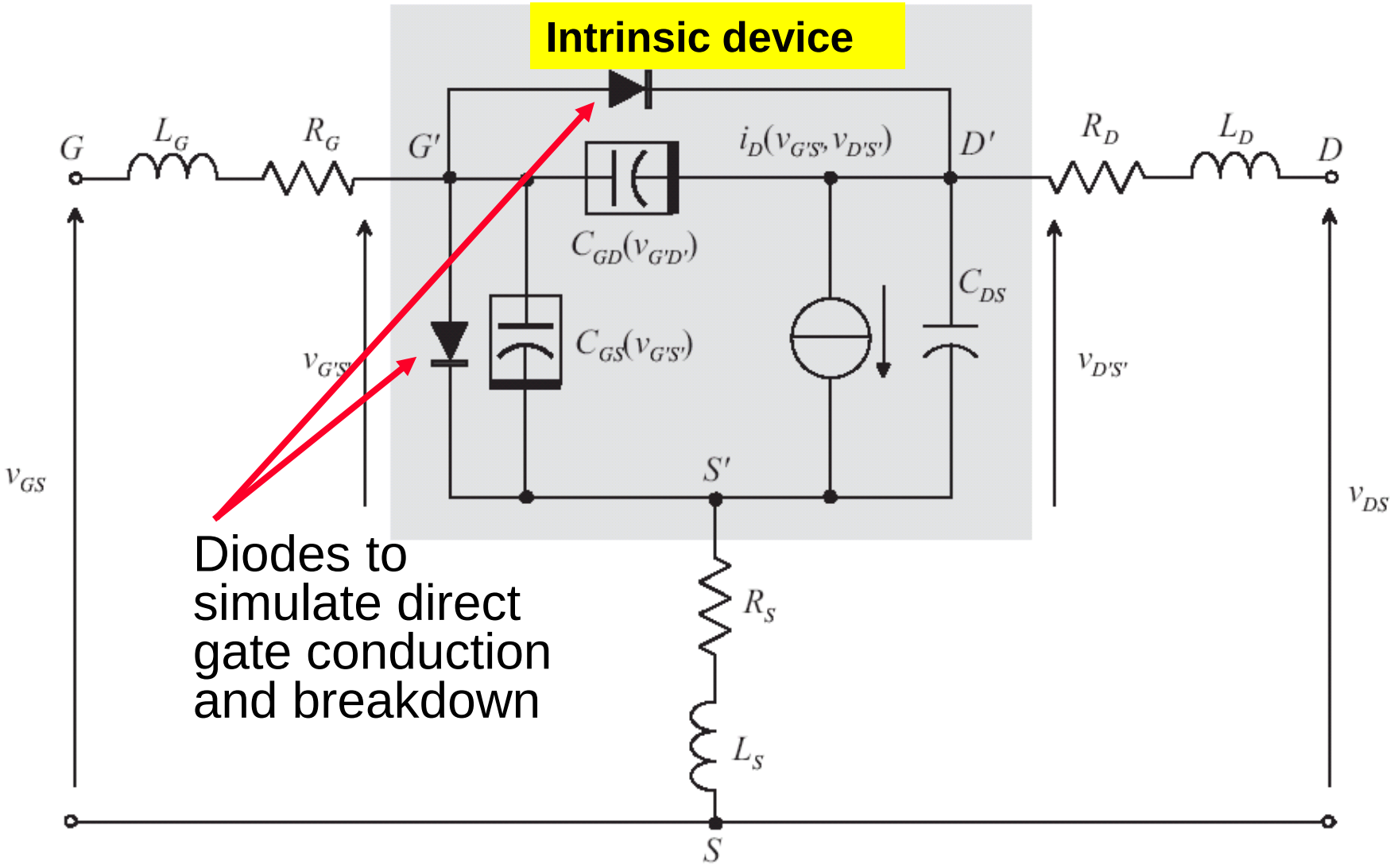
$$i_G(t) = \frac{\mathrm{d}Q_G}{\mathrm{d}t} = \frac{\mathrm{d}\hat{Q}_G}{\mathrm{d}v_{GS,i}} \frac{\mathrm{d}v_{GS,i}}{\mathrm{d}t} = C_{GS}(V_{GS,i}) \frac{\mathrm{d}v_{GS,i}}{\mathrm{d}t}$$

- Breakdown, direct gate bias etc. → can be modeled through proper *ideal diodes* added to the circuit
- Other elements can be approximately taken as constant (like external parasitics) since the do not have a strong dependence on the bias point

Getting your way through the model jungle

- A nonlinear equivalent circuit is characterized by a topology and by analytical approximations to the input and output voltage dependence of the nonlinear elements
- As a matter of principle *all nonlinear elements have to depend on two voltages*, but for capacitors this leads to charge conservation problems
- For this reason many simple models exploit nonlinear capacitors depending *only on the voltage across them*
- Different combinations of topology and of models have led to an almost infinite variety of equivalent circuits
- We just mention two: the **Curtice** model family (MESFETs) and the **Chalmers** model family (HEMTs)

The “quadratic” Curtice model



The output generator model

Quadratic polynomial for dependency on v_{GS}

Effect of output resistance R_{DS}

Empirical tanh model for dependence on v_{DS}

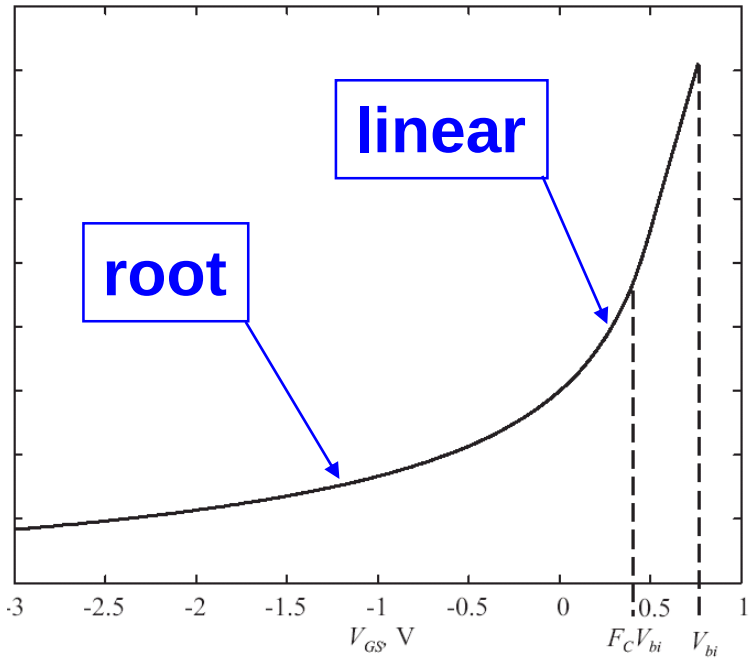
$$i_D = \begin{cases} \beta(v_{GS,i} - V_{TO})^2(1 + \lambda v_{DS,i}) \tanh(\alpha v_{DS,i}) & v_{GS,i} > V_{T0} \\ 0 & v_{GS,i} \leq V_{T0} \end{cases}$$

Zero subthreshold current

The capacitance model

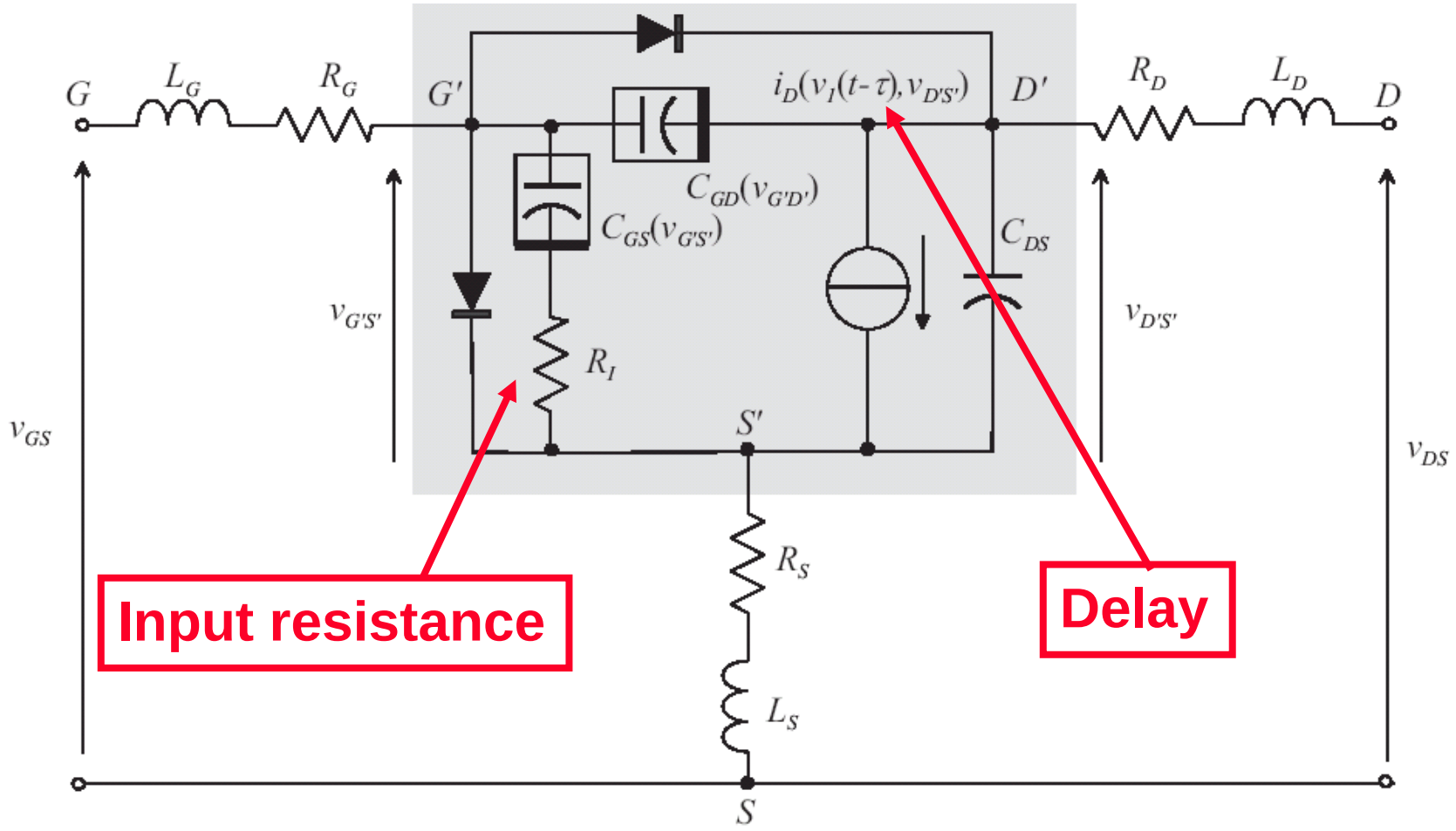
Simply the SPICE model for the junction capacitance of a pn junction!

$$C_{GS}(v_{GS,i}) = \begin{cases} \dfrac{C_{GS0}}{\sqrt{1 - v_{GS,i}/V_{\mathrm{bi}}}} & v_{GS,i} < F_C V_{\mathrm{bi}} \\ \dfrac{C_{GS0}}{\sqrt{1 - F_C}} \left[1 + \dfrac{v_{GS,i} - F_C V_{\mathrm{bi}}}{2V_{\mathrm{bi}}(1 - F_C)} \right] & v_{GS,i} \geq F_C V_{\mathrm{bi}} \end{cases}$$



- Same model for C_{GD} (feedback) as a function of v_{GD}

The “cubic” Curtice model



The output generator model

Cubic polynomial for dependency on v_{GS}

$$v_1 = v_{GS,i}[1 + \beta(v_{DS0} - v_{DS,i})]$$

Effect of output resistance R_{DS}

Empirical tanh model for dependence on v_{DS}

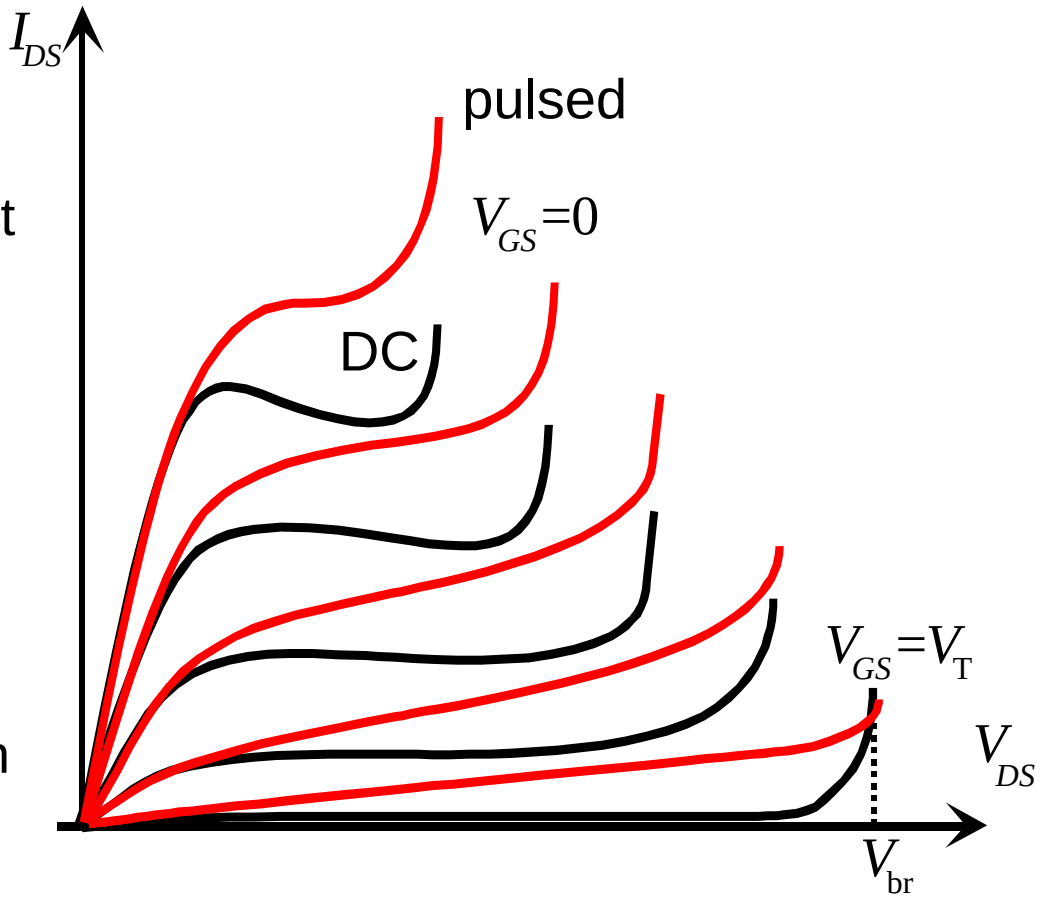
$$i_D = \begin{cases} (A_0 + A_1 v_1 + A_2 v_1^2 + A_3 v_1^3)(1 + \lambda v_{DS,i}) \tanh(\alpha v_{DS,i}) & i_D > 0 \\ 0 & i_D < 0 \end{cases}$$

Zero subthreshold current

- Better analog model, capacitance model similar to quadratic

Real devices often are more complex!

- To obtain really accurate models simple capacitance models as in Curtice are not enough
- Low-frequency dispersion effect make the static (DC) values R_{DS} and g_m quite different from the RF small-signal ones → difference in real DC and pulsed DC curves
- Accurate models should also take care of device self-heating
- In conclusion, real-world design requires something more complex than plain Curtice!

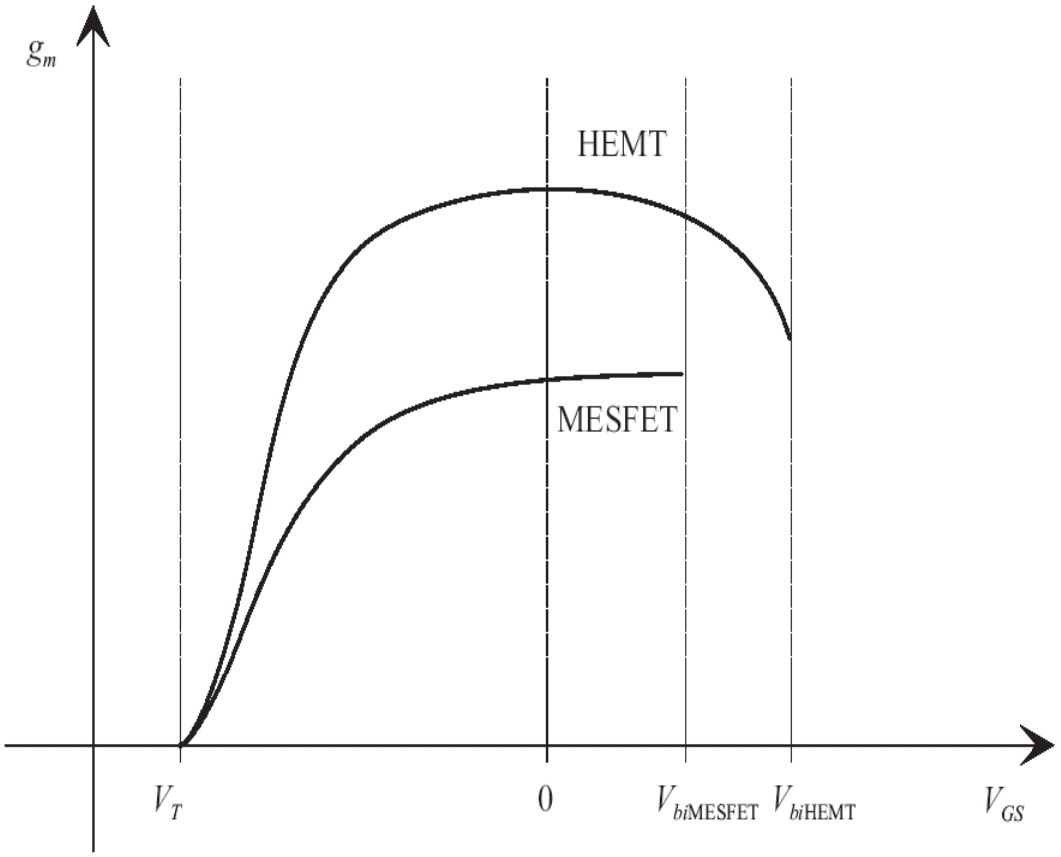


MESFET vs. HEMT models

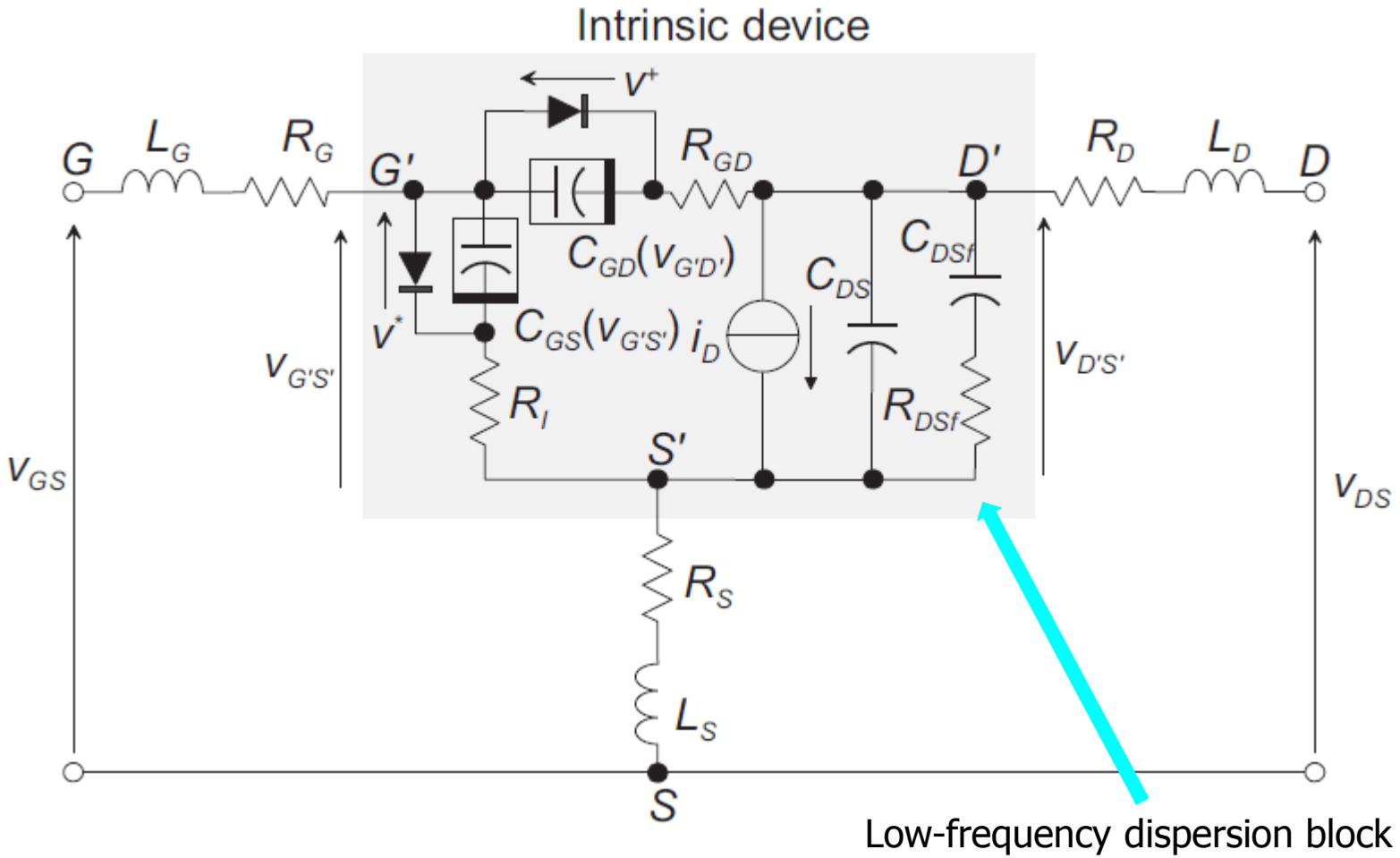
- HEMTs show a slightly different behaviour of the transconductance vs. input voltage, this makes the use of Curtice-like approaches inaccurate
- Specific models have been developed for HEMTs, e.g. the Chalmers (Angelov) model, which exploits different approximations of components
- Changing FET also the model change → there is no universal equivalent circuit, even though the intrinsic part is always similar → MOSFET models, LDMOS models…
- Still another story for bipolars!
- Most Si or GaAs foundries have developed proprietary models tuned to their process.

HEMT models

- Curtice-like models are unfit to simulate the transconductance saturation typical of HEMTs
- Dedicated models are needed → one of the most popular is the Chalmers (Angelov) model with a tanh like transcharacteristics



Chalmers model (intrinsic + resistive parasitics)



DC Chalmers model

$$I_{ds} = I_{pk}\left[1+\tanh(\psi)\right]\left(1+\lambda V_{ds}+L_{sb}\right)\tanh(\alpha V_{ds})$$

$$\psi = P_1(V_{gs}-V_{pk}) + P_2(V_{gs}-V_{pk})^2 + P_3(V_{gs}-V_{pk})^3 \ \ldots$$

$$P_1 = P_{sat}\left(1+\frac{B_1}{\cosh^2(B_2 V_{ds})}\right)$$

$$L_{sb} = L_{sb0}\cdot\left(e^{L_{sd1}V_{dgt}}-1\right)$$

$$L_{sd1} = L_{d1}\left(1-L_{g1}V_{gs}\right)$$

$$V_{dgt} = \frac{V_{ds}-K_{trg}V_{gs}}{V_{tr}}$$

Chalmers model capacitances

$$
\begin{aligned}
Q_{\mathrm{gs}} &= C_{\mathrm{gsp}} V_{\mathrm{gs}} + C_{\mathrm{gso}} \left[V_{\mathrm{gs}} + \frac{\ln\cosh\psi_1}{P_{11}} \right] (1 + \tanh\psi_2) \\
&- \frac{C_{\mathrm{gso}} \ln\cosh P_{10} \, (1 + \tanh P_{20})}{P_{11}} \, .
\end{aligned}
$$

$$
\begin{aligned}
Q_{\mathrm{gd}} &= C_{\mathrm{gdp}} V_{\mathrm{gd}} + C_{\mathrm{gdo}} \left[V_{\mathrm{gd}} + \frac{P_{400} \ln\cosh\psi_4}{P_{41}} \right] (1 + \tanh\psi_3) \\
&- \frac{C_{\mathrm{gdo}} P_{400} \ln\cosh P_{40} \, (1 + \tanh P_{30})}{P_{41}} \, ,
\end{aligned}
$$

$$
\psi_1 = P_{10} + P_{11} V_{\mathrm{gs}} + P_{12} V_{\mathrm{gs}}^2 \ \ldots \qquad \psi_2 = P_{20} + P_{21} V_{\mathrm{ds}} + P_{22} V_{\mathrm{ds}}^2 \ \ldots
$$

$$
\psi_3 = P_{30} + P_{31} V_{\mathrm{gs}} \qquad \psi_4 = P_{40} + P_{41} V_{\mathrm{gd}} .
$$

DC Chalmers model example

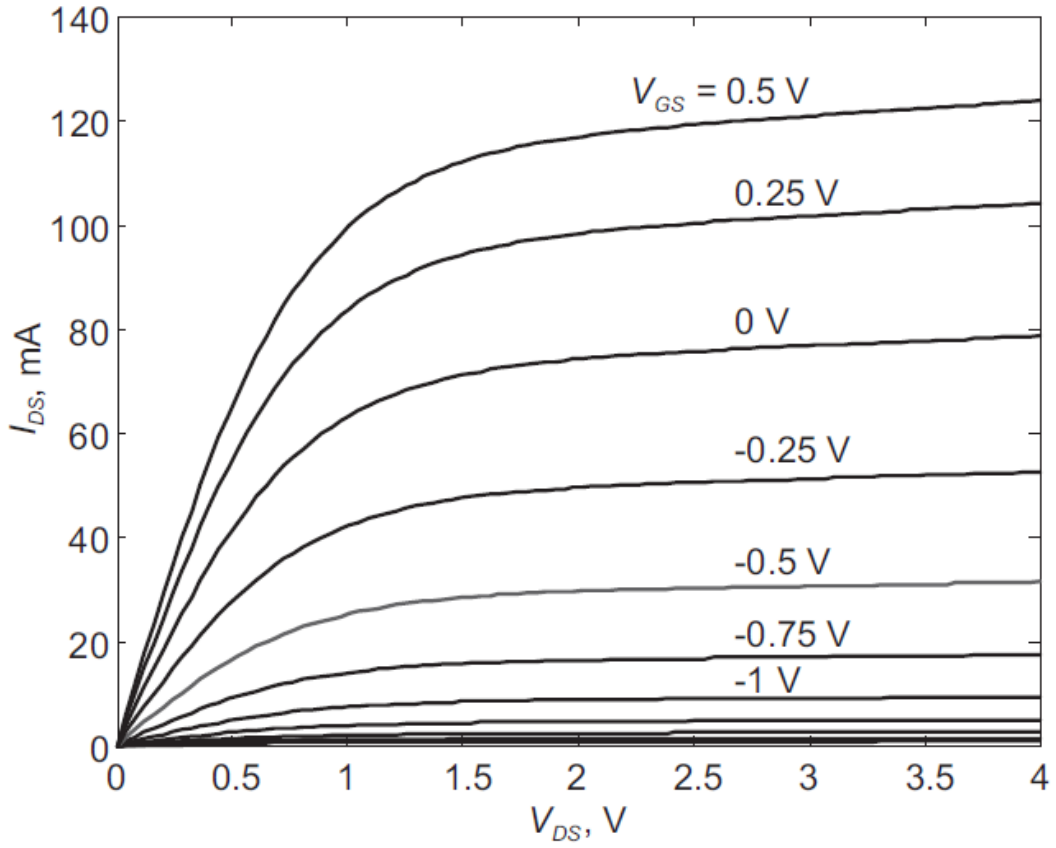


Figure 5.57 The Chalmers model DC characteristics. The parameters are: $I_{pk} = 69$ mA, $\lambda = 0.025$, $\alpha = 1.3$, $V_{pk} = -0.025$ V, $P_1 = 1.42$, $P_2 = 0$, $P_3 = -0.02$ (data from [45, Fig. 4, caption]). Note that the breakdown model is not activated in the drain voltage range shown.

Chalmers model transconductance

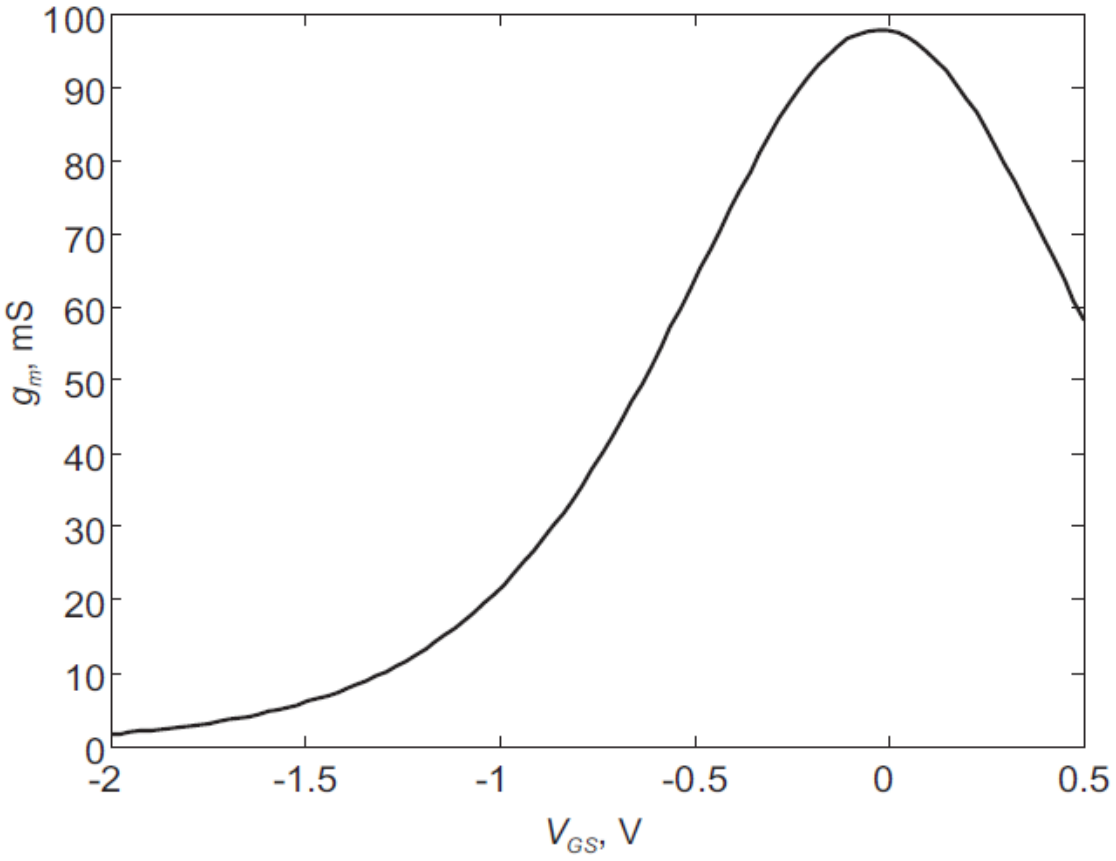


Figure 5.58 The Chalmers model DC transconductance from (5.35). The parameters are: $I_{pk} = 69$ mA, $V_{pk} = -0.025$ V, $P_1 = 1.42$, $P_2 = 0$, $P_3 = -0.02$ (data from [45, Fig. 4, caption]).