Examples, Exercises and Extension Material

The following text includes examples, exercises and extension material for the book *Foundations of Radio for Scientists and Technologists* by Christopher Coleman. This online resource will be supplemented by additional material at future dates in response to reader interests.

Realistic Tuned Circuits

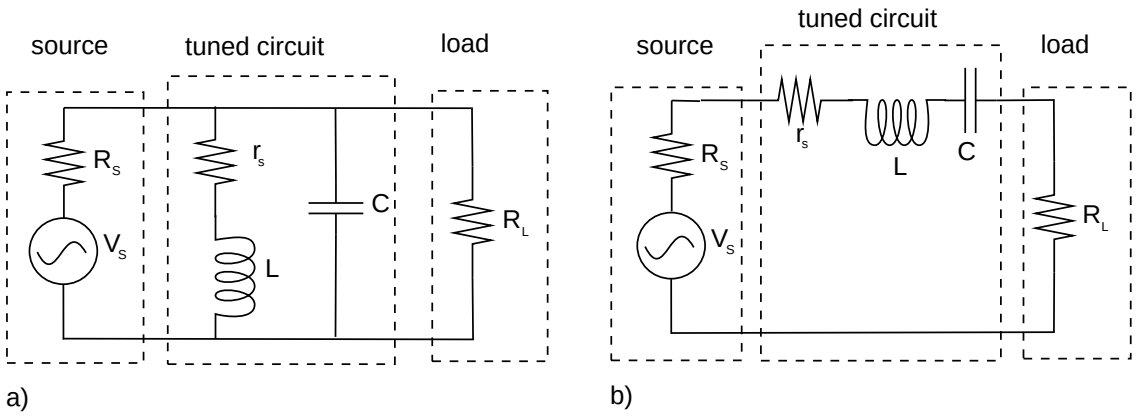

Figure 1: Realistic tuned circuits.

Although it is possible to make high quality capacitors with very low loss, it is difficult to make low loss inductors. In reality, the losses in realistic inductors can be quite large. A realistic inductor can modelled as a parasitic resistance r_s in series with a perfect (no loss) inductor L. Such loss is often expressed in terms of the unloaded quality factor $Q_U = \omega L/r_s$. Consider the circuit of Figure 1a, this shows a realistic parallel tuned circuit. The impedance Z of the tuned circuit will be given by

$$\begin{aligned} Z &= (j\omega L + r_s) \parallel \left(\frac{1}{j\omega C}\right) \\ &= \frac{j\omega L + r_s}{1 + j\omega C(j\omega L + r_s)} \\ &= \frac{(r_s^2 + \omega^2 L^2)}{r_s - j\omega L + j\omega C(r_s^2 + \omega^2 L^2)} \end{aligned} \tag{1}$$

The circuit will be resonant when $r_s^2+\omega^2L^2 = L/C$, i.e. at a frequency $\omega_0 = \sqrt{1/LC + r_s^2/L^2}$. Unlike the ideal case ($r_s = 0$), however, the impedance has a finite value $Q_U/\omega_0 C$ at resonance. Obviously, a high Q_U is essential for the efficient transfer of power from the source to the load. Now consider the admittance (i.e. $Y = 1/Z$) of the the tuned circuit

$$Y = \frac{r_s}{r_s^2 + \omega^2 L^2} + j\left(\omega C - \frac{\omega L}{r_s^2 + \omega^2 L^2}\right) \tag{2}$$

For impedances in parallel, their admittances are additive and so we essentially have a resistance $(r_s^2+\omega^2L^2)/r_s$ in parallel with capacitance C and inductance $(r_s^2+\omega^2L^2)/\omega^2L$. For large Q_U (i.e. $\omega L \gg r_s$), this will mean that the effect of r_s is to add a resistor $r_p = \omega^2L^2/r_s$ in parallel with the ideal tuned circuit. The effect will be a lower circuit Q and a consequent increase in bandwidth.

If we consider frequencies close to to the resonant frequency ω_0, i.e. $\omega = \omega_0 + \delta\omega$, then $r_s^2 + \omega^2L^2 \approx L/C + 2\omega_0L^2\delta\omega$ and hence $1/(r_s^2 + \omega^2L^2) \approx C/L - 2\omega_0C^2\delta\omega$. As a consequence

$$Y = \frac{r_sC}{L} - 2\delta\omega\left(r_s\omega_0C^2 - j\omega_0^2LC^2\right) \tag{3}$$

and for large Q_U, $Y \approx 1/r_p + 2jC\delta\omega$. In terms of the source voltage V_S, the voltage across the load can be written as

$$\begin{aligned} V_L &= V_S\frac{Z \parallel R_L}{R_S + Z//R_L} \\ &= V_S\frac{1}{1 + R_S\left(\frac{1}{R_L} + Y\right)} \end{aligned} \tag{4}$$

For large Q_U, we then have that

$$\begin{aligned} V_L &\approx V_S\frac{1}{1 + R_S\left(\frac{1}{R_L \parallel r_s} + 2jC\delta\omega\right)} \\ &= V_S\frac{R_L \parallel r_s}{R_L \parallel r_s + R_S + 2jR_S(R_L \parallel r_s)C\delta\omega} \\ &= V_S\frac{R_L \parallel r_s}{R_L \parallel r_s + R_S}\frac{1}{1 + 2jQ\frac{\delta\omega}{\omega_0}} \end{aligned} \tag{5}$$

where $Q = (R_S \parallel R_L \parallel r_s)\omega_0C = (R_S \parallel R_L \parallel r_s)/\omega_0L$. The bandwidth of the circuit will now be $B = \omega_0/Q$ and the maximum voltage across the load will be $V_SR_L \parallel r_s/(R_L \parallel r_s + R_S)$. As a consequence, the effect of the intrinsic resistance of the conductor is to reduce the level of peak voltage and to increase the bandwidth.

Exercise

Repeat the the above analysis for the case of the series tuned circuit of Figure 1b.

Practical Inductors

The design of inductors is an important part of practical RF engineering. One of the simplest inductors is the solenoid (see Figure 2a) for which the inductance (in micro Henries or μH) is given by

$$L = \frac{.0985 D^2 N^2}{4.5D + 10l} \tag{6}$$

where D is the solenoid diameter in cm, l is the length of the solenoid in cm and N is the number of turns. The inductor is often made of fairly thick wire so that it can be self supporting. However, if large inductances are required, the number of turns needs to be large and the wire will need to be thin, and/or closely spaced, if the length is not to be excessive. If the wire is closely spaced, there will be parasitic capacitance between the windings and this can cause a self resonance at quite low frequencies. If the wire is thin, this will increase the resistance per unit length and hence the parasitic resistance r_s. As a consequence, such inductors will have low Q_U. At high frequencies the situation is even worse since the current will only flow through a layer that is close to the surface of the conducting wire. This is known as the *skin effect*, a phenomenon whereby RF frequency currents can only penetrate a short distance $\delta = \sqrt{2/\omega\mu_0\sigma}$ into a conducting material ($\delta = 0.0066$mm for a copper wire at 100MHz). As a consequence, $r_s = d/2\pi a\delta\sigma$ where d is the total length of wire and a is the radius of the wire. From the above considerations, it can be seen that solenoids will be problematic at high frequencies if large inductances are required.

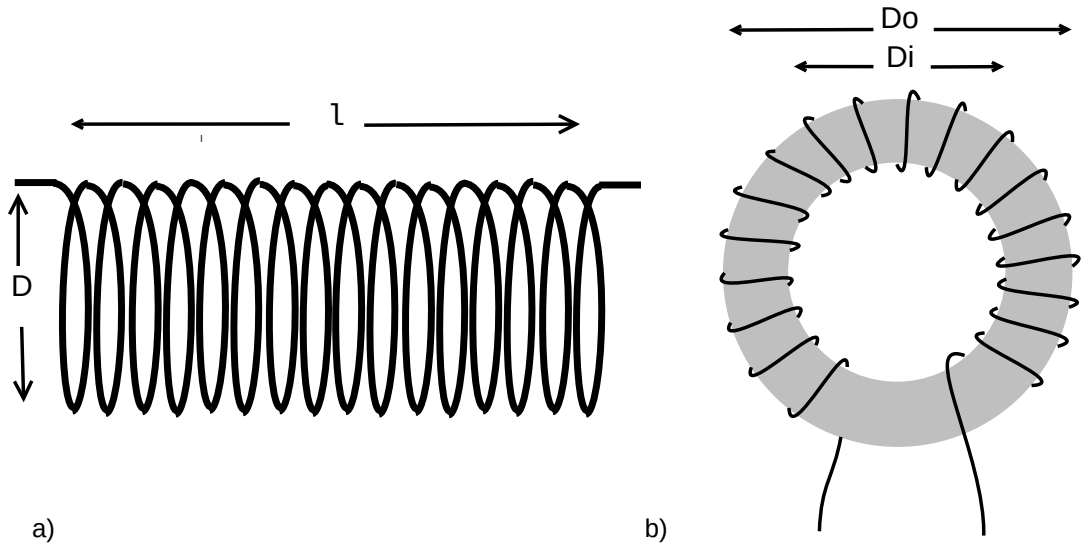

Figure 2: Practical Inductors.

To overcome the above problems, it is common to wind an inductor on a core with a high relative permeability. However, such cores will need to be low loss otherwise they will add additional parasitic resistance. Commonly, cores are made of iron. However, this is usually in the form of iron dust that is bound together by an epoxy resin. This avoids the eddy currents that would be induced in solid iron and lead to ohmic losses. Cores can also be made of ferrites, ceramic compounds containing iron oxide. These are non

conducting materials with high relative permeability. Such cores can greatly increase the inductance of solenoids that are wound over them. However, they will also enhance the magnetic field of the solenoid and this could cause unwanted transformer like interactions between different parts of an RF circuit. To avoid this the inductor is often wound on a toroid core. This will produce a closed magnetic field that will isolate itself from other components. A toroid inductor (see Figure 2b) will have an inductance

$$L = A_L N^2 \tag{7}$$

where A_L is known as the *inductance index* and is usually given as nano Henries per turns squared (a number normally supplied by the toroid manufacturer). This equation assumes that the windings are spread out uniformly around the toroid. In terms of more fundamental quantities

$$A_L = \frac{0.004\mu\pi A}{l} \tag{8}$$

where A is the cross sectional area of the toroid, μ is its permeability and l is the effective length of the winding ($l = \pi(Do+Di)/2$ for a winding that is spread out uniformly around the toroid).

We will consider the design of a simple bandpass filter using a parallel capacitor and inductance (see Figure 1a). We will assume that both the source and loads have impedances of 200Ω (i.e. $R_L = R_S = 200\Omega$) and that we require a filter with bandwidth 4MHz at a centre frequency of 10MHz. We assume, for the moment, that the parasitic resistance is zero and so the bandwidth is $B = \omega_0/Q$ where $Q = (R_S \parallel R_L)/\omega_0 L$. Since $\omega_0^2 LC = 1$, we have that $B = 1/R_S \parallel R_L C$. As a consequence, $2\pi \times 4 \times 10^6 = 1/100C$, i.e. $C = 1.25 \times 10^{-9}/\pi$ Farads. Then $L = 1/C\omega^2 = \pi \times 10^{-6}/5$ Henries. We consider the design of a solenoid with suitable inductance (i.e. $L = .628\mu H$). If we consider a solenoid with a diameter of 2cm and length 2cm, 6 implies that the inductor will need just under 7 turns. If we build an inductor with 7 turns, we can adjust it to the correct inductance by slightly opening out the windings. We now need to choose the wire thickness so that there is sufficient spacing between the windings. For 7 turns over 2cm, we will need a thickness that is less than 3mm and so, if we choose a thickness of 1mm, we will easily satisfy this and have a wire that is thick enough to be self supporting. We now need analyse whether we were justified in ignoring the parasitic resistance r_s. The length d of wire is approximately $N\pi D$ where D is the diameter of the solenoid and so $d = 440mm$. We will assume the wire to be made of copper and the the skin depth δ will be 0.021mm. Consequently, since $r_s = d/2\pi a\delta\sigma$ where a is the radius of the wire and σ its conductivity (5.5×10^7s/m in the case of copper), $r_s = 0.121\Omega$. This value is considerably less than than the source or load impedances and so the parasitic resistance can safely be ignored.

Exercise

Design a band pass filter with the same characteristics using a series resonant tuned circuit (see Figure 1b).

L Network Matching

An L network can be used to match impedances as shown in Figure 3.

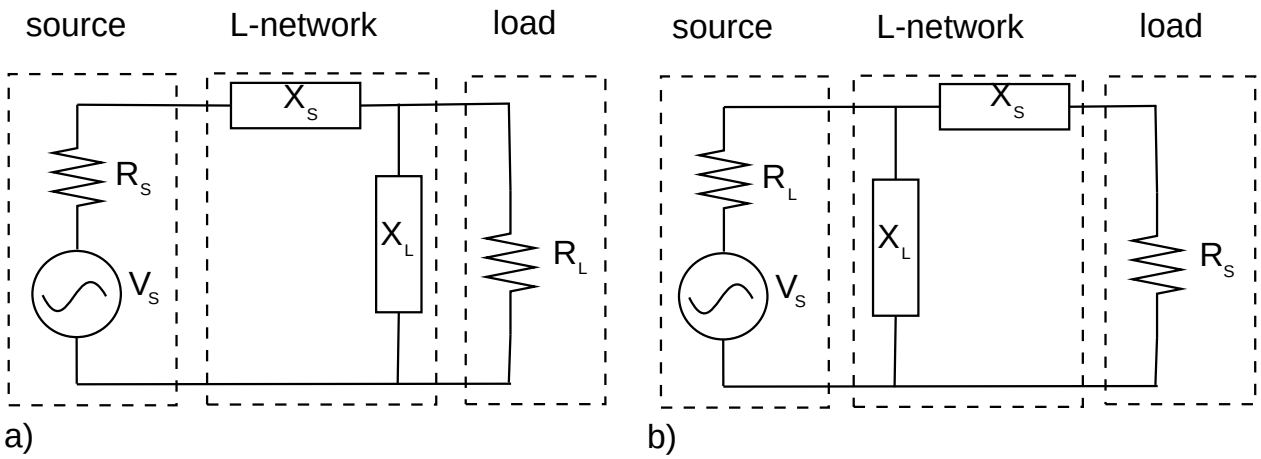

Figure 3: L network matching.

Figure 3 shows L matching networks that will allow the the matching of resistive sources and loads for $R_L > R_S$. We first calculate $Q = \sqrt{R_L/R_S - 1}$ and then reactance X_L follows from $X_L = \pm R_L/Q$. The arbitrary sign follows allows the choice of capacitive (+ sign) or inductive (- sign) reactance. We can calculate X_S using the relation $X_S = -X_L Q^2/(1+Q^2)$. If we choose X_L to be negative this will be realised by a capacitor C and X_S will be realised by an inductor L. Obviously, we choose the values of C and L to give the correct X_L and X_S at the desired operating frequency ω_0. This implies that $C = Q/\omega_0 R_L$ and $L = (R_L/\omega_0)Q/(1+Q^2)$.

We consider the example of matching a 50Ω source to a $100 + j100\Omega$ impedance load. The load is equivalent to a 200Ω resistance in parallel with a 200Ω reactance. For the moment we ignore the reactance and design the network as if the load is 200Ω alone. We have that $Q = \sqrt{200/50 - 1} = \sqrt{3}$. Then $X_L = \pm 200/\sqrt{3}$ and $X_S = -\frac{3}{4}X_L$. It will now be noted that the real load will generate some of the required X_L and so we adjust its value to X'_L such that $1/X'_L + 1/200 = 1/X_L$. If we choose X_L to be capacitive, we have that $X'_L = -200/(1+\sqrt{3})$ and $X_S = 150/\sqrt{3}$. If the matching is required to operate at a frequency of 10MHz we have $\omega_0 = 6.283 \times 10^7$, then the capacitor C that realises X'_L will be given by $C = (1+\sqrt{3})/200 \times 6.83 \times 10^7 = .2 \times 10^{-9}$, i.e. 200pF. We will also have that $X_S = 200/\sqrt{3}$ and so $L = X_S/\omega_0$, i.e. $L = 1.8936\mu H$. The fairly large value of inductance will make a toroid inductor a natural choice. For the frequency range 1 to 30MHz, the Amidon toroid T-86-2 is appropriate. This has an outer diameter of 1.75cm and an inductance index $A_L = 57$nH per turns squared. The toroid requires just under 6 turns to reach the required inductance with the winding uniformly spaced around the toroid. However, the length of the windings can be adjusted to achieve the exact inductance.

Exercise

Use an L network to match a source with impedance $5 + j10\Omega$ to a 50Ω load.

Capacitive Transformers

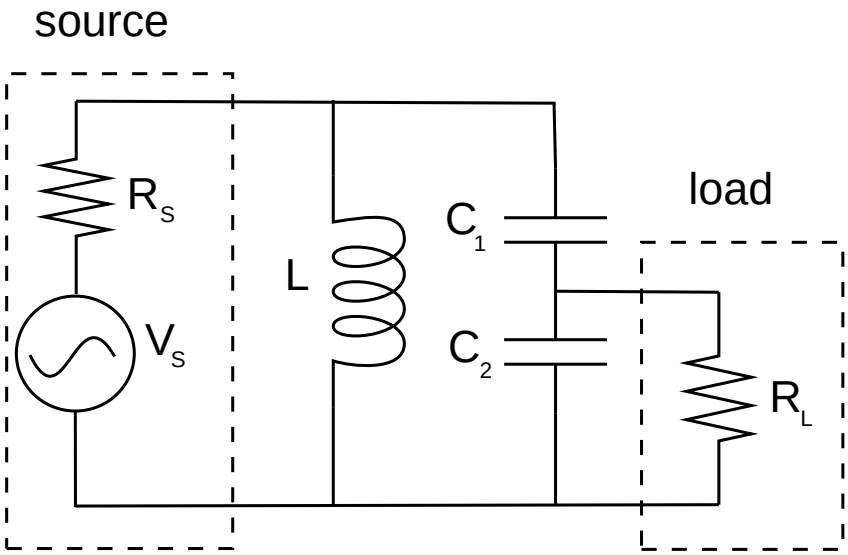

Figure 4: Capacitive transformer.

Figure 4 shows a circuit that uses a capacitive voltage divider as a transformer. Such a transformer is frequency selective and is useful when both impedance transformation and filtering is desirable. The transformer will only pass signals at, or around , the resonant frequency $\omega_0 = 1/\sqrt{LC}$ where $C = C_1C_2/(C_1 + C_2)$. For small deviations in frequency $\delta\omega$ around this resonance, the voltage across the load is

$$V_L \approx V_S \frac{1/n}{1 + j2Q\frac{\delta\omega}{\omega_0}} \tag{9}$$

where $n = (C_1 + C_2)/C_1$ and $Q = R_S/\omega_0 L$. We have a transformer with turns ratio n and filter with bandwidth $B = \omega_0/Q$.

We design a capacitive transformer to match a source impedance of $R_S = 800\Omega$ to a load impedance $R_L = 50\Omega$ and to act as a band pass filter of bandwidth 1MHz at frequency $15MHz$. The impedance transformation will require a turns ratio n of 4 and the bandwidth a Q of 15. A Q of 15 will imply that $L = 800/15\omega_0$ and, since a resonant frequency of 10MHZ will imply $\omega_0 = 6.283 \times 10^7$, we have that $L = .849\mu H$. For a turns ratio 4 we must have $C_2 = 3C_1$, so that $C = 3C_1/4$ and hence $\omega_0^2 = 1/LC$ implies that $C_1 = 4/3L\omega_0^2$. As consequence $C_1 = 398pF$ and hence $C_2 = 1194pF$.

Exercise

Design a capacitive transformer to match a 200Ω source to a 50Ω load to operate at a frequency of 30MHz with a bandwidth of 2MHz.

Bandpass Filter Design

Consider the situation where a direct digitising receiver is required for the frequency range range from $f_L = 6.5$MHz to $f_U = 9$MHz. We can build a bandpass filter for this frequency range by first designing a low pass filter with bandwidth $B = f_U - f_L$ (i.e. 2.5MHz) and then resonating the elements at the centre frequency $f_0 = \sqrt{f_L f_U}$ (i.e. 7.6485MHz). We

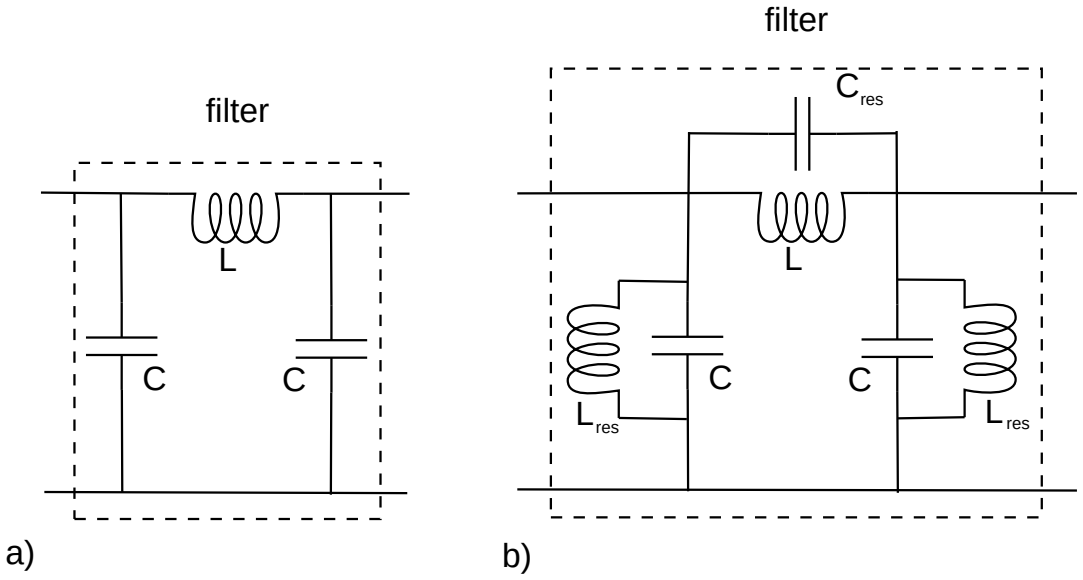

Figure 5: A 3 element low pass filter and its conversion to a bandpass filter.

first design the low pass filter and note that $\omega_B = 2\pi B = 15.708 \times 10^6$rad/sec. We will design a .5dB ripple Chebyshev filter. For such a filter, $L = \alpha R/\omega_B$ and $C = \beta/R\omega_B$ where $\beta = 1.5963$ and $\alpha = 1.0967$. From this we have that $L = 3.49\mu H$ and $C = 2nF$.

In order to convert the filter into a bandpass filter based on the frequency 7.6485MHz, we need to resonate the capacitances and inductor at this frequency. We require that $CL_{res} = 1/\omega_0^2$ and $C_{res}L = 1/\omega_0^2$ where C_{res} and L_{res} are the resonating capacitance and inductance. We then find that $C_{res} = 124pF$ and $L_{res} = 0.2165\mu H$.

Exercise

The above filter is of fairly low order and will not sufficiently attenuate strong signals that are within a few MHz of the pass band (the attenuation is only down by 20dB at 2.5MHz from the band edges). The bandpass filter in a digital receiver will act as an anti alias filter and will often need to have much greater attenuation, especially if the rate of digitisation is low. Figure 6 shows a 9 element Chebyshev filter with much better performance (the attenuation is more than 80db at a bandwidth away from the band edges). For terminating impedances R and a passband ripple of .122 (a .5dB ripple), the values of the capacitances will be $C_1 = 1.7504\omega_0/R$, $C_2 = 26678\omega_0/R$ and $C_3 = 2.7939\omega_0/R$. The values of the inductances will be $L1 = 1.269R/\omega_0$ and $L2 = 1.3673R/\omega_0$. Using this information, design a 9 element filter Chebyshev filter with a bandwidth 2.5MHz and then convert this into a bandpass filter with centre frequency $f_0 = 7.6485$MHz.

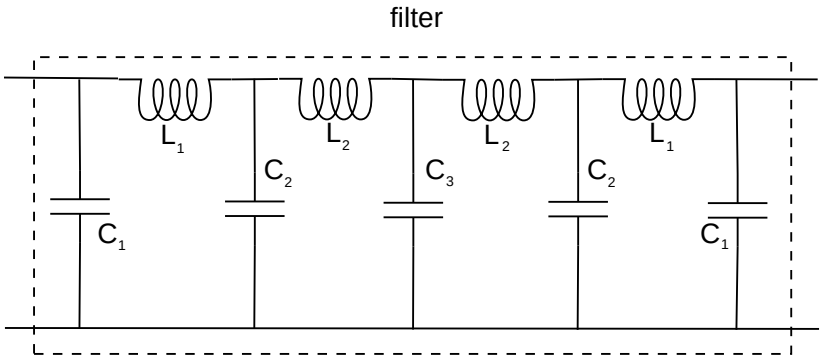

Figure 6: A 9 element low pass Chebyshev filter with 0.122 passband ripple.

Notch Filters

A series resonant circuit can also be used to create a notch filter (sometimes called a band stop filter), i.e. a filter that blocks out a range of frequencies. Consider the circuit of

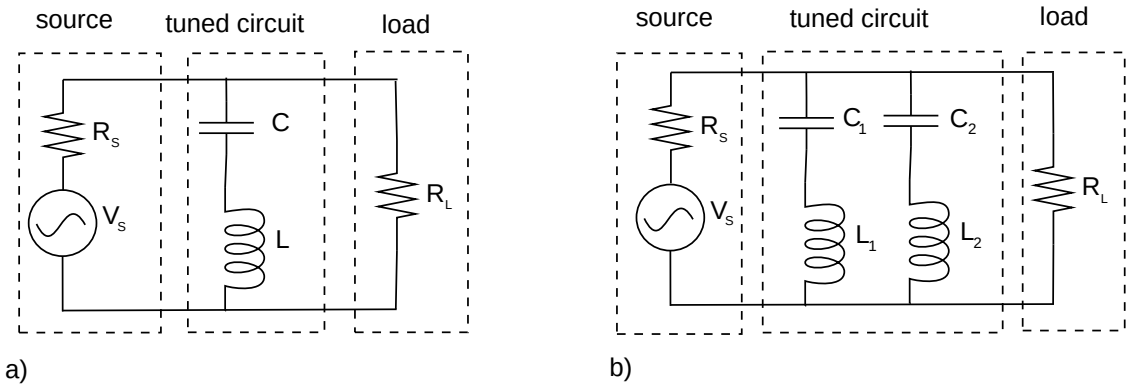

Figure 7: Notch (band stop) filters.

Figure 7a. The voltage drop across the load will be given by

$$\begin{aligned} V_L &= V_S \frac{\left(j\omega L + \frac{1}{j\omega C}\right) \parallel R_L}{\left(j\omega L + \frac{1}{j\omega C}\right) \parallel R_L + R_S} \\ &= V_S \frac{R_L(1-\omega^2 LC)}{(R_L+R_S)(1-\omega^2 LC) + j\omega C R_L R_S} \end{aligned} \tag{10}$$

From which the power dissipated in the load will be

$$P_L = \frac{V_L \bar{V}_L}{R_L} = \frac{V_S \bar{V}_S}{R_L} \left(\frac{R_L}{R_L+R_S}\right)^2 \frac{(1-\omega^2 LC)^2}{(1-\omega^2 LC)^2 + \omega^2 C^2 (R_L \parallel R_S)^2} \tag{11}$$

Note that zero signal is passed to the load at the series resonant frequency $\omega_0 = 1/\sqrt{LC}$ and that for frequencies well away from this the full signal is passed to the load.

The frequencies where the signal is reduced to 3dB of the maximum will occur when

$$\frac{(1-\omega^2 LC)^2}{(1-\omega^2 LC)^2 + \omega^2 C^2 (R_L \parallel R_S)^2} = \frac{1}{2} \tag{12}$$

which implies that

$$1 - \omega^2 LC = \pm\omega C(R_L \parallel R_S) \tag{13}$$

From this, the 3dB frequencies are given by

$$\omega = \frac{\mp C(R_L \parallel R_S) + \sqrt{C^2(R_L \parallel R_S)^2 + 4LC}}{2LC} \tag{14}$$

i.e. the bandwidth of the notch filter will be $B = (R_L \parallel R_S)/L$. If we define $Q = \omega_0 L/(R_L \parallel R_S)$, then the performance of the filter with different Q is illustrated in Figure 8 and from which it will be noted that Q now controls the sharpness of the filter.

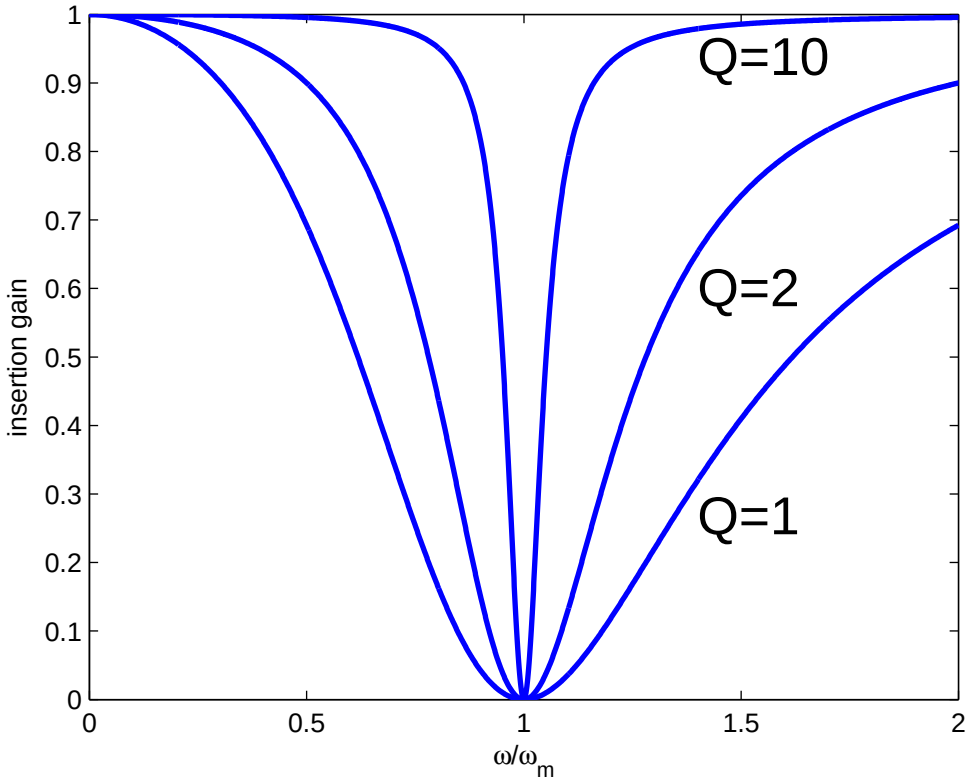

Figure 8: Performance of a notch filter.

In a digital receiver, dynamic range is is often a problem. Strong in band signals can exhaust the dynamic range of the A to D converters and overload the receiver. In the case of the receiver of example 6, the bandwidth contains the 41m broadcast band (7.2MHz to 7.6MHz) which itself contains several extremely strong broadcast signals. We can use the above notch filter to reduce the strength of these broadcast signals to an acceptable level. The broadcast signals will be AM with a bandwidth of about 10kHz and so we will need a filter of width 100kHz if the signal is to be attenuated by 20dB (we assume this to be sufficient otherwise the bandwidth of the above notch will need to be even wider). If the terminating impedances are 50Ω, $B = (R_L \parallel R_S)/L$ implies that $L = 250\mu H$ (the high inductance will require a toroid with large A_L). To notch out an AM signal centred on frequency ω_{AM}, we will need $C = 1/L\omega_{AM}^2$. If we need to notch out several signals, we can place several notch filters in parallel (see Figure 7b).

Exercise

Design a notch for use in the 60m broadcast band.

Designing a Common Emitter Amplifier

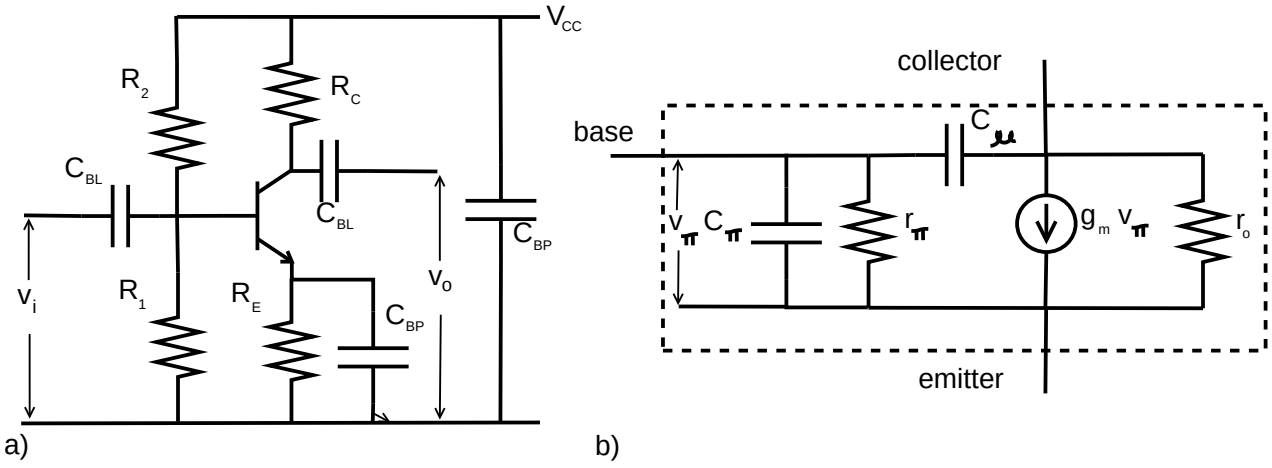

Figure 9: Biasing an NPN BJT amplifier.

We will consider the design of a simple BJT common emitter amplifier that is based upon an single silicon NPN transistor (see Figure 9a) with a current gain $\beta = 100$ (typical of a BF224). We assume that $V_{CC} = 6V$ and will need the quiescent I_Q to place the variation in output well away from the region of nonlinearity in the transistor characteristics (see Figure 10). A good rule of thumb is for there to be a quiescent voltage drop $V_{CC}/3$ across the collector resistor, the transistor and the emitter resistor (this is sometimes known as the 1/3 rule). For a 2V drop across the collector resistor we need $R_C I_Q = 2$ and for a 2V drop across the emitter resistor we need $R_E I_Q$ (note that the collector and emitter currents are approximately equal). This choice allows a reasonable voltage swing at the collector and plenty of feedback at the emitter to stabilise the operation of the transistor. With the collector voltage fixed, we then need to choose a quiescent current I_Q such that the the transistor operates as linearly as possible about this current, i.e. we choose operating point O in Figure 10. Once we know the operating point, resistance R_C follows as the slope of the load line. (Note that it is sometimes necessary to lower the voltage drop across R_E, especially when the supply voltage V_{CC} is low). We will assume that such an analysis of the transistor characteristics has suggested a current of $2mA$ and and hence a load resistor of $1k\Omega$. As a consequence we will also have an emitter resistance of $1k\Omega$. The voltage between the emitter and base will be approximately the diffusion voltage V_d (0.3V for germanium and 0.8V for silicon) and so the voltage at the base will be approximately $R_E I_Q + V_d$. We will assume the base current is negligible in comparison to the current that flows through the biasing resistors (R_1 and R_2) and then $R_E I_Q + V_d = V_{CC} R_1/(R_1 + R_2)$, i.e. $10^3 \times 2 \times 10^{-3} + 0.8 = 6R_1/(R_1 + R_2)$ from which $R_2 = 1.143R_1$. We still, however, need another condition to determine the bias resistors. It will be noted, however, the the emitter feedback mechanism requires that any change in emitter voltage arising from a

change in quiescent current ΔI_Q is much greater than the accompanying change in base voltage. This will mean that $\Delta I_Q R_E \gg \Delta I_Q (R_1 \parallel R_2)/(\beta+1)$, i.e. $(\beta+1)R_E \gg R_1 \parallel R_2$. It is usually sufficient to choose $R_1 \parallel R_2 = 10R_E$, sometimes known as the one tenth rule. We will now have that and $R_1 R_2/(R_1 + R_2) = 10R_E$, i.e. $R_1 R_2 = 10 \times 10^3 (R_1 + R_2)$, and from which $R_1 = 18.75k\Omega$ using the relation $R_2 = 1.143R_1$. Finally, we have that $R_2 = 21.43k\Omega$.

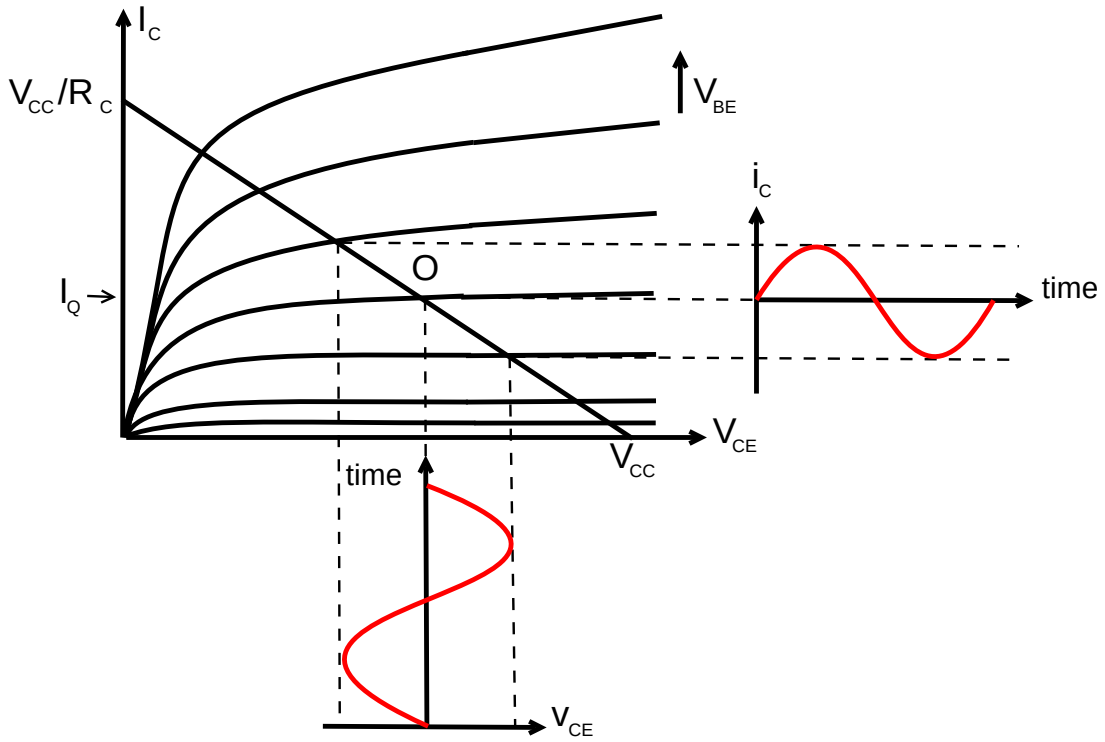

Figure 10: Input/output relationship for a biased amplifier.

The transconductance of the amplifier will be given by $g_m = I_Q/V_T = .08\Omega^{-1}$ and so the unloaded voltage gain of the amplifier will be $A = -g_m R_C = -80$, the output impedance will be $1k\Omega$ (note that r_o can be neglected) and the input impedance is $r_\pi = (\beta+1)/g_m = 1.26k\Omega$. This is all fine at low frequencies, but as frequency rises the parasitic capacitances of the BJT become a problem (see Figure 9b for a more realistic model of the BJT at higher frequencies). For a BF224, typical values for the parasitic capacitances are $C_\mu = 0.28pF$ and $C_\pi = 2pF$. This will mean that, taking into account the Miller result, there will be an effective shunt capacitance at the input of $C_i = 2 + 81 \times 0.28 = 24.7pF$. Consequently, at a frequency of 10MHz, the effective input capacitance will behave as a shunt reactance of magnitude 640Ω and, at a frequency of a 100MHz, as a shunt reactance of 64Ω. Clearly, as frequency rises, more and more RF will be shunted to ground by the Miller capacitance. It will be noted that the bias and collector resistances, can influence the the input and output resistances of the amplifier. In particular, for amplifiers at higher powers, we cannot afford a large power dissipation in the collector resistance. In this case, we can isolate the bias through RF chokes (inductances with a very large reactance at the desired operating frequency). This is illustrated in Figure 11a.

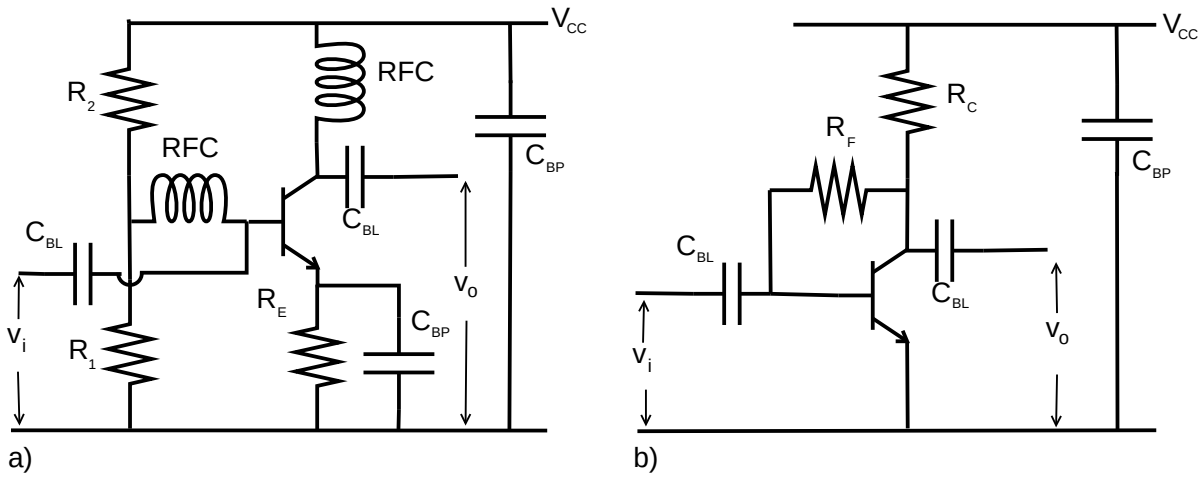

Figure 11: Alternative biasing circuits.

Exercise

By adjusting the quiescent current I_Q, and relaxing the 1/3 rule, redesign the amplifier to have a gain of -50 at low frequencies.

Alternative Bias Circuits

An alternative biasing system is shown in Figure 11b, but is not as stable as that shown in Figure 9a. If a quiescent collector current I_Q is required, then the base current will need to be $I_B = I_Q/\beta$ and the total current through the collector resistance will be $I_Q(1+1/\beta)$. As a consequence, $V_{CC} - V_{CE} = R_C I_Q(\beta + 1)$ and hence $R_C = (V_{CC} - V_{CE})/I_Q(\beta + 1)$. It will also be noted that $V_{CE} - V_{BE} = R_F I_B$ and so $R_F = (V_{CE} - V_{BE})/I_Q$ (once again V_d can be used as a first approximation V_{BE}). To provide for maximum swing in the RF signal, we usually $V_{CE} = V_{CC}/2$.

Although not as stable as the the biasing of the previous example, the circuit of Figure 11b does provide some stabilising feedback. If I_Q increases, then the quiescent collector voltage will decrease and, as a consequence, the current flowing through the feedback resistor will decrease. This will result in lower quiescent base current and hence a lower I_Q.

Exercise

Bias a BJT with $\beta = 100$ for a quiescent current of 2mA and with maximum swing available for the RF component.

Designing a Common Source Amplifier

Using a Fairchild BS170 NMOS transistor, we will design a common source amplifier (see Figure 12) with a unloaded voltage gain of -100 (to within 20 percent) and harmonics at

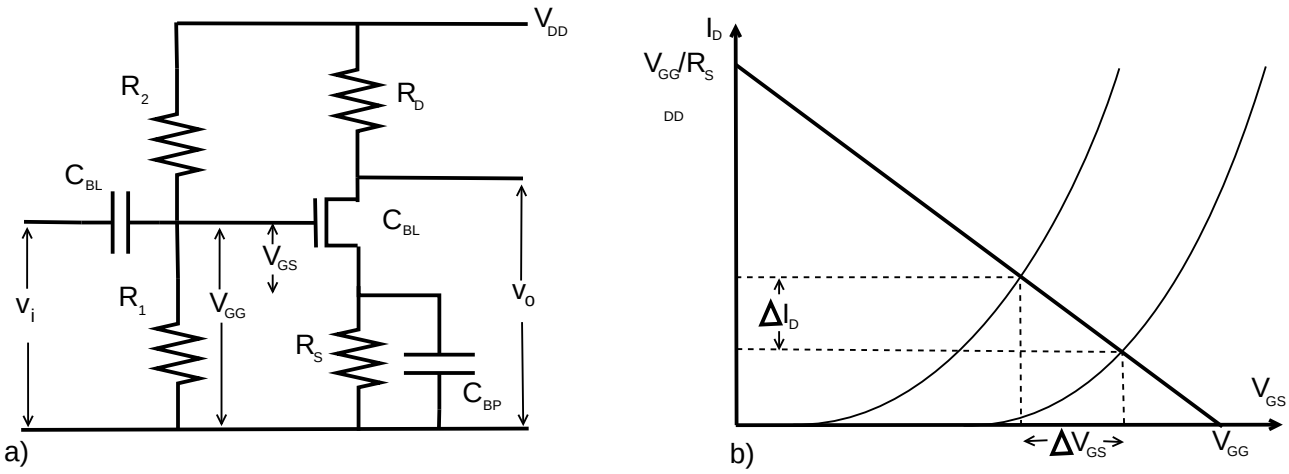

Figure 12: NMOS amplifier and biasing.

least -20dB below the fundamental for a 100mV amplitude input signal. (We will assume a supply voltage of 12V.) The relation between the source to gate voltage V_{GS} and the drain current I_D is given by

$$I_D = K(V_{GS} - V_T)^2 \tag{15}$$

where, for a typical BS170 NMOS, $K = 80mA/V^2$ and $V_T = 2.1V$. The parasitic capacitances are typically $C_{GS} = 24pF$, $C_{DS} = 17pF$ and $C_{GD} = 7pF$.

The drain voltage of the amplifier will be related to the input voltage v_o through

$$v_o = V_D - R_L K(V_{GS} + v_i - V_T)^2 \tag{16}$$

where V_{GS} is now taken to be the quiescent source to gate voltage. Consequently,

$$v_o = V_D - R_L K(V_{GS} - V_T)^2 - 2R_L K(V_{GS} - V_T)v_i - R_L K v_i^2 \tag{17}$$

Let $v_i = V_i \cos(\omega t)$ then $v_i^2 = V_i^2(1 + \cos(2\omega t))/2$ and so, for the harmonic (frequency 2ω) to be 20dB below the fundamental, we must have

$$\frac{V_i}{4(V_{GS} - V_T))} < \frac{1}{10} \tag{18}$$

on noting that a 20dB drop in power is equivalent to a voltage drop by a factor of 10. Since $I_{DQ} = K(V_{GS} - V_T)^2$, this condition implies that $I_{DQ} > K25V_i^2/4$ where I_{DQ} is the quiescent current through the transistor, i.e. $I_{DQ} > 5mA$. We will choose $I_{DQ} = 6mA$.

The transistor transconductance is given by $g_m = 2\sqrt{KI_{DQ}}$ and the voltage gain by $A = -g_m R_D = -2R_D\sqrt{KI_{DQ}}$ (we have neglected r_d in calculating the gain). If the current varies by ΔI the gain will vary by $\Delta A = -R_D\sqrt{K}\Delta I/\sqrt{I_{DQ}}$ and so $\Delta A/A = \Delta I/2I_{DQ}$. Consequently, since we must have $\Delta A/A < 1/5$, then $\Delta I_D < I_{DQ}/2.5$. From the data sheets for the BS170, the threshold voltage can vary between 0.8V and 3V and so the range of variation in V_{GS} will be $\Delta V_{GS} = 2.2V$. Referring to Figure 12, we must choose R_S such that $\Delta I_{DQ} > \Delta V_{GS}/R_S$, i.e. $R_S > \Delta V_{GS}/\Delta I_{DQ}$. Since $\Delta I_D < I_{DQ}/2.5$ and $\Delta V_{GS} = 2.2V$, we must have that $R_S > 5.5/I_{DQ}$. We will choose $R_S = 1k\Omega$.

For the a voltage gain of -100, we will need $g_m R_D = 100$, i.e. $2R_D\sqrt{KI_{DQ}} = 100$ and therefore $R_D = 50/\sqrt{KI_{DQ}}$. For quiescent current $I_{DQ} = 6mA$ we will now have that $R_D = 2.28k\Omega$. In order to generate the quiescent current I_{DQ}, we need to choose appropriate values of the divider resistors R_1 and R_2. The input resistance of the FET is very large (in the region of many $M\Omega$) and so the resistances can be chosen to be of the order of several hundred $k\Omega$. We will need a quiescent V_{GS} such that $K(V_{GS}-V_T)^2 = 6mA$, i.e. $V_{GS} - V_T = 0.274V$. Since $V_{GS} = R_1 V_{DD}/(R_1 + R_2) - R_S I_{DQ}$, we have $V_T + .274 = R_1 V_{DD}/(R_1+R_2) - R_S I_{DQ}$ and so $2.374 = V_{DD}R_1/(R_1+R_2) - 10^3 \times 6 \times 10^{-3}$. If we assume a value of $200k\Omega$ for R_2 then $6.+2.374 = 12R_1/(R1+R2)$ from which $8.374R_2 = 3.626R_1$, i.e. $R_1 = 462\Omega$.

For this amplifier the Miller effect will cause an additional shunt capacitance $(1 - A)C_{GS} = 567pF$ and so the total capacitance at the amplifier input will be $C_i = (1 - A)C_{GS} + C_{GS} = 592pF$. As a consequence, a lot of the input power will be shunted to ground by this capacitance. If the RF source has impedance R_{source}, the power will be reduced by 3dB when $\omega = 1/C_i R_{source}$. For a source impedance of 100Ω this will imply a frequency of 2.7Mhz as the effective upper limit of operation. This is not a very good RF amplifier.

Exercise

Redesign the amplifier for a gain of -40 and harmonics at least -26dB below the fundamental.

Combating the Miller Effect

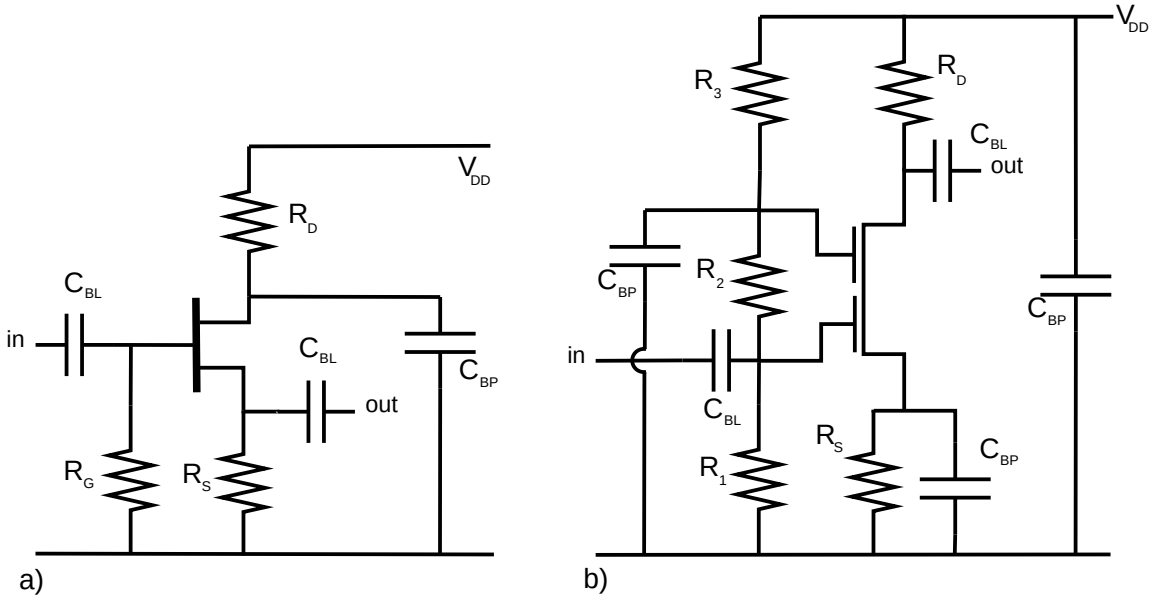

Figure 13: Amplifiers that do not suffer from the Miller Effect.

We have seen in the above example that the Miller effect can have an extremely detrimental effect upon the operation of an amplifier at RF frequencies. Figure 13 shows two examples of amplifiers that do not suffer from the Miller effect. Figure 13a shows a common drain (sometimes known as a source follower) amplifier. This amplifier only has a voltage gain of about 1 (the reason for its lack of Miller effect), but very lightly loads the signal source due to its high input impedance. However, it can have a low impedance output and therefore is useful as a buffer (it can be used to buffer an oscillator for example). The amplifier shown in Figure 13 is based on a JFET, a typical example of which is the J309. This transistor has a threshold voltage $V_T = -2.5V$ and $K = 6 \times 10^{-3} A/V^2$. Because of the large negative value of V_T, we have the option of self bias, i.e. the gate is grounded through a large gate resistance (a value of $500k\Omega$ is appropriate) and the current through the source resistor makes the source negative with respect to the gate. The quiescent drain current I_{DQ} will satisfy

$$I_{DQ} = K(-I_{DQ}R_S - V_T)^2 \tag{19}$$

We will design an amplifier with an output impedance of 100Ω. The output impedance is given by $g_m^{-1} \parallel R_S = R_S/(1 + g_m R_S)$. If we assume $R_S \gg g_m^{-1}$ then the output impedance is approximately g_m^{-1} and, since $g_m = 2\sqrt{KI_{DQ}}$, we will need $2\sqrt{KI_{DQ}} = 1/100$, i.e. $I_{DQ} = 1/4K \times 10^4 = 4.17mA$.From 19 we now obtain that $R_S = 400\Omega$.

Although this amplifier does not suffer from the Miller effect, there is still the gate source capacitance C_{GS} to deal with. If the RF source has impedance R_{source}, the power will be reduced by 3dB when $\omega = 1/C_{GS}R_{source}$. In the case of a J309 $C_{GS} = 5pF$ and so, for a source impedance of $1k\Omega$, this will imply a frequency of 32Mhz as the effective upper limit of operation. In the case that the amplifier is used as a buffer for a Colpitts oscillator, however, C_{GS} can be incorporated into the oscillator capacitance and does not cause a problem.

Figure 13b shows the circuit of a cascode amplifier that is based on a dual gate MOSFET. This has a similar behaviour to the common source amplifier, but without the Miller effect. The circuit consists of a common source amplifier follow by a common gate amplifier whose input impedance is g_m^{-1} also serves as the load to the common source amplifier. As a consequence, the first amplifier has a voltage gain of 1 (if we ignore r_d), i.e. no Miller effect. The common gate amplifier will suffer from the Miller effect, but the reactance due to the Miller capacitance will be negligible in comparison to the input impedance. We will design an amplifier that has a gain of $A = -10$ (to within 30 percent) that is based on 40673 MOSFET and has a supply voltage of 15V. We will normally set the bias at the upper gate several volts above that at the lower gate to ensure that both the FETs in the device run in their saturation region and the current will therefore be controlled by the source resistor. From example 9 we find that the variation ΔI in quiescent drain current I_{DQ} is related to the variation ΔA in voltage gain through $\Delta A/A = \Delta I/2I_{DQ}$ and, since $\Delta A/A < 3/10$, we have $\Delta I < 3I_{DQ}/5$. For the 40673, V_T varies between -4V and -1V with a typical value of -2.5V, i.e. the variation is $\Delta V_T = 3V$. We will need to choose an R_S that ensures that $\Delta I_{DQ} > \Delta V_{GS}/R_S$ and so $R_S > \Delta V_T/\Delta I$ and, since $\Delta I < 3I_{DQ}/5$, $R_S > 5/I_{DQ}$. We have that the voltage drop across R_S will need to be greater than 5 and so we choose it to be 6V, i.e. $R_S I_{DQ} = 6$. This voltage drop will leave us with a 9V drop across the transistor and drain resistance R_D. We will choose the voltage drop across R_D to be 6V and therefore $R_D = R_S$.

For a 40673, with the upper biased so that both FETs are in saturation,

$$I_D = K(V_{GS1} - V_T)^2 \tag{20}$$

where $K = 2.5mA/V^2$ for a typical device and V_{GS1} is the voltage between the source the lower gate. The voltage gain is given by $A = g_m R_D$ if we neglect r_d and so we must have that $g_m R_D = 10$. Since $g_m = 2\sqrt{KI_{DQ}}$, we have that $\sqrt{KI_{DQ}}R_D = 5$. However, we also have that $R_D I_{DQ} = 6$ and so $\sqrt{K}/\sqrt{I_{DQ}} = 5/6$, i.e. $I_{DQ} = 3.6mA$. As a consequence $R_D = R_S = 1.67k\Omega$. From 20 we now obtain that $V_{GS1} - V_T = 1.2$ from which $V_{GS1} = -1.3$. As a consequence the voltage at gate 1 will need to be 4.7V and we will choose the voltage at gate 2 to be 10V to ensure both FETs are in saturation. We can generate this bias if we choose $R_1 = 94k\Omega$, $R_2 = 106k\Omega$ and $R_3 = 100k\Omega$.

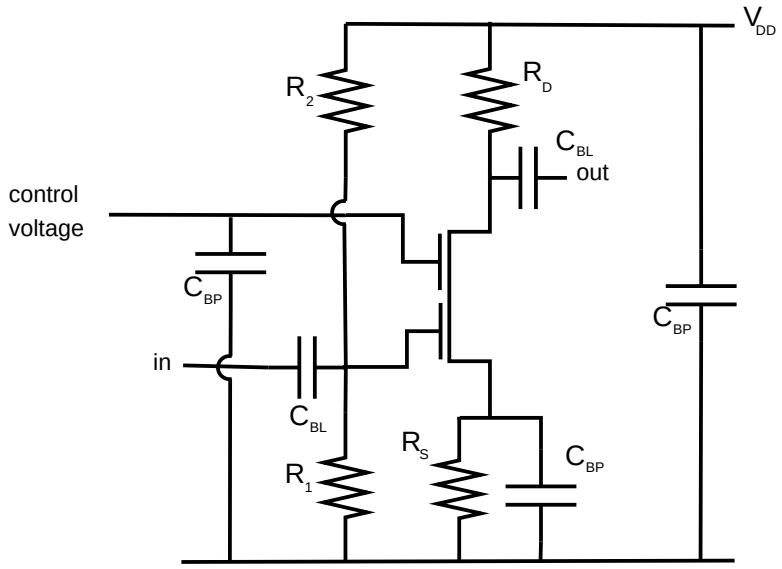

Figure 14: Dual gate MOSFET amplifier with voltage controlled gain.

A particularly useful application of the dual gate MOSFET is as an amplifier with voltage controlled gain (see Figure 14). Instead of fixing the voltage at the upper gate, we now place a control voltage at this gate. For several volts above that of the source, the transistor will exhibit full gain. As this voltage drops, however, the gain will reduce until it reaches zero at negative voltages.

Exercise

Redesign the source follower amplifier for an output impedance of 50Ω.

Exercise

Design an NPN BJT emitter follower amplifier with an output impedance 50Ω.

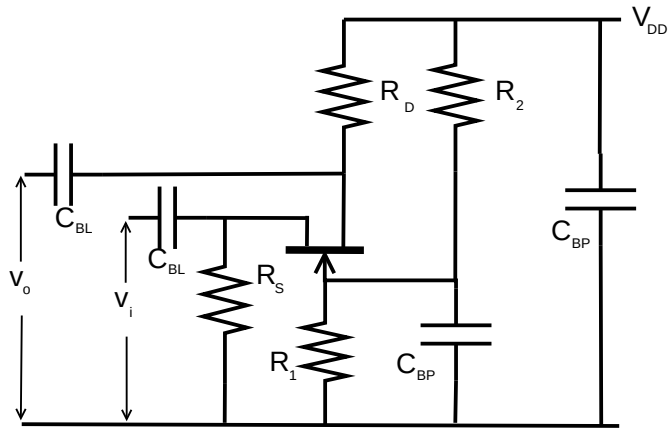

Figure 15: The common gate amplifier.

The Common Gate Amplifier

Figure 15 is the the circuit of what is known as a common gate amplifier. This amplifier still suffers from the Miller effect, but the input impedance is of low impedance ($g_m^{-1} \parallel R_S$) and the reactance due to the Miller capacitance is negligible by comparison. However, such amplifiers are useful when they are to be driven by a low impedance source (an antenna for example). The figure shows an amplifier using a JFET and for which self biasing is an option, i.e. we can remove the biasing resistor R_2 and make R_1 a short circuit (we can obviously also remove its bypass capacitor). Bias is set by choosing a suitable value of the source resistor R_S. For the amplifier of Figure 15, find values of R_S and R_D to produce an unloaded voltage gain of -10 and an input impedance of 50Ω (you can assume $R_S \gg g_m^{-1}$).

Designing a Colpitts Oscillator

Consider the design of an FET Colpitts oscillator based on a common drain JFET amplifier (see Figure 16). We will design around a 2N3819 JFET for which $V_t = -3V$, $K = 10^{-3}A/V^2$ and $C_{GS} = 4pF$. At oscillation, the theory implies that

$$\omega = \sqrt{\frac{C_1 + C_2}{LC_1C_2}} \quad \text{and} \quad g_m = \omega^2 C_2 C_1 r_s \tag{21}$$

Resistor r_s is the series resistance of the inductor and is related to Q_U, its unloaded Q, through $Q_U = \omega L/r_s$. To reduce the effect of transistor capacitance, C_1 and C_2 should have values much greater than the input capacitance ($4pF$). We need to choose the bias such that $g_m = \omega^2 C_2 C_1 r_s$ is satisfied. However, due to the high variation in component manufacture, it is almost impossible to exactly satisfy this relation. Consequently, we instead choose bias such that $g_m > \omega^2 C_2 C_1 R$ in order to ensure that oscillations start. Then, as the oscillations grow in amplitude, the value of g_m will fall due to gain compression and the condition of equality will be satisfied at some point. We will assume that $C_1 = C_2 = C$, but note that for C_1, C must be then increased by C_{GS} in any calculation in order to take into account the parasitic capacitance of the transistor. It is normal to

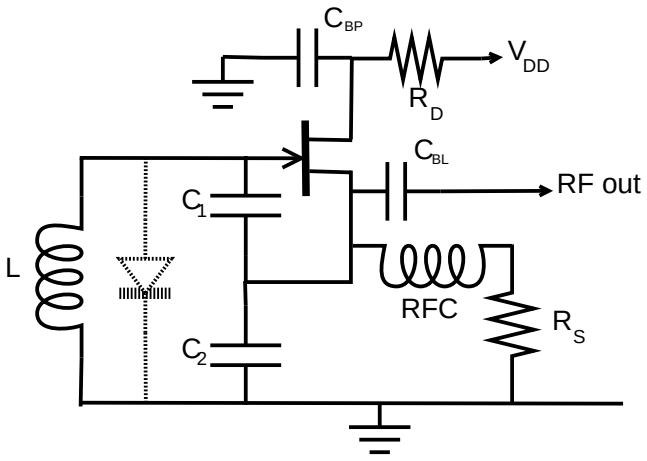

Figure 16: A simple JFET common drain Colpitts oscillator.

choose $C_1 \gg C_{GS}$ in order to ensure that the design is not overly affected by variations in transitor characteristics (a problem with real transistors). We will choose a value of 500pF for C, and then $C_1 = 504$pF and $C_2 = 500$pF. In order the circuit to oscillate at 10MHz, we will need a value of $L = (C_1 + C_2)/C_1C_2\omega^2 = 1.01\mu H$. Then, in order to start oscillation, we will need

$$g_m > (C_1 + C_2)r_s/L = \omega(C_1 + C_2)/Q_U \tag{22}$$

If we assume an unloaded Q of 50 (a value that is well within the range of practical inductors), we will need $g_m > .0013$. We choose $g_m = .002$ in order that the oscillation condition is well satisfied and note that $g_m = 2\sqrt{KI_{DQ}}$ where I_{DQ} is the quiescent current. As a consequence,$I_{DQ} = g_m^2/4K = 1mA$. Since $I_{DQ} = K(V_{GS} - V_T)^2$, we will need $V_{GS} = V_T + 1$ for the desired current to flow. As a consequence there will need to be a voltage drop of 2 volts across the source resistor R_S, i.e. this resistor will need to have a value of $2k\Omega$. As the amplitude of oscillations rise, the transistor will stop conducting for large negative voltage swings and this will lead to a drop in g_m and the desired gain compression leading to equilibrium.

Exercise

Redesign the above oscillator to run on a frequency of 7Mhz.

The Dual Gate MOSFET mixer

The ability to control gain through the second gate of a dual gate MOSFET makes it a useful device for mixing purposes. Figure 17 shoes a typical mixer circuit. The lower half of the MOSFET is configured as a self biasing amplifier, with the upper gate used to control gain. However, it will be noted that the bias of this gate set to the source voltage. This makes it possible to switch the transistor on and off with relatively low local oscillator voltages. At the MOSFET drain there is a parallel tuned circuit that

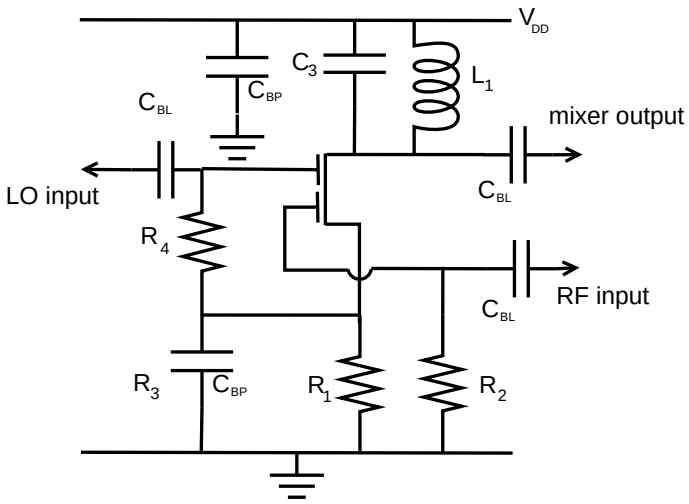

Figure 17: A dual gate MOSFET mixer.

selects the desired mixer product. A suitable dual gate MOSFET for such a mixer is the NPX BF995.

A Simple Direct Conversion Receiver

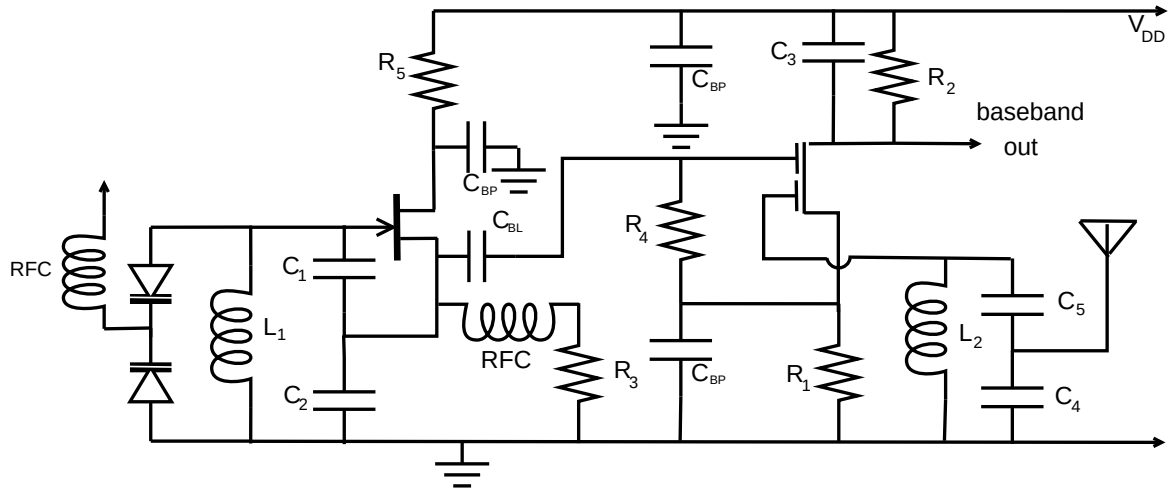

Figure 18: A simple direct conversion receiver based on a dual gate MOSFET mixer.

We can bring the above oscillator and mixer designs together to form a simple direct conversion receiver, as shown in Figure 18. Since the relevant output at the drain of the mixer will be the base band, the tuned circuit has been replaced by a parallel combination of resistor and capacitor to act as a low pass filter. From the data sheets for the BF995, we need the quiescent lower gate voltage V_{GS1} to be well above the pinch off voltage V_T (about $-1.6V$ for the BF995) in order to obtain large drain current variations when the upper gate voltage V_{GS} is varied. However, V_{GS1} should not be so high that it could cause the current to fall outside the limits of the device. From the data sheets, a reasonable compromise is $-.2V$ for which the quiescent drain current is 2mA. In order to achieve

the required bias we will need a source resistor R_1 of value 100Ω. We will assume supply voltage V_D of 8V and choose a value of the drain resistor R_2 such that we can have maximum possible voltage swing at the drain. We set the drain at a quiescent voltage 5V so that R_2 will need to drop a voltage of 3V. Consequently, will have the value of $1.5k\Omega$ for R_2. If the baseband is BHz wide, capacitor C_3 now needs to be chosen to be $C_3 = 1/R_2\pi B$. For a 4kHz baseband, this will imply that $C_3 = 53nF$.

Exercise

Design a 3 element Chebyshev filter to replace the capacitor C_3.

A Simple Regenerative Receiver

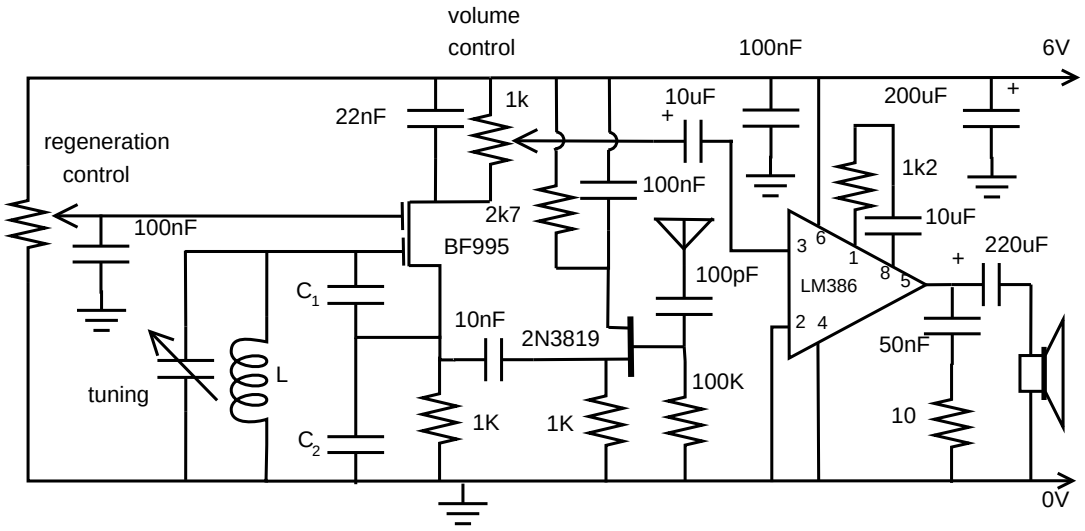

Figure 19: A simple regenerative receiver.

Another simple receiver architecture is that based upon regeneration. Regeneration has the dual advantages of increasing both the sensitivity and selectivity of a receiver. Further, such receivers (in their valve form) were the staple of early consumer radio. Figure 20 shows a simple realisation of a regenerative receiver. The receiver consists of a dual gate MOSFET amplifier that is configured as a Colpitts oscillator in order to produce positive feedback. The gain however is set just before the point of oscillation. The RF input is fed into the MOSFET source via a source follower amplifier which isolates any accidental oscillations from the antenna. In addition, this feature can act as an active antenna (a device we will discuss later).

Exercise

Generate suitable values for C_1, C_2 and L for a receiver to operate at a frequency of 14MHz.

Crystal Ladder Filters

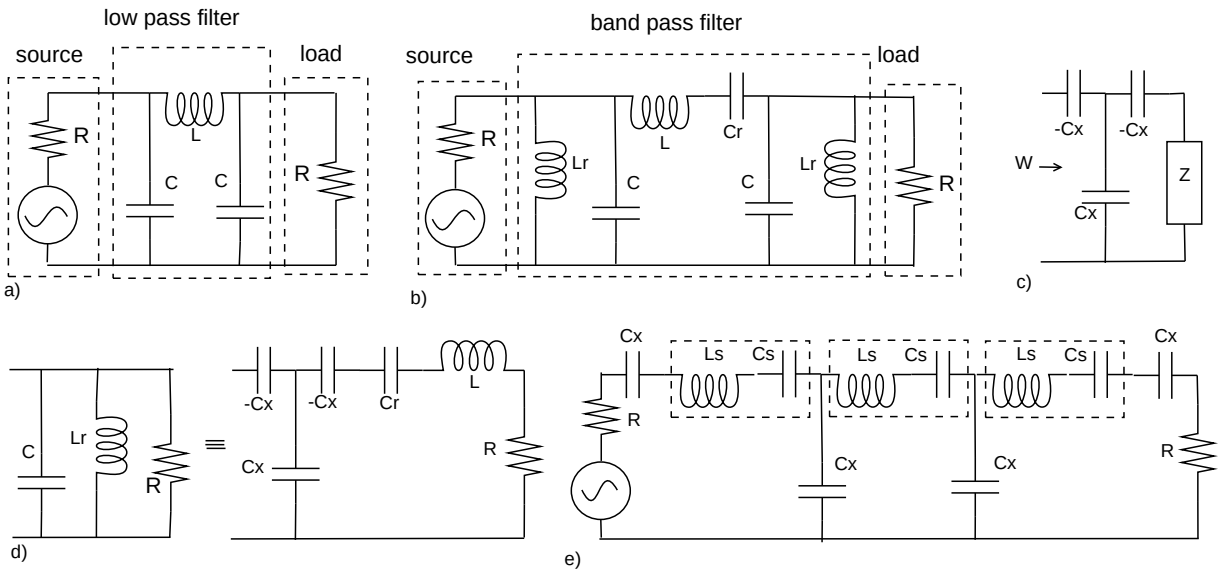

Figure 20: Butterworth low pass and band pass filters.

Figures 20 a shows a simple 3 element Butterworth low pass filter (bandwidth B in Hz and terminating impedances R) where $L = 2R/\omega_B$ and $C = 1/R\omega_B$ ($\omega_B = 2\pi B$). This can be transformed into a bandpass filter with bandwidth B, and centre frequency f_c, by adding inductances L_r and capacitance C_r that resonate with C and L respectively at this frequency. We then obtain the bandpass filter shown in Figure 20b. The parallel resonant circuits in the above filter can be inconvenient and so we now looks at ways of converting this into a series resonant circuit. Key to this is the impedance inverting circuit shown in Figure 20c. The impedance W looking into this circuit is given by $1/\omega^2 Cx^2 Z$. Unfortunately, the circuit requires a negative capacitance. However, we will find in our target application that this negative capacitance is cancelled by real capacitance and therefore does not pose a problem for circuit realisation. Figure 20d shows the the parallel resonant circuit of the filter output in parallel with the filter load R (similar considerations apply at the source end). We claim that this equivalent to the circuit on the right. It must be emphasised that this is only the case for frequencies around resonance, but for narrow band filters this is not a problem. The admittance looking into the right hand circuit will be given by

$$Y = \omega^2 C_X^2 \left(\frac{1}{j\omega C_r} + j\omega L + 2R \right) \tag{23}$$

By the definition of C_r, we know that $L = 1/\omega_c^2 C_r$ and so

$$Y = \omega^2 C_X^2 \left(j\omega_c L \left(\frac{\omega}{\omega_c} - \frac{\omega_c}{\omega} \right) + R \right) \tag{24}$$

where ω is the angular frequency ($\omega = 2\pi f$). However, around resonance frequency ω_c,

this must look like the admittance looking into the circuit on the left, i.e.

$$\begin{aligned} Y &\approx j\omega C - \frac{1}{j\omega L_r} + \frac{1}{R} \\ &= j\omega_c C\left(\frac{\omega}{\omega_c} - \frac{\omega_c}{\omega}\right) + \frac{1}{R} \end{aligned} \tag{25}$$

For susceptances and conductances to be approximately equal we will need $C_X = \sqrt{CC_r}$ and $R = 1/\omega_c C_X$. We finally arrive at the filter in Figure 20e, where $L_s = L$ and $C_s = C_r - 2C_X$.

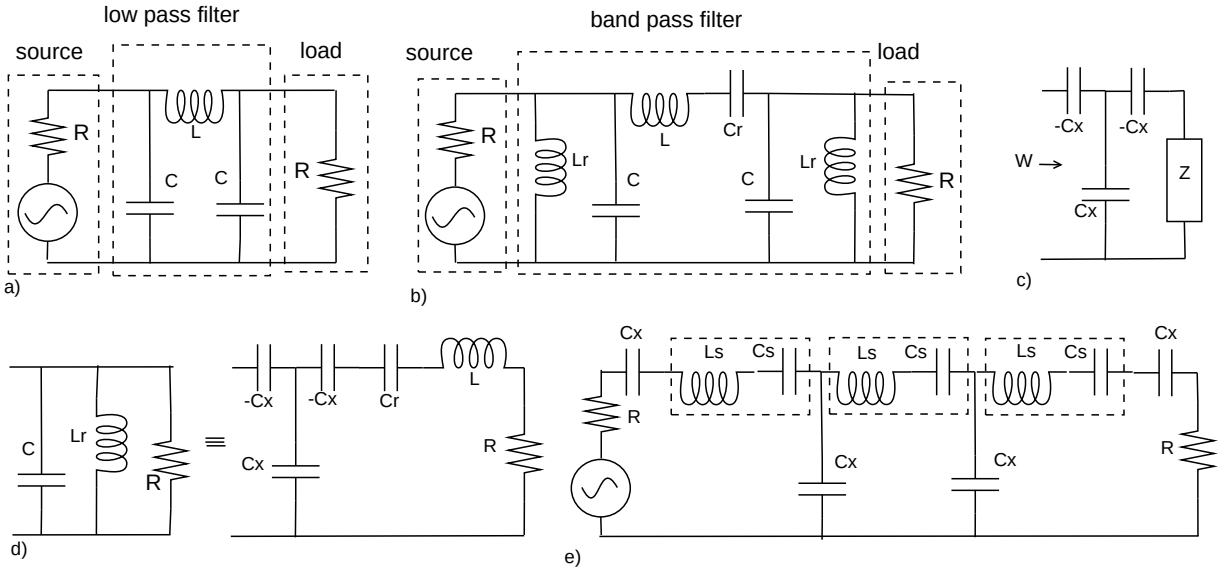

Figure 21: Conversion of a Butterworth band pass filter.

We will now see how the above rearrangement of a bandpass filter can be used to produce what is known as a crystal ladder filter. A Crystal can be described by the model in Figure 21a. However, around resonance, this can simply be approximated by the inductance L_s in series with the capacitance C_s. As a consequences, we can replace the series resonators in Figure 20e by crystal resonators, i.e. the filter in Figure 21b. However, it will be noted that L_s and C_s are not under the designers control and L_s has a typical value of about 10mH for a crystal with resonant frequency $f_c = 10$MHz. From the design of the filter in Figure 20b, we have that $L = R/\pi B$ and so there is a direct relation between bandwidth and terminating impedance. For a filter with bandwidth around 10KHz, this will mean terminating impedances of the order of about 316Ω and a value of 50pF for C_X. It is possible to replace the series capacitors by shunt capacitances, but in this case the capacitance must be halved and the terminating resistances doubled (note that $C_X = 1/\omega_c R$ around resonance).

Exercise

Find out the changes that will need to be made if the bandpass crystal filter is to be based on a Chebyshev filter with 1dB ripple in the pass band ($L = 0.994R/\omega_B$ and $C = 2.024/R\omega_B$).

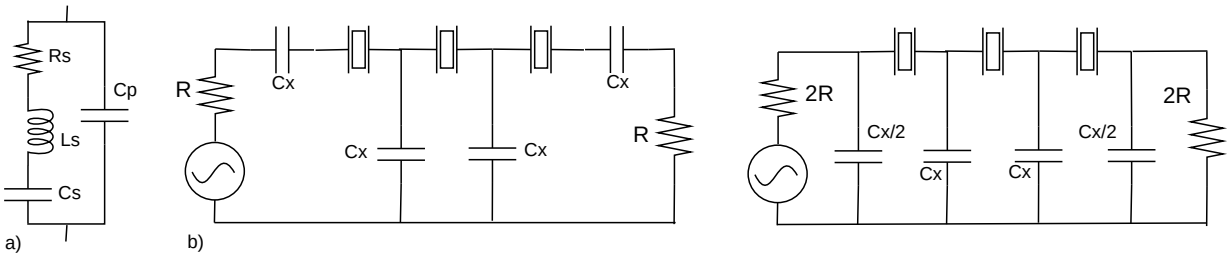

Figure 22: Crystal ladder filters.

Designing a Power Amplifier

We will consider the design of a class C BJT power amplifier. In class C amplifiers, the conduction angle is less than 180° and this is usually achieved by either no bias or a reverse bias. As a consequence, the waveform will be highly distorted, i.e. there is no possibility of regenerating the original waveform. However, class C amplifiers can be very efficient and can be very useful for angle modulation (phase and frequency modulation). The design procedure is as follows :

1) For given supply voltage V_{CC}, and the output power P_{RF}, choose load according to $R_L = \frac{V_{CC}^2}{2P_o}$ in order to ensure that the transistor can make the maximum possible voltage swing. (To make full use of expensive power transistor capacity, we tend to design power amplifiers for maximum swing rather than optimum power transfer.) If this impedance does not match the desired load (R'_L), we can transform it using a suitable matching network.

2) Choose a transistor that can handle a maximum voltage, i.e. $2V_{CC}$, the maximum current and the maximum power dissipation.

3) The transistor should be biased for the required conduction angle (less than 180°). Unfortunately, the major constraint on class C amplifiers is the current carrying capacity of the transistor and the required conduction angle might not be possible. Since the the maximum current increases as the conduction angle falls, we normally design for the minimum conduction angle that is consistent with the current capacity of the transistor.

Consider an SD1143 bipolar device, a transistor that has a gain of 10dB. We will design a class C amplifier that provides approximately 5.0 watts into a 50Ω load from a 50Ω source at a frequency of 220MHz and uses an 12 volt power supply. The input impedance of this device is approximately $1.3 + 2j\Omega$ at 220MHz (i.e. the input exhibits some inductance) and the output impedance is approximately $8.5 - 2.5j\Omega$ (i.e. the output exhibits some capacitance). For maximum swing (a maximum RF voltage amplitude of V_{CC}),

$$R_L = \frac{V_{CC}^2}{2P_{RF}} = \frac{12^2}{2 \times 5} = 14.4\Omega$$

We require an output network that transforms the 50Ω of the specified load into 14.4Ω and, at the input, we will require a network that transforms the transistor input impedance $1.3 + 2.j\Omega$ into the 50Ω of the source. The total circuit is shown in Figure 23. (Note that the blocking capacitors that isolate transistor biases from external circuits.)

We need to check that the dissipation and maximum current are within the limits of

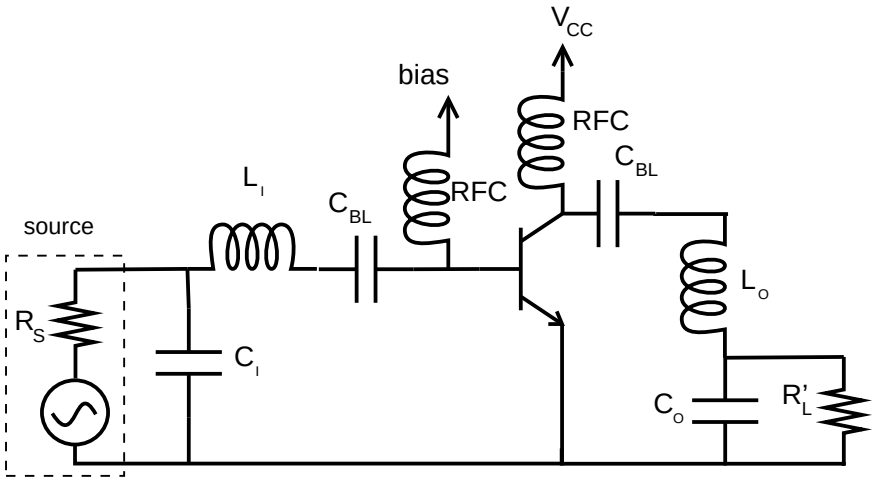

Figure 23: Power amplifier example.

the transistor. At maximum voltage swing, the maximum current is given by

$$I_{max} = \frac{2\pi V_{CC}(1-\cos\theta)}{R_L(2\theta - \sin 2\theta)} \tag{26}$$

the power dissipation by

$$P_D = P_{DC} - P_{RF} = P_{RF}(\frac{4(\sin\theta - \theta\cos\theta)}{2\theta - \sin 2\theta} - 1) \tag{27}$$

and the efficiency by

$$\text{efficiency} = \frac{P_{RF}}{P_{DC}} = \frac{2\theta - \sin 2\theta}{4(\sin\theta - \theta\cos\theta)} \tag{28}$$

where 2θ is the conduction angle (see chapter 5). The maximum current that an SD1143 can handle is 2.0A and this will limit the values of θ to satisfy

$$\frac{2\pi \times 8}{16}\frac{1-\cos\theta}{2\theta - \sin 2\theta} < 2.0 \tag{29}$$

This condition is satisfied if $\theta > 66°$. At this conduction angle, a power $P_D = .7W$ is dissipated in the transistor, well within the capacity of the transistor (37W). The maximum possible efficiency will be 87.7%.

The output network transforms a 50Ω load into the 14.4Ω that is required for maximum swing. The network reactances are calculated from the design formulas of chapter 3. At the transistor output

$$X_{C_O} = -\frac{R_L}{Q} \quad \text{and} \quad X_{L_O} = -\frac{X_{C_O}Q^2}{Q^2+1} \tag{30}$$

where $Q = \sqrt{R'_L/R_L - 1}$. We will have $Q = 1.57$ from which $X_{C_O} = -31.8\Omega$ and $X_{L_O} = 22.6\Omega$. The output reactance of the transistor will form part of X_{L_O} and so we need to use an effective reactance $X'_{L_O} = 22.6 + 2.5 = 25.1\Omega$ when calculating L_O. Since $\omega = 2\pi \times 2.2 \times 10^8$rad/sec and $\omega L_O = 20.1$, $L_O = 18.2$nH. Further, since $X'_{C_O} = \frac{-1}{\omega C_O}$, $C_O = 23$pF.

At the input, ignoring the reactance of the transistor,

$$X_{C_I} = -\frac{R_S}{Q} \quad \text{and} \quad X_{L_I} = -\frac{X_{C_I} Q^2}{Q^2 + 1} \tag{31}$$

where $Q = \sqrt{R'_S/R_T - 1}$ and R_T is the input resistance of the transistor. We need to transform the resistance of the source ($R_S = 50\Omega$) into $R_T = 2.2$. From the above network design formulas, we find that $Q = 4.66$ and from which $X_{C_I} = -10.73\Omega$ and $X_{L_I} = 10.26\Omega$. The input reactance will form part of X_{L_I} and so we will use an effective value of $X'_{L_I} = 8.46\Omega$. The final values for the input network components will then be $C_I = 67$pF and $L_I = 6.1$nH.

A class C amplifier will only be useful for amplifying angle modulated signals and we will need to go to at least class B ($\theta = 90°$) operation if we are to retain amplitude data. In studying power amplifiers, we have assumed a linear transistor characteristic and that the transistor switches on as soon as the base voltage becomes positive. The reality is that there will need to be a small positive bias at the base if the transistor is to switch on for all positive swings of the input voltage. An amplifier with such a bias is often known as a *class AB* amplifier. A simple means of achieving this bias is shown in Figure 24. The diode *mirrors* the behaviour of the emitter-base junction and generates a bias voltage so that the transistor is just into conduction. An advantage of such a bias system is that the diode itself can be placed next to the transistor body and respond to the transistor if it overheats. The heating will increase the current flow through the diode and this, in turn, will cause a voltage drop at the base and hence a reduction in current through the transistor. Such a thermal feedback mechanism is important since power transistors are prone to thermal runaway. A further problem for signals with amplitude data is that full swing at the output will require the collector voltage to become zero at some point in a cycle. However, it will be noted that the transistor characteristics become highly nonlinear close to zero voltage and this will severely diminish the quality of the amplitude data. To combat this, the maximum amplitude at the output of a class AB amplifier is often limited to slightly below V_{CC}.

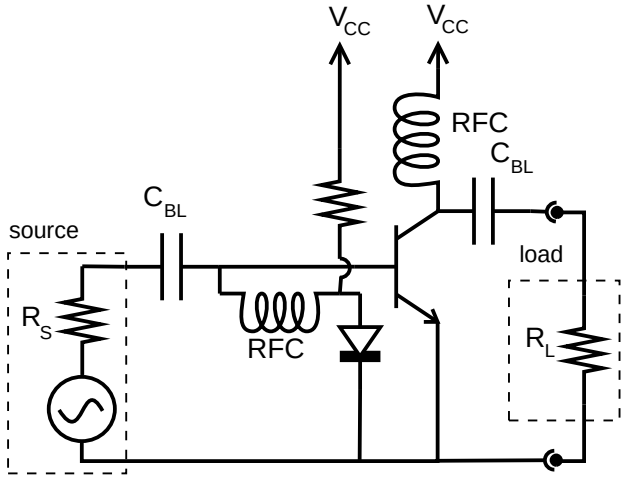

Figure 24: Bias for class AB operation.

Exercise

Redesign the above class C amplifier for a frequency of 150MHz. At this frequency the transistor input impedance is $1.5 - j0.9\Omega$ and output impedance is $5.2 + j0.4\Omega$.

A Class E Amplifier

In theory, the class D amplifier achieves high efficiency by acting as an ideal switch. In the ideal case, the drain voltage is zero when the transistor is on, i.e. current flows, and the supply voltage when the transistor is off, i.e. no current flows. As a consequence there will be no dissipation (IV is always zero) and hence 100% efficiency. However,

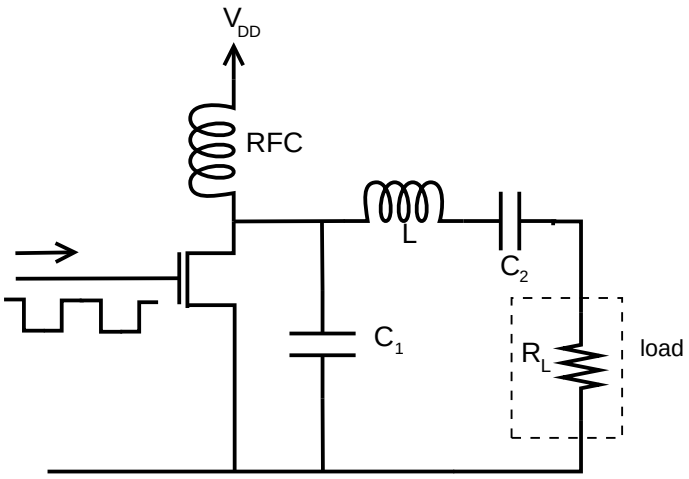

Figure 25: Class E amplifier.

the transition between conduction and non conduction will not be instantaneous and there will be some dissipation during the transition. In the transition to an off state, the dissipation can be reduced by means of a shunt capacitance C_1 across the FET output (the parasitic capacitance at the output is often sufficient). This will then slow down the rise of the drain voltage while there is still current flow. In the transition to an on state, the dissipation is reduced by choosing the resonant frequency of L and C_2 to be just below the drive frequency. At the drive frequency there will be a phase shift between the voltage and current that causes the voltage to tail off to zero before there is significant current flow in the transistor. A class D amplifier with the above modifications is commonly known as a class E amplifier. It can be shown (see N.O.Sokal and A.D.Sokal, IEEE Journal of Solid-state Circuits, SC-10, N0.3, pp. 168-176, 1975) that the appropriate values of C_1, C_2 and L can be calculated according to

$$C_1 \approx \frac{1}{5.447\omega R_L}, \quad L = \frac{QR_L}{\omega}$$

$$\text{and} \quad C_2 \approx C_1 \frac{5.447}{Q}(1 + \frac{1.42}{Q - 2.08})$$

where $R_L = 0.577\frac{V_{DD}}{P_o}$, P_o is the desired output power and Q is calculated from the desired bandwidth B ($Q = \omega_0/B$ where ω_0 is the desired operating frequency). R_L will

not necessarily be equal to the desired load and so it is possible that matching, possibly an L network, will be required to match the desired load. Unfortunately, the above formulas do not take into account the fact that a real inductor will also have some resistance $r_p = Q_U \omega_0 L$ where Q_U is the unloaded Q of the inductor. This resistance will be in series with the load and so the load resistance will need to be adjusted if r_p is significant in comparison with R_L (see N.O.Sokal, ARRL QEX magazine, Jan/Feb, 2001).

Exercise

Design a class E amplifier to produce 10W of output power at a frequency of 10MHz, with a bandwidth of 3kHz and a drain voltage of 10V. Design an L network that allows this amplifier to feed a 50Ω load whilst reducing the harmonic content.

Receiver Performance Calculations

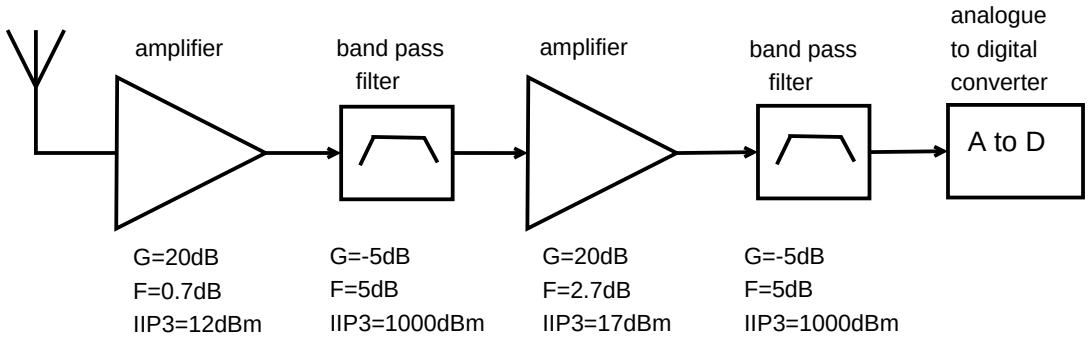

Figure 26: Direct digitising software radio.

For frequencies below about 60MHz, there are now readily available A to D converters that can directly digitise the RF and, as a consequence, all of the receiver functions can be performed digitally. According to the Nyquist sampling theorem, this will require sampling at a rate of 120MHz. Further, the ADC must be preceded by a filter that will remove frequencies above 60MHz so that they cannot alias into the desired frequency range. It is possible, however, to use the phenomenon of aliasing to digitise signals at higher frequencies through undersampling. If f_S is the sampling rate of the ADC we can digitise any bandwidth $B = f_s/2$ by filtering out all signals outside this bandwidth. Then, as long as the sample and hold of the ADC has sufficiently fast response, this band will be moved down in frequency by a multiple of the sample rate.

The key to the success of the undersampling approach is to have suitable bandpass filtering and suitable amplification to bring the signals up to a level that is compatible with the A to D converter. Figure 26 shows such a system with typical for the relevant key performance parameters of gain, noise figure and intercept point (all given in logarithmic scales). Since the first amplifier affects noise the most, this has a very low noise figure (the performance figures are approximately those of a low noise E-PHEMT transistor amplifier such as the Mini-Circuits PSA4-5043). The second amplifier, however, has a

higher intercept point, but larger noise figure (the performance figures are approximately those of a Mini-Circuits GAL74). Finally, the filters have a fairly high loss which is a hallmark of the high order filters that are required for strong out of band rejection (the performance figures are approximately those of a Temwell four chamber helical filter). (Note that for passive devices, such as filters, the noise figure is equal to the device loss.)

We now calculate the performance figures of the total system that feeds into the ADC. The total gain is obtained by adding the gains and so is $30dB$. For a 2 device system the total noise factor is

$$\mathrm{F} = F_1 + \frac{F_2 - 1}{G_1} \tag{32}$$

where F1 and F2 are the noise factors for the 1st and second devices. By repeated application, we obtain

$$\mathrm{F} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} \tag{33}$$

for a four device system. For a two device system the total $IIP3$ is given by

$$\frac{1}{IIP3} = \frac{1}{IIP3_1} + \frac{G_1}{IIP3_2} \tag{34}$$

and, by repeated application,

$$\frac{1}{IIP3} = \frac{1}{IIP3_1} + \frac{G_1}{IIP3_2} + \frac{G_1 G_2}{IIP3_3} + \frac{G_1 G_2 G_3}{IIP3_4} \tag{35}$$

for a four device system. It will be noted that linearity requirement on the later devices needs to be more stringent, hence the use of a GALI74 as the second amplifier. In general, the early devices need to have good noise performance and the later devices need to have good linearity performance.

Labelling the devices 1 to 4 from the left, we will have $G_1 = 100$, $G_2 = 0.316$, $G_3 = 100$, $G_4 = 0.316$, $F_1 = 1.175$, $F_2 = 3.162$, $F_3 = 1.862$, $F_4 = 3.162$, $IIP1 = 15.85mW$, $IIP2 = 1W$, $IIP3 = 50.12mW$ and $IIP4 = 1W$. From these numbers, we obtain that $F = 1.225$ (i.e. 0.88dB) and $IIP3 = 1.377mW$ (i.e. $IIP3 = 1.389dBm$).

We now ask how the performance figures, i.e. G,F and $IIP3$, relate to the actual performance of the radio. The noise floor N_f is the most important measure of performance as it tells us the actual level of signal below which the signal is hidden amongst the noise. In terms of noise factor,

$$N_f = F = kT_A B + (F - 1)kTB \tag{36}$$

where T_A is the antenna temperature, B is the bandwidth and T is the ambient temperature (taken to be $290K$). The next important figure is the SFDR (spurious free dynamic range) as this tells us the range of input powers over which the spurious signals caused by nonlinearities remain hidden in the noise. In terms of N_f and $IIP3$,

$$\mathrm{SFDR} = \left(\frac{IIP3}{N_f}\right)^{2/3} \tag{37}$$

We first assume an antenna temperature of $10000k$ and a bandwidth $B = 1MHz$. Then, $N_f = 2.28 \times 10^{-15}W$ and $SFDR = 7.15 \times 10^7$ or $78.5dB$. The dynamic range is compatible with that of a typical 14 bit ADC. However, it should be noted that the level of amplification before the ADC needs to be controlled in order to prevent the largest signals being *clipped* at the maximum level of the ADC. If the signal environment is dynamic, this usually requires AGC (automatic gain control). The system will monitor the maximum signal level and feed this back to control a variable gain amplifier.

Exercise

What will be the effect upon performance of interchanging the amplifiers.

The Tayloe Mixer

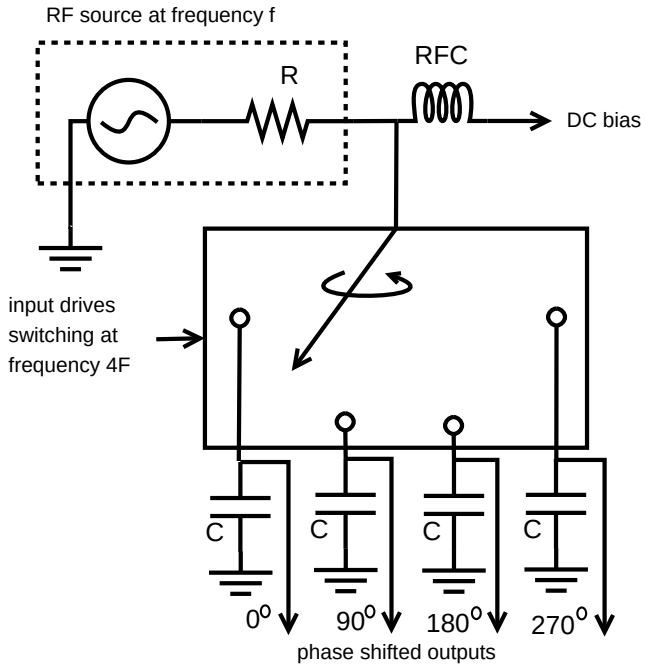

Figure 27: Basic Tayloe mixer and its operation.

The advent of high speed digital devices has introduced many possibilities for RF electronics. One possibility is the use of high speed digital switches for mixing. As we have seen in chapter 5, we can achieve the mixing function by treating transistors as switches. Figure 27 shows a more sophisticated switching mixer circuit that is known as a Tayloe mixer after its designer (Dan Tayloe, Letters to the editor in ARRL QEX magazine, March/April, 2001). The mixer switches the RF input sequentially between four outputs, the switch being triggered at a frequency of $4F$ where F is the centre frequency of the band of interest. Consequently, each output will only sample the input signal for a quarter of a period of the centre frequency. For output N, the output signal

will be given by the

$$s_N = s_{RF} H(2\pi F t - (N-2)\pi/2) \tag{38}$$

where s_{RF} is the input RF signal. H is a periodic function (repeats itself every 2π) with

$$\begin{aligned} H(\theta) &= 0 \quad 0 < \theta < \frac{3\pi}{4} \\ &= 1 \quad \frac{3\pi}{4} < \theta < \frac{5\pi}{4} \\ &= 0 \quad \frac{5\pi}{4} < \theta < 2\pi \end{aligned} \tag{39}$$

It is clear that $H(2\pi F t - (N-2)\pi/2)$ is non zero for a quarter of a period, which quarter depending on the value of N. We can be expand $H(\theta)$ in Fourier series as

$$H(\theta) = \frac{1}{4} - \frac{2}{\pi}\left(\frac{1}{\sqrt{2}}\cos(\theta) - \frac{1}{2}\cos(2\theta) + \frac{1}{3\sqrt{2}}\cos(3\theta) - ...\right) \tag{40}$$

Assuming a sinusoidal RF source, i.e. $s_{RF} = s_0 \cos(\omega t)$ where $\omega = 2\pi f$, we obtain that

$$\begin{aligned} s_N &= \frac{1}{4}s_0\cos(\omega t) - \frac{s_0}{\sqrt{2}\pi}\left(\cos(\Omega t - (N-2)\pi/2 - \omega t) + \cos(\Omega t - (N-2)\pi/2 + \omega t)\right) \\ &\quad + \frac{s_0}{2\pi}\left(\cos(2\Omega t - (N-2)\pi - \omega t) + \cos(2\Omega t - (N-2)\pi + \omega t)\right) + ... \end{aligned} \tag{41}$$

where $\Omega = 2\pi F$. The capacitors in the circuit will filter out all the higher frequency terms and so we will be left with

$$s_N \approx + \frac{s_0}{\pi\sqrt{2}}\cos((\Omega - \omega)t - N\pi/2) \tag{42}$$

i.e. the output a port N is the baseband signal with phase phase shift $N\pi/2$.

The switch in the Tayloe mixer can be realised using a high speed digital multiplexer circuit, or MUX as it is known. A MUX is a device that switches an input between different outputs according to the value of a digital control input. Figure 28 shows a practical circuit of a Tayloe mixer (G.Youngblood, ARRL QEX magazine, Jul/Aug, 2002) that uses a 4:1 MUX. The position of the switch in the 4:1 MUX is controlled by a 2 bit binary number, the inputs A and B representing the bits of this number. Input clock pulses at frequency $4F$ are converted to control signals through a device that counts the input pulses (those at frequency $4F$) in binary (00, 01, 10, 11, etc). However, since the counter is only 2 bit, after its output reaches the binary value 11 it goes back to 00, i.e. it counts modulo 4. This will cause the MUX to cycle round round its outputs in the desired manner. The counter in Figure 28 is known as a *Johnson counter* and achieves its purpose through a pair of D flip-flops (these are contained within a single 74AC74 integrated circuit). A single D flip-flop has a single input D and two outputs Q and $\overline{Q}$ ($\overline{Q}$ being the logical conjugate of Q). The value of Q then becomes that of D at the rising edge of a clock pulse.

Since each channel of the switch is only on for a quarter of a cycle, the effective source resistance is $4R$. Consequently, the capacitance C will filter each channel with with bandwidth $1/4\pi RC$. The outputs with 0° and 180° phase shifts are combined differentially

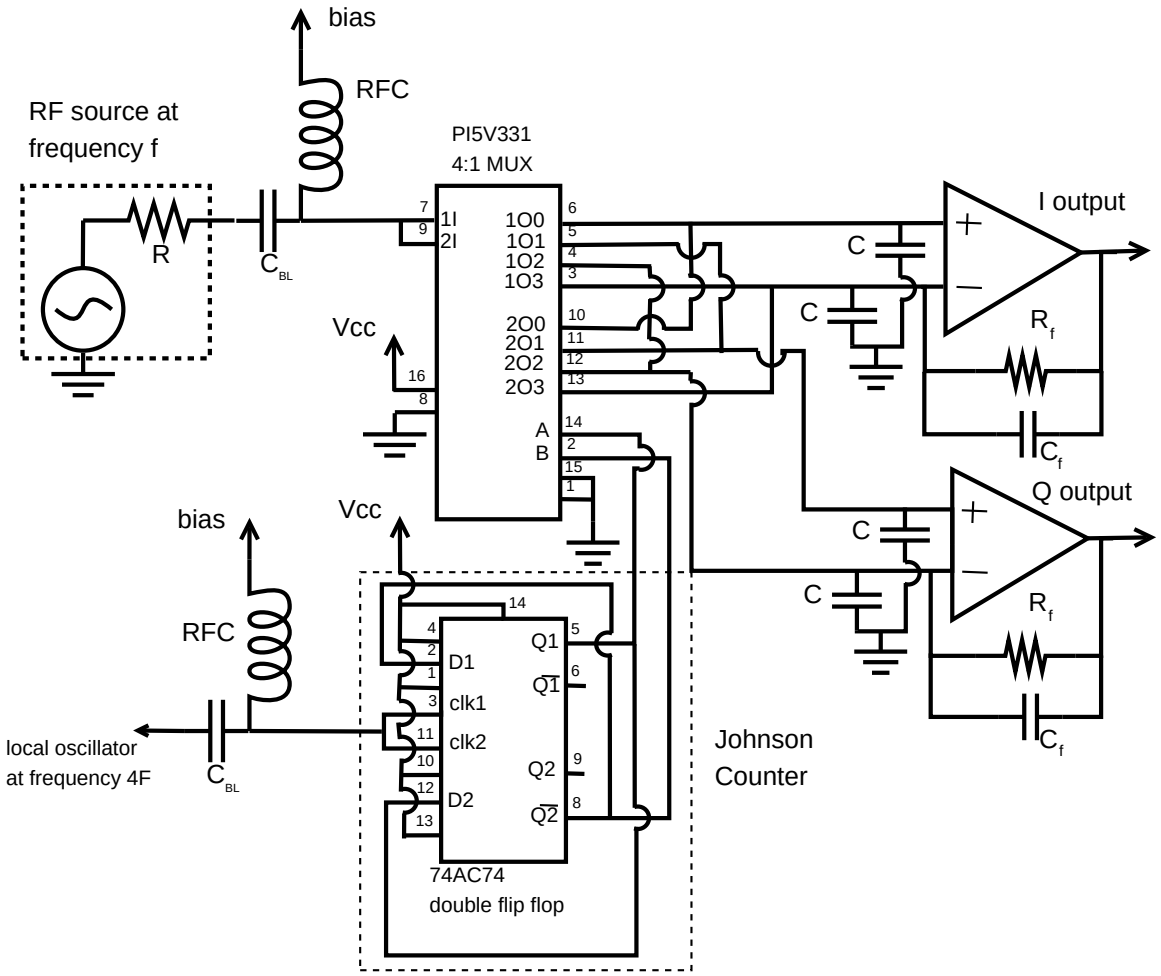

Figure 28: Practical receiver based on a single balanced Tayloe mixer.

to give the in phase output (I) and the outputs with 90° and 270° phase shifts combined differentially to give the quadrature output (Q). This combination occurs through operation amplifiers that will also amplify these signals. The voltage gain of each amplifier is given by $A = R_f/4R$ where R_f is the feedback resistance. A feedback capacitor C_f can be added in order to improve the removal of the high frequency components mentioned above. The simplest software radio receivers feed the I and Q outputs into the stereo microphone inputs of a computer where they are digitised and can then be processed in the manner described in chapter 6.

In the IC of Figure 28 there are two MUX switches, but these are configured in parallel. However, these two switches can be separated and reconfigured to form a mixer of the double balanced variety. Figure 29 shows the receiver with the mixer reconfigured. The two MUX are fed anti-phase from a balun and the outputs are combined anti-phase. The result is that the non product are cancelled and, as a consequence, the output filtering requirements severely reduced. The Tayloe mixer can also be used in the generation of signals and Figure 29 shows the generation process (note that a circle at the end of the input amplifiers represents a 180° phase shift). In this design, the the I and Q signals will be computer generated (possibly at the stereo outputs of a computer) and the output will be fed through a bandpass filter in order to remove any unwanted mixer products.

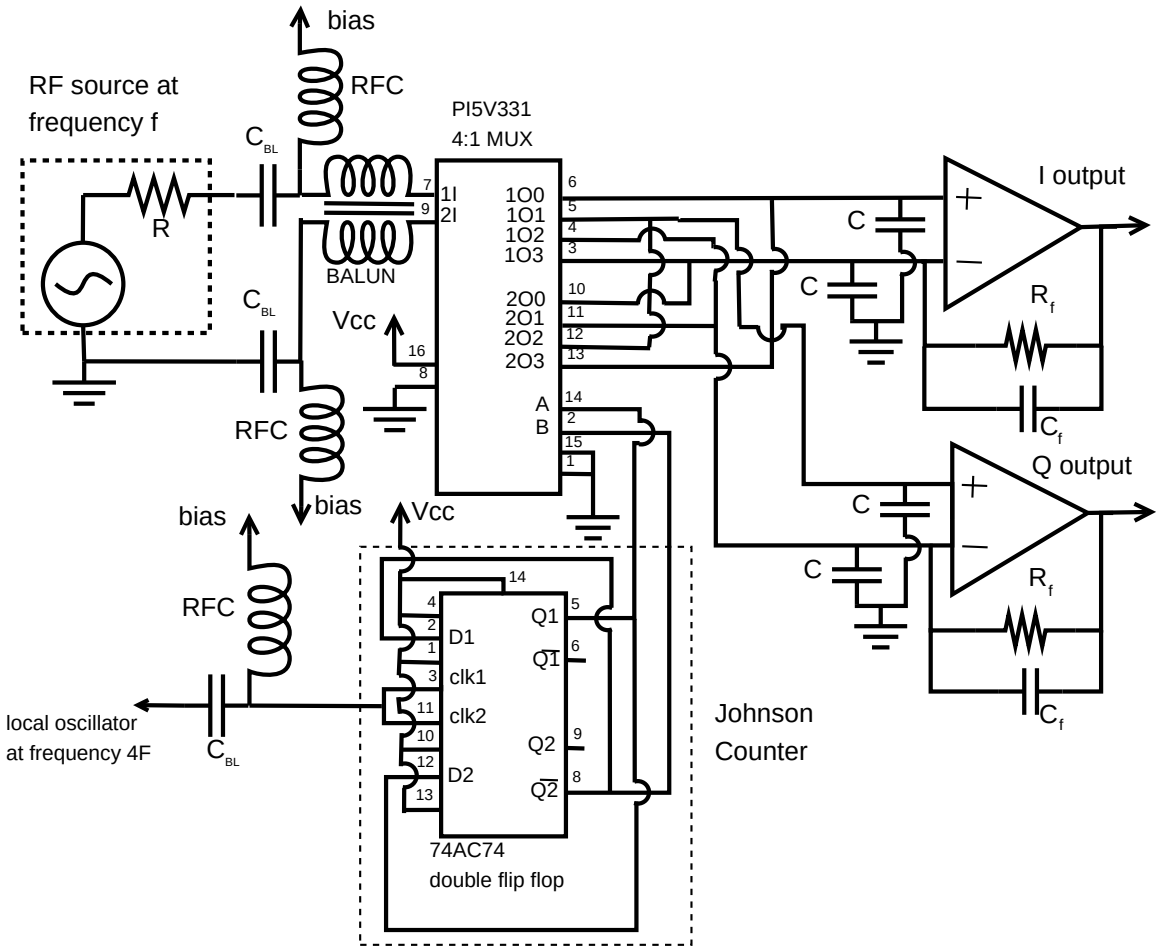

Figure 29: Practical receiver based on a double balanced Tayloe mixer.

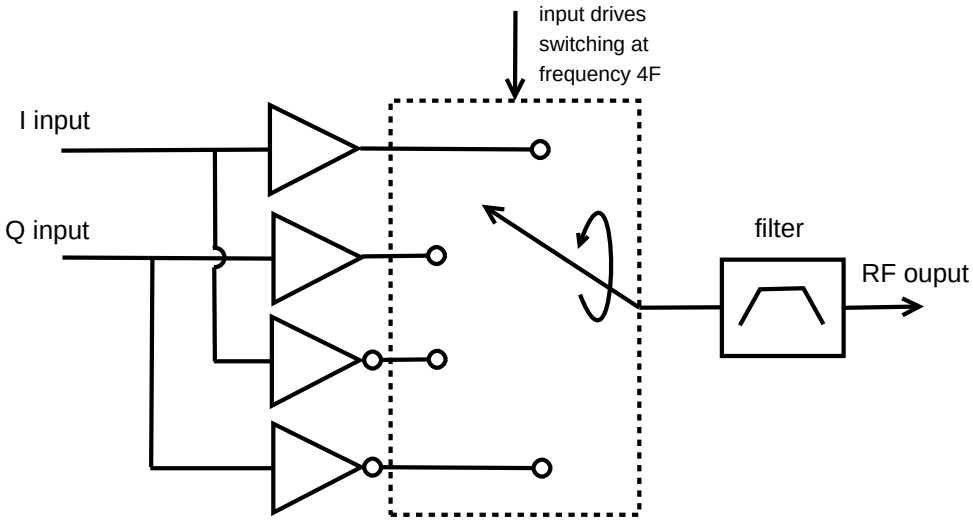

Figure 30: Signal generation using a Tayloe mixer.

Stabilising Oscillators

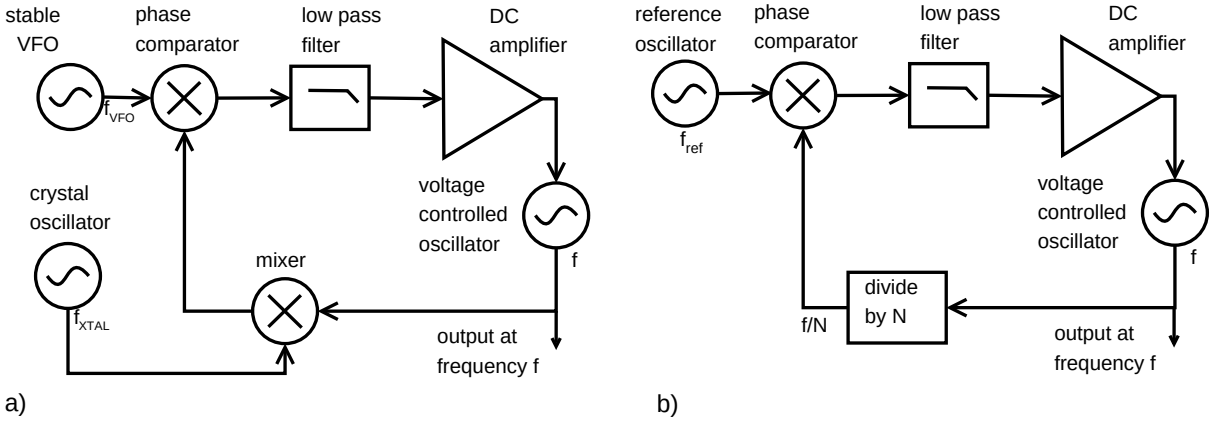

Figure 31: Frequency generation using phase locked loop stabilisation.

In chapter 5 we have seen that phase locked loops can used to provide a means of stabilising free running oscillators (see Figure 31). The key to such loops is an effective means of phase comparison. In chapter 5 we considered a simple mixer as a phase comparator, but digital electronics has opened up other possibilities for phase comparators. Figure 33 shows an example of a comparator based on a D flip flop together with a NAND gate. The running average of the output is a measure of the difference between the VCO and reference signal phases and provides a simple, but effective, phase comparator.

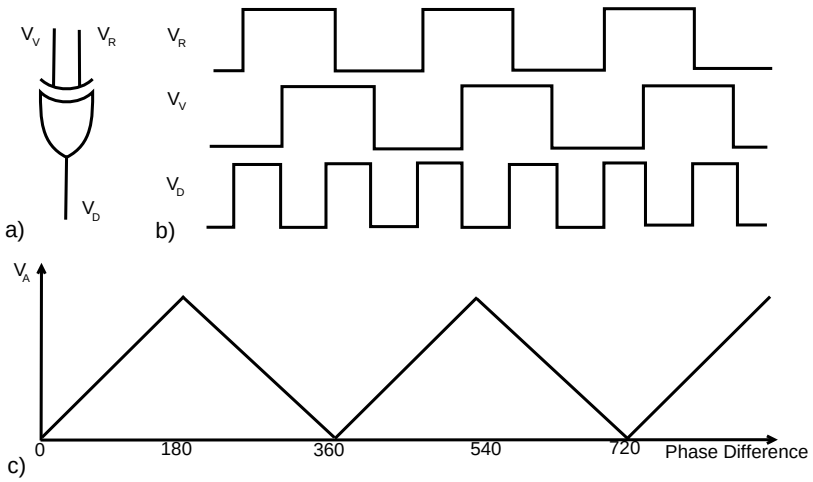

Figure 32: XOR gate as a digital phase comparator.

The phase comparator allows a free running oscillator to be locked onto a stable reference. However, as mentioned in chapter 5, there can be a problem in initially achieving lock, i.e. initially guiding the reference and VCO signals onto the same frequencies. This problem can be overcome by a device that can compare the frequencies of the reference and VCO signals. If the frequencies are different, this device will generate a voltage that makes the VCO move closer to the reference in frequency. Such a frequency comparator is easily created using digital electronics and Figure 33 shows a particular example.

This circuit also has the advantage that, for signals with the same frequency, its output is a voltage that is proportional to their pase difference. Such a circuit is known as a phase/frequency comparator. Frequency coincident oscillators are kept in frequency lock by the phase comparator aspect of the circuit. The circuit consists of two edge triggered D flip flops. However, at the output there is NAND gate that resets both of the flip flops when their Q outputs are logic 1. As a consequence, the output of either flip flop is only triggered to logic level 1 when the outputs of both flip flops are at different logic levels. Figure 33 also shows the effect of the reference signal when compared with two different VCO frequencies. I will be noted that the average of the output, i.e. the output after low pass filtering by the capacitor, is less for the VCO signal at the higher frequency. It this voltage the guides the VCO onto the reference signal.

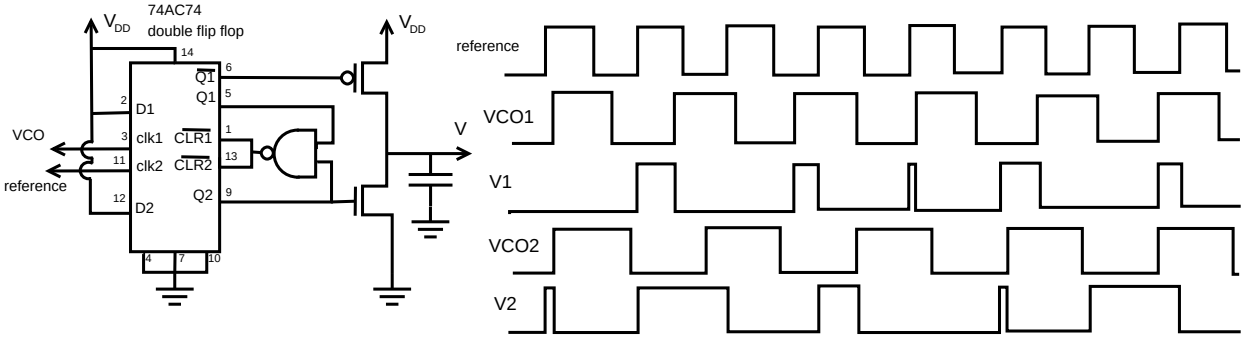

Figure 33: Phase/frequency comparator.

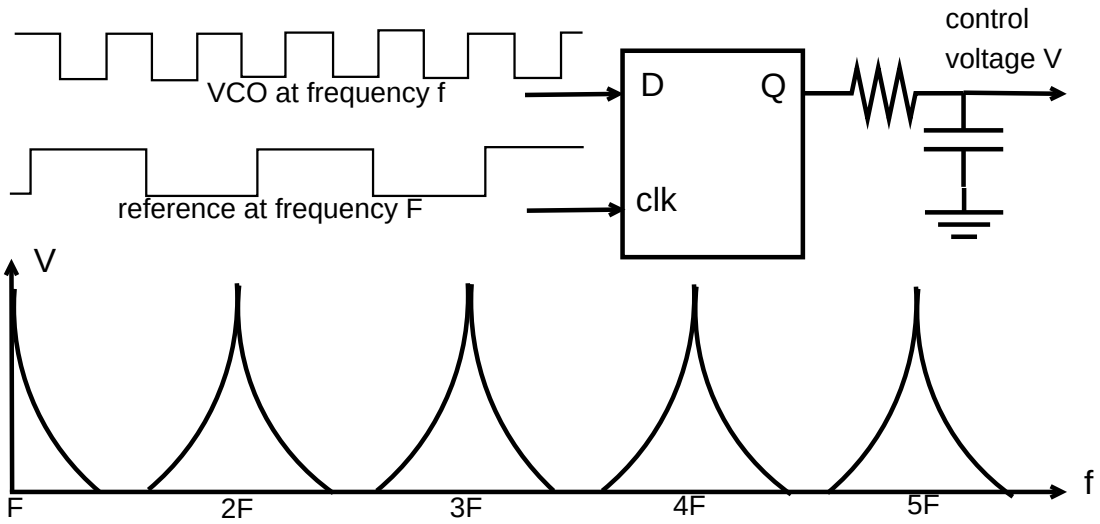

Figure 34: The HUFF-PUFF frequency stabiliser based on a type D flip flop.

An ingenious method of stabilising a free running VCO is known as HUFF-PUFF and was invented by Klaus Spaargaren (see Technical Topics in Radio Communication, July, 1973). The key to this approach is the circuit shown in Figure 34. By means of a D type flip flop that is triggered on the leading edge of the clock pulse, the output of a VFO running at frequency f is compared with the output of stable fixed clock running at frequency F. After low pass filtering (the result of the capacitor on the output) the output

voltage V will vary with oscillator frequency as shown in Figure 34. Consider the circuit of Figure 35. If the VFO frequency is just below the harmonic NF of the clock, and its frequency f is drifting upwards, the output voltage V will rise with the drift and further enhance the drift towards frequency NF. However, if the frequency f is just above NF, upwards drift in f will cause the voltage V to fall and hence push the frequency f back to NF. In this fashion, the feedback in the circuit will stabilise the VCO. It will be noted that there is an countable infinity of frequencies at which the oscillator could be stable, separated by the frequency of the clock. However, in reality, the number of frequencies at which the oscillator can be stable will be dictated by the capacitance range of the diode. If the VFO is tuned to a new frequency, using the variable capacitor, the VFO will settle into the closest multiple of frequency F and then be locked onto that frequency until the VFO is retuned.

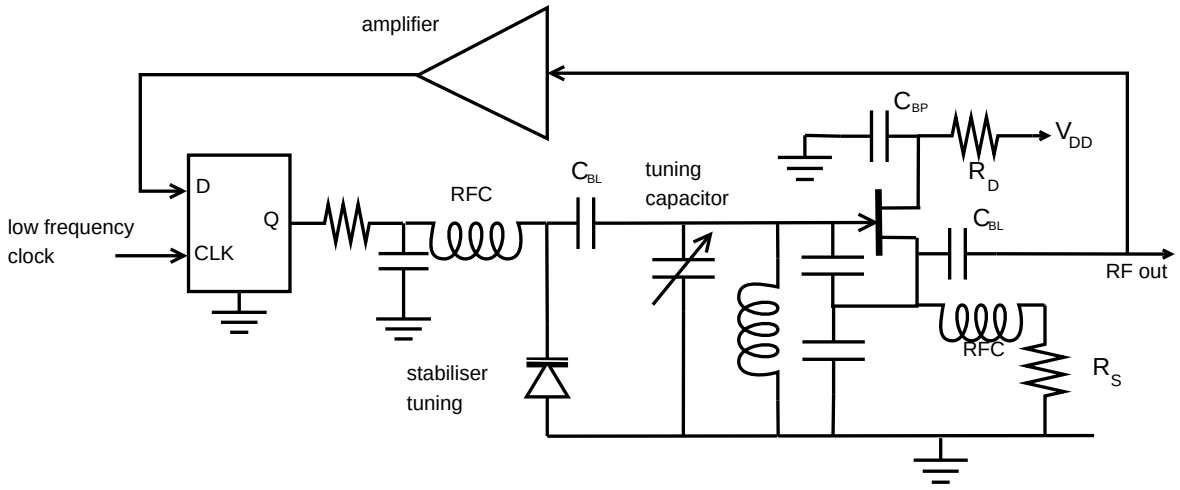

Figure 35: A HUFF-PUFF stabilised VFO.

An increasingly popular method for providing stable signals is known as direct digital synthesis (DDS). In a DDS system, a highly detailed waveform is stored in memory as a long sequence of waveform samples. On each tick of the clock, the address accumulator moves on by a preassigned number N and this address is fed into the waveform sample memory from where the associated wave sample is fed to a DAC (digital to analogue converter). The DAC output will be the stored waveform (albeit as a highly refined step function representation) with frequency proportional to N. The analogue output is then low passed filtered at the highest frequency required in order to provide a smooth waveform. It is clear that the stability of the signal will depend on the stability of the clock and so a great deal of care needs to be invested in this aspect (a GPS disciplined clock is often used in the most demanding cases).

The Design of Microstrip Transmission Lines

Complex microwave circuits can be built on double sided printed circuit board (copper on both sides of the substrate). The copper on one side of the board will remain continuous (the ground plane) and the circuit will be built up on the other side. The basic building

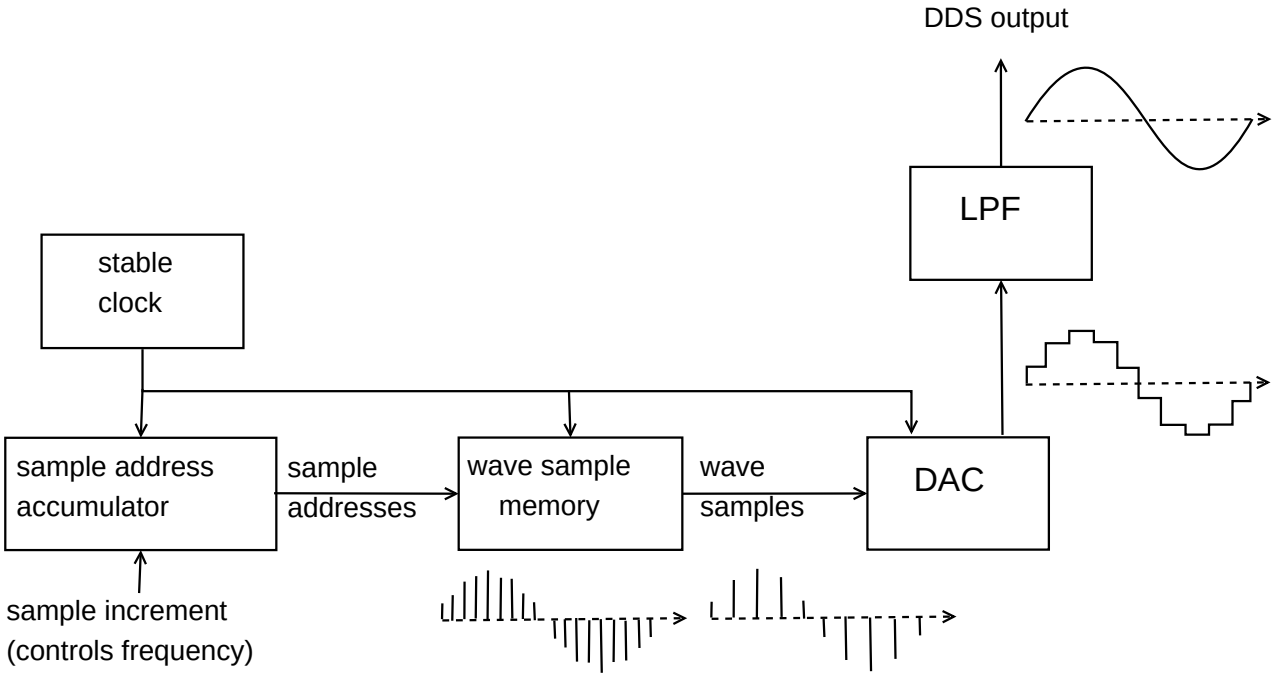

Figure 36: The architecture of a direct digital synthesiser.

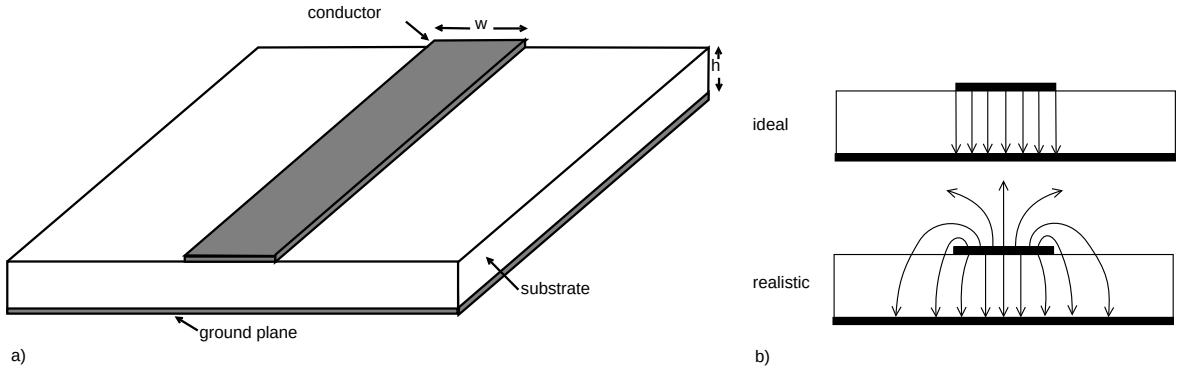

Figure 37: A microstrip transmission line.

block in such a circuit is the microstrip transmission line (see Figure 37a) For a microstrip transmission line with characteristic impedance Z_0, $w/h \approx Z_0/\eta$ where η is the impedance of the substrate. However, this assumes that the substrate thickness is small in comparison to the microstrip width, i.e. the electric field can be approximated as shown in the top panel of Figure 37b. In reality, due to edge effects, the fields will be more like those shown in the bottom panel of Figure 37b. A more accurate expression is

$$\frac{w}{h} = \frac{8}{A}\sqrt{\frac{7\epsilon_r + 4}{11\epsilon_r}A + \frac{\epsilon_r + 1}{0.81\epsilon_r}} \tag{43}$$

where

$$A = \exp\left(\left(\frac{Z_0}{42.4}\right)\sqrt{\epsilon_r + 1}\right) - 1 \tag{44}$$

and ϵ_r is the relative permittivity of the substrate. It will be noted that the wave speed on a transmission line is less than that in free space, i.e. $c = c_0/\sqrt{\epsilon_{\text{eff}}}$ where c_0 is the wave

speed in free space (i.e. $3 \times 10^8 m/s$) and $\epsilon_{\text{eff}} \approx (\epsilon_r + 1)/2 + ((\epsilon_r - 1)/2)/\sqrt{1 + 12h/w}$ is the effective relative permittivity of the substrate under the microstrip. If λ_0 the wavelength at a given frequency in free space, the wavelength on the transmission line for that frequency is $\lambda = \lambda_0/\sqrt{\epsilon_{\text{eff}}}$.

We will design a microstrip transmission line with characteristic impedance 50Ω for a 1.56mm thick substrate with $\epsilon_r = 4.4$. From the above expressions $A = 14.492$ and then $w/h = 1.9071$, i.e. $w = 2.975mm$. Now consider a frequency of 900Mz and for which the wavelength in free space will be $\lambda_0 = 333.3mm$. For the above transmission line, $\epsilon_{\text{eff}} = 3.33$ and so the physical wavelength on the transmission line will be $\lambda = 182.6mm$.

Exercise

Design a microstrip transmission line with characteristic impedance 100Ω for a 3mm thick substrate with $\epsilon_r = 4.4$. Calculate the physical length of a wavelength at 900MHz.

A Transmission Line Notch Filter

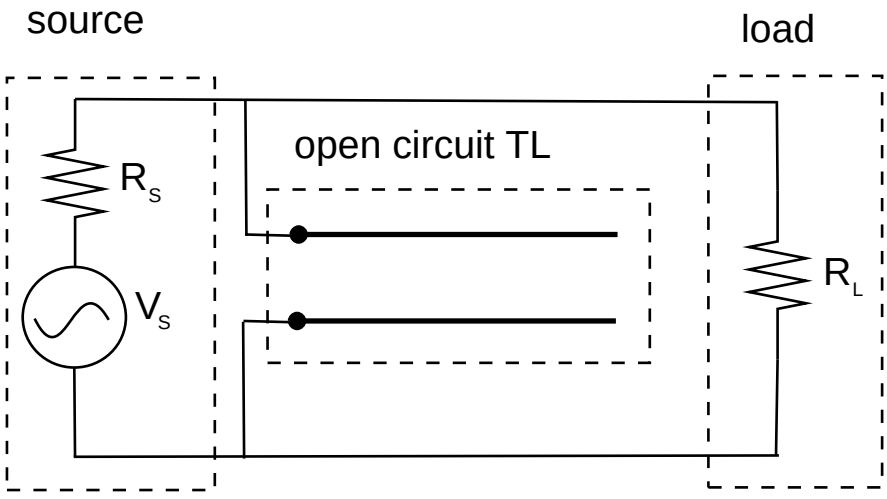

Figure 38: A transmission line notch filter.

An open circuited transmission line behaves like a series resonant circuit with a resonance at a frequency ω_0 for which the line is a quarter wavelength. The impedance of such a resonator is given by $Z = -jZ_0 \cot\left(\frac{\pi}{2}\frac{\omega}{\omega_0}\right)$. If we use the resonator in the configuration shown in Figure 38, the voltage drop across the load resistor is given by

$$V_L = V_S \frac{ZR_L}{R_S Z + R_L Z + R_S R_L} = V_S \frac{R_L}{R_S + R_L} \frac{\cot\left(\frac{\pi}{2}\frac{\omega}{\omega_0}\right)}{\cot\left(\frac{\pi}{2}\frac{\omega}{\omega_0}\right) + j\frac{R_S \| R_L}{Z_0}} \tag{45}$$

As with the shunt series capacitor/inductor combination, this will also act as a notch filter (see example 6) around ω_0. However, as with other transmission line filters, this will also have similar behaviour around frequencies that are harmonically related to ω_0.

Exercise

Plot the insertion gain as a function of frequency for a variety of $Q = \pi R_S \parallel R_L/4Z_0$.

Stub Matching Using Microstrip Transmission Lines

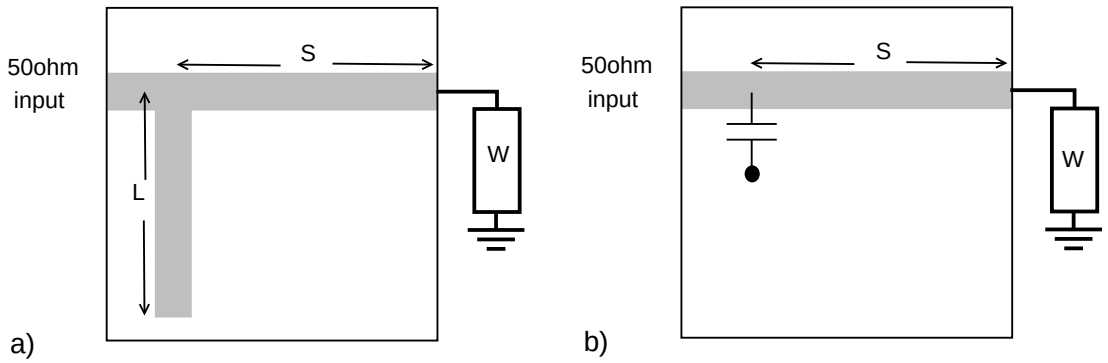

Figure 39: Matching using microstrip transmission lines.

As mentioned in chapter 7, lengths of transmission line, together with stubs, can be used to transform impedances. Figure 39a shows the situation where this approach is used to couple an arbitrary load W into a microstrip transmission line with characteristic impedance $Z_0 = 50\Omega$. We will consider the problem in terms of the admittances $Y = 1/W$ and $Y_0 = 1/Z_0 = .02$. The admittance transforms along the transmission line according to

$$Y_{in} = Y_0 \frac{Y\cos(\beta S) + jY_0 \sin(\beta S)}{Y_0 \cos(\beta S) + jY \sin(\beta S)} \tag{46}$$

For a matching to occur, we need Y_{in} to equal Y_0 and so we first choose the length S such that $\Re\{Y_{in}\} = \Re\{Y_0\}$. Then, if $\Im\{Y_{in}\} \neq 0$, we manufacture a stub reactance X such that

$$\Im\{Y_{in}\} - \frac{1}{X} = 0 \tag{47}$$

(note that the admittances of parallel impedances add). Although we have shown the stub as open circuit, it could equally well be an short circuit stub and it usual to choose the type of stub that has the shortest length. In the case of a shorted stub, the end of the microstrip stub will need to be connected to the ground plane through a suitably large capacitor, i.e. an RF short circuit. In the case that there is no room for the stub, it could be replaced by the equivalent discrete component reactance (see Figure 39b).

We will consider the transformation of the impedance $W = 7 + j5\Omega$ into 50Ω. If we join the load W to the 50Ω microstrip transmission line, then the admittance Y_{in} will vary along the transmission line as shown in Figure 40 (wavelengths are measured as wavelengths on the transmission line). For a 50Ω transmission line, $\Re\{Y_{in}\}$ will be 0.02 at a distance of $S = 0.0405\lambda$ along the transmission line at which point $\Im\{Y_{in}\} = -0.0463$. In order to cancel out the reactance at this point we will need to add a microstrip stub with reactance $X = -1/0.0463 = -21.6\Omega$. The reactance is capacitive and so we will need a open circuit stub with length L that satisfies $X = -Z_0 \cot(2\pi L/\lambda)$, i.e. $L = 0.1851\lambda$.

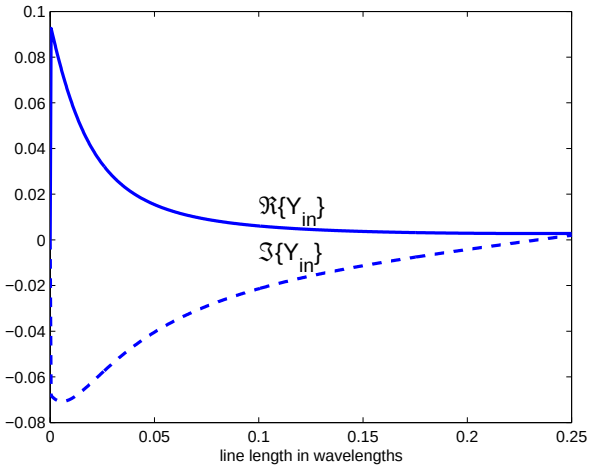

Figure 40: Variation of admittance along the transmission line.

We will assume a printed circuit board with 1.56mm substrate and $\epsilon_r = 4.4$. Assuming all transmission lines to be 50Ω, then $w = 2.975mm$ and $\lambda = 182.6mm$. As a consequence, $S = 32.34mm$ and $L = 33.8mm$. Unfortunately, open ended stubs will suffer from end effects that cause the effective length to be increased by

$$\Delta = 0.412 \frac{\epsilon_{\text{eff}} + 0.3}{\epsilon_{\text{eff}} - 0.258} \frac{w + 0.264h}{w + 0.8h} h \tag{48}$$

and this amount will need to be removed from the calculated length L of the stub. For the above $50/Omega$ transmission line $\Delta = 0.61mm$ and so $L = 33.19mm$.

Exercise

Design a stub matching system that transforms the impedance for $100 + j20\Omega$ into 50Ω.

Design of Amplifiers Based on Microstrip Transmission Lines

We will now consider the design of a power amplifier for the frequency of 900MHz using a Philips BLT81 BJT transistor. The transistor can handle over 1W of power and we will design for 50Ω load and source. From the data sheet of the BLT81, it will present a $W = 7 + j5\Omega$ input impedance and a require a load of $W = 18 + j4\Omega$. We will transform the input and output impedance using microstrip transmission line matching. Consequently, we can use a printed circuit construction of the form shown in Figure 41. If we assume a 1.56mm substrate with $\epsilon_r = 4.4$, then we have already designed the input matching circuit in the example above, i.e. $S1 = 32.34mm$ and $L1 = 33.19mm$. The output of the amplifier will need to look into a load $18 + j4\Omega$ and this is equivalent to the problem of matching a $18 - j4\Omega$ source to 50Ω. In the same fashion as above, we find that the transmission line connected to the 50Ω load will have a conductance of 0.02 at

distance $S2 = 0.1\lambda$ from the load with susceptance -0.0215. To cancel the susceptance we will need a reactance $X = -46.5\Omega$. This is capacitive and is achieved with a open stub of length $L2 = 0.181\lambda$. As a consequence $S2 = 33.33mm$ and $L2 = 33.05mm$. As for the input L network, we will need to remove $\Delta = 0.61mm$ from the end of the stub to account for end effects, i.e. $L2 = 32.66mm$.

To complete the design, we need to add base bias and collector supply. Further, these supplies need to be isolated RF wise from the transistor. In a low frequency design, this is normally achieved through RF chokes. In the case of a high frequency design, however, there is the option of using short circuited $\lambda/4$ transmission lines. At the open end of such transmission lines, there will be infinite impedance and so no RF current will flow into the line, i.e. they will act like a choke. In the circuit of Figure 41, the base bias and supply voltage are isolated by this means.

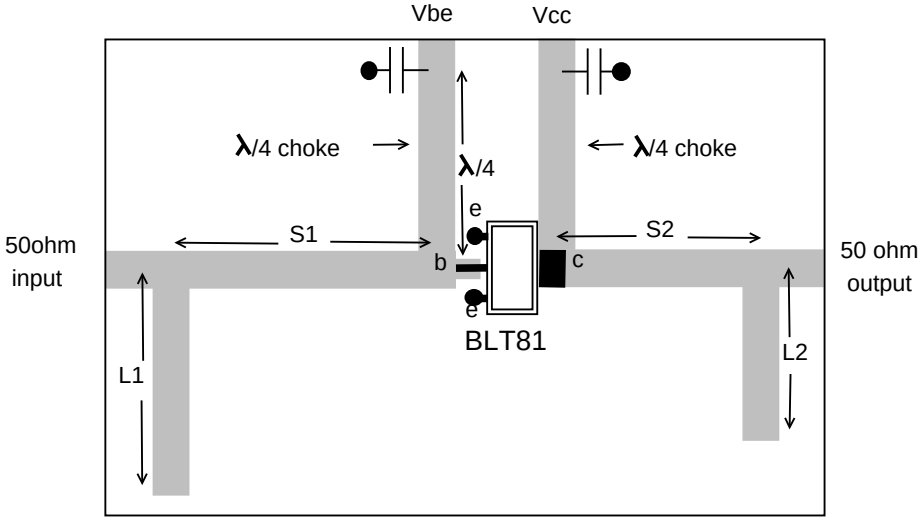

Figure 41: A UHF power amplifier with microstrip matching.

Exercise

Redesign the above amplifier for a frequency of 800Mhz.

Feeding Dipole Antennas

Arguably the simplest antenna is the electrical dipole, but there are important factors to be recognised in its practical implementation. Firstly, a dipole is a balanced device and so, if we need to feed it with an unbalanced transmission line (a coaxial cable for example), we will need to interface it with a BALUN (see Figure 42a). Commonly available cable has an impedance of 50Ω and so, even after interfacing with a 1:1 BALUN, there will still be a mismatch due to the 73Ω impedance of the dipole. In fact, there will be a reflection coefficient of 0.19. Fortunately, however, this only amounts to reflected power of a few percent. We need not feed the dipole at the middle, but the antenna input resistance R_d

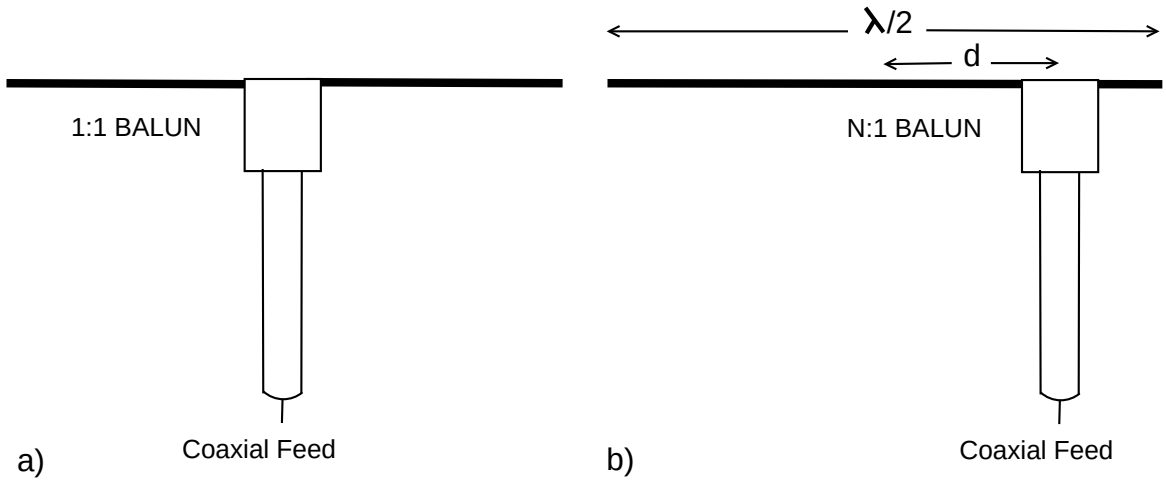

Figure 42: Dipole antennas fed by BALUNS.

rises as we move out along the dipole. At distance d from the centre,

$$R_d = R_m \frac{1}{\cos^2\left(\pi \frac{d}{\lambda}\right)} \tag{49}$$

where R_m is the resistance at the centre. Consequently, for an offset feed, we clearly need a BALUN that also transforms impedance (see Figure 42b) and a typical broadband 4:1 BALUN (4 to 1 impedance conversion) is shown in Figure 43.

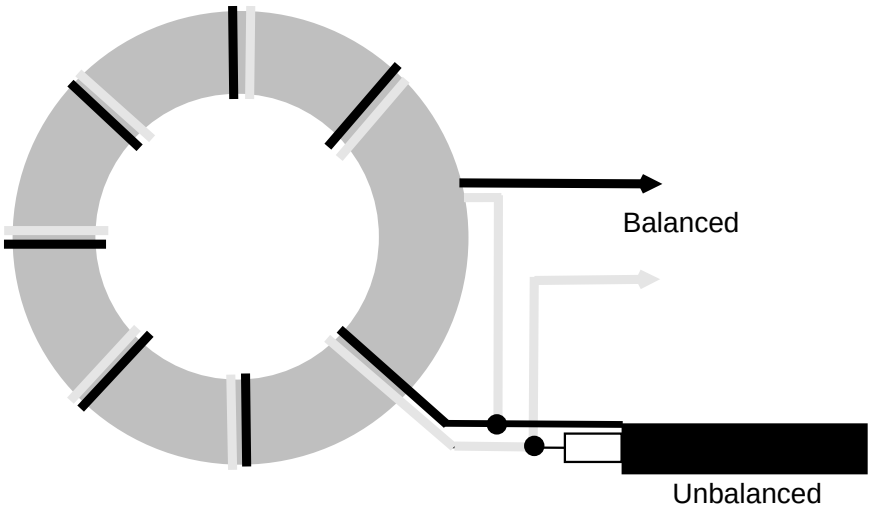

Figure 43: A 4:1 BALUN.

T and Gamma Matching

A dipole, when driven by a T match, consists of an unbroken dipole rod (length $2l$) and a parallel shorter rod (length $2s$) that is fed at its centre by a balanced feeder (see Figure 44a). (Note that the shorter rod is connect to the dipole at its ends and that the

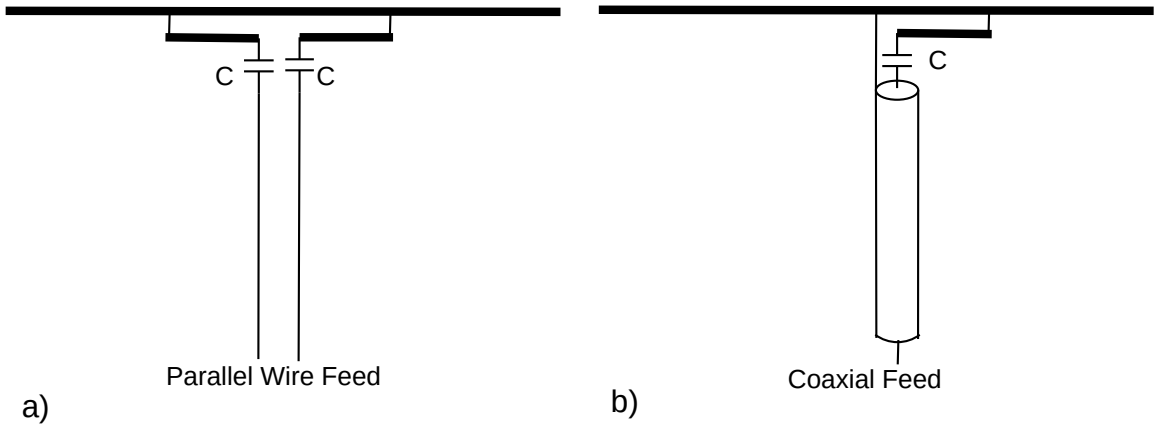

Figure 44: Dipole antennas fed with various feeds.

feed includes capacitors that cancel out the inductance that is generated by the match.) If we split the antenna in the middle (see Figure 45), we can replace one half by an imaginary perfectly conducting plane (i.e. the missing half of the dipole is the image in the plane). Essentially, we will have a monopole that is fed against a perfectly conducting plane. The two parallel rods form a transmission line stub on which there are both even and odd modes. The odd mode (this is the standard mode for a transmission line) will have equal magnitude currents travelling in opposite directions (I_o and $-I_o$). This will be the result of voltage sources V_o and $-V_o$ that drive the monopole rods. There will also be an even mode with currents I_e and I_e flowing into each rod. Together, these flows constitute the current in the monopole and result from the voltage sources V_o and V_e that drive the monopole rods. However, the centre of the dipole is at zero volts (it is connected to the imaginary conducting plane) and so we must have $V_e = V_o$. For the odd mode (the transmission line mode) we will have $I_o = 2V_o/Z_{tl}$ where Z_{tl} is the impedance looking into the the transmission line. For the even mode, we note that the total current flowing into the monopole is $2I_e$ and that the impedance looking into the monopole is $Z_{dip}/2$ where Z_{dip} is the impedance looking into the dipole. The voltage between between the monopole and the imaginary plane is V_e and so $V_e/2I_e = Z_{dip}/2$, i.e. $I_e = \frac{V_e}{Z_{dip}}$. The current flowing from the feedline into the gamma match will be

$$I = I_e + I_o = \frac{V_e}{Z_{dip}} + 2\frac{V_o}{Z_{tl}} \tag{50}$$

On noting that $V_e = V_o$, the voltage drop between the feedline and the plane will be $2V_e$ and hence the impedance looking into monopole with gamma match will be

$$\begin{aligned} Z_G &= \frac{2V_e}{I} = \frac{2V_e}{\frac{V_e}{Z_{dip}} + 2\frac{V_o}{Z_{tl}}} \\ &= \frac{2Z_{dip}Z_{tl}}{2Z_{dip} + Z_{tl}} \end{aligned} \tag{51}$$

The impedance is essentially that of twice the antenna impedance in parallel with the stub transmission line impedance. Looking into a dipole with T match, we essentially

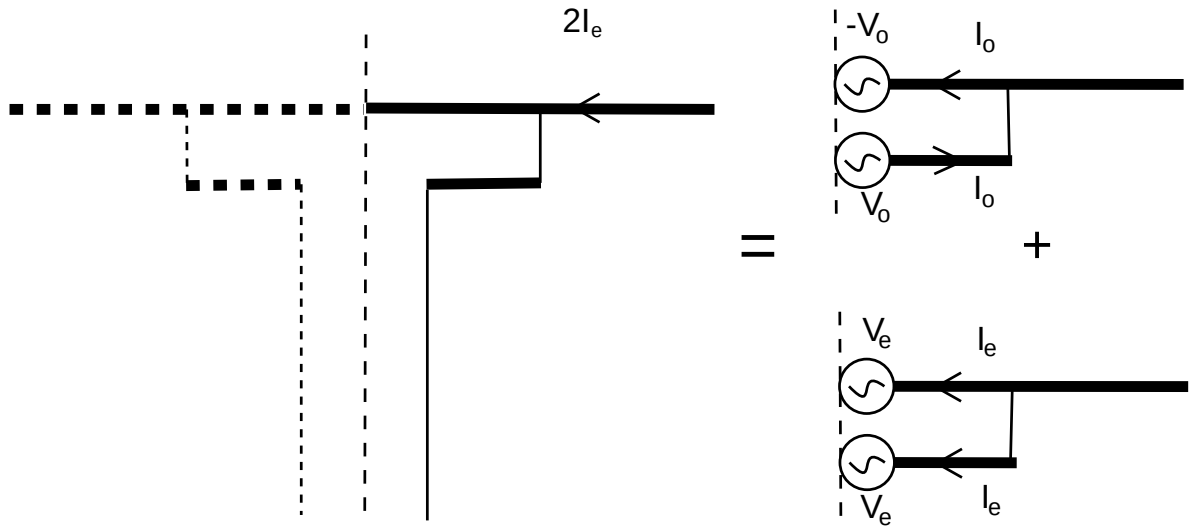

Figure 45: Dipole antenna fed with a gamma match when analysed as a monopole.

have back to back monopoles with T gamma matches and the impedance will simply be $2Z_G$, i.e. the impedance

$$Z_T = \frac{4Z_{dip}Z_{tl}}{2Z_{dip} + Z_{tl}} \tag{52}$$

The impedance is essentially that of four time the antenna impedance in parallel with twice the stub transmission line impedance. Consequently, by choosing Z_{tl} correctly, we can transform the input impedance of a dipole to that which matches the feed. If the antenna has an unbalanced feed (typically a coaxial cable), we can use the arrangement shown in Figure 44b. Essentially, we treat the antenna as a monopole with the right hand half of the dipole generating an effective conducting plane. The input impedance that this arrangement presents to the feed will then be the Z_G above.

As an example, consider a dipole for which we have slightly shortened in length so that its centre impedance is 73Ω (to do this we need to shorten a $\lambda/2$ dipole by about 5 percent). We want to match this to a 50Ω coaxial cable by means of a gamma match and first note that Z_{tl} can be calculated from expression 51. However, the transmission line can only produce a reactive impedance, i.e. $Z_{tl} = jX_{tl}$, and so the transmission line alone cannot produce a Z_G that is purely resistive, i.e. $Z_G = 50 + jX_G$. Noting that $Z_{dip} = 73$, 51 will imply that

$$(50 + jX_G)(2 \times 73 + jX_{tl}) = j2 \times 73X_{tl} \tag{53}$$

and from which $X_G X_{tl} = 7300$ and $X_G = 96X_{tl}/146$. As a consequence, $X_{tl} = 105\Omega$ and $X_G = 69\Omega$. However, the reactive part of Z_G can now be canceled by choosing the capacitor C in Figure 44 such that $C = 1/X_G\omega$.

In order to produce a suitable X_{tl}, we need to know its relationship to the physical properties of the transmission. We assume both rods have the same radius a and a spacing of D. For a short circuit transmission line of length s and characteristic impedance Z_0, we have $X_{tl} = Z_0 \tan(\beta s)$. For a parallel wire transmission line, we have $Z_{tl} = 120 \cosh^{-1}(D/2a)$ and $\beta = 2\pi/\lambda$ where λ is the free space wavelength. We will normally have that $D \gg a$ and so we will have that $Z_{tl} \approx 120 \log(D/a)$. If the rods of the transmission line have unequal radius, we replace a by the geometric mean of their radii.

Exercise

Design a Dipole for use at 14MHz for use with a 50Ω coaxial feed.

Folded Dipoles and Full Wave Loops

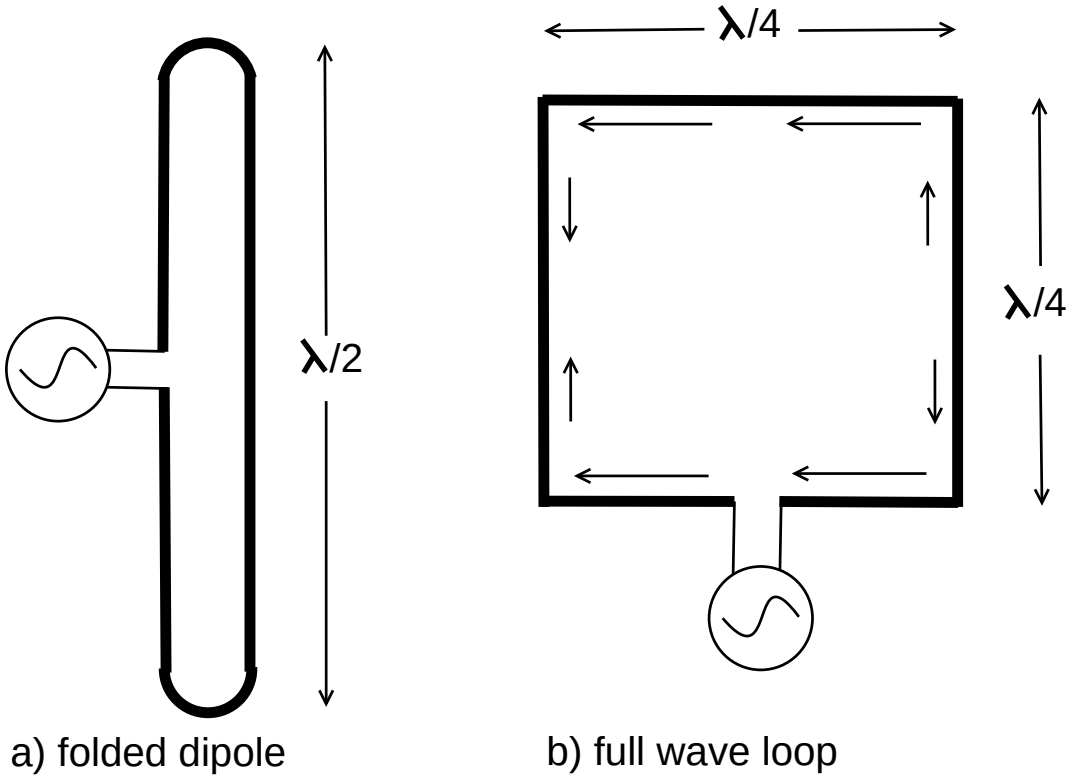

Figure 46: Folded dipole and large loop antennas.

We now consider the special case of a T match (see the previous example) for which the the stubs each have length $\lambda/4$. The reactance looking into the stubs will be $X_{tl} = Z_0 \tan(\beta\lambda/4) = \infty$ and hence, from 52, $Z_T = 4Z_{dip}$. This form of the dipole is known as a *folded dipole* and has an input impedance of 292Ω and a much wider bandwidth than the standard dipole. Essentially, the folded dipole is a loop antenna with sides of total length λ. However, two sides of the loop are so close together, and with matching currents, that they have the same total current distribution as a $\lambda/2$ dipole and hence the same radiation pattern. Another loop of interest is a square with sides of length $\lambda/4$. This can be regarded as a pair of two elements arrays (the sides parallel to the feed side and the sides orthogonal to the feed side). The radiation from the sides orthogonal to the feed side will cancel. However, the feed side, and the other side parallel to it, will combine to form a broadside array with strongest radiation in the directions orthogonal to the loop and with maximum gain of about 4dB. The loop will have an input resistance of around 100Ω, but needs to have a total length that is about 10 percent greater than a wavelength in order to eliminate the reactive part of its input impedance.

Dipole Chokes and Choke Dipoles

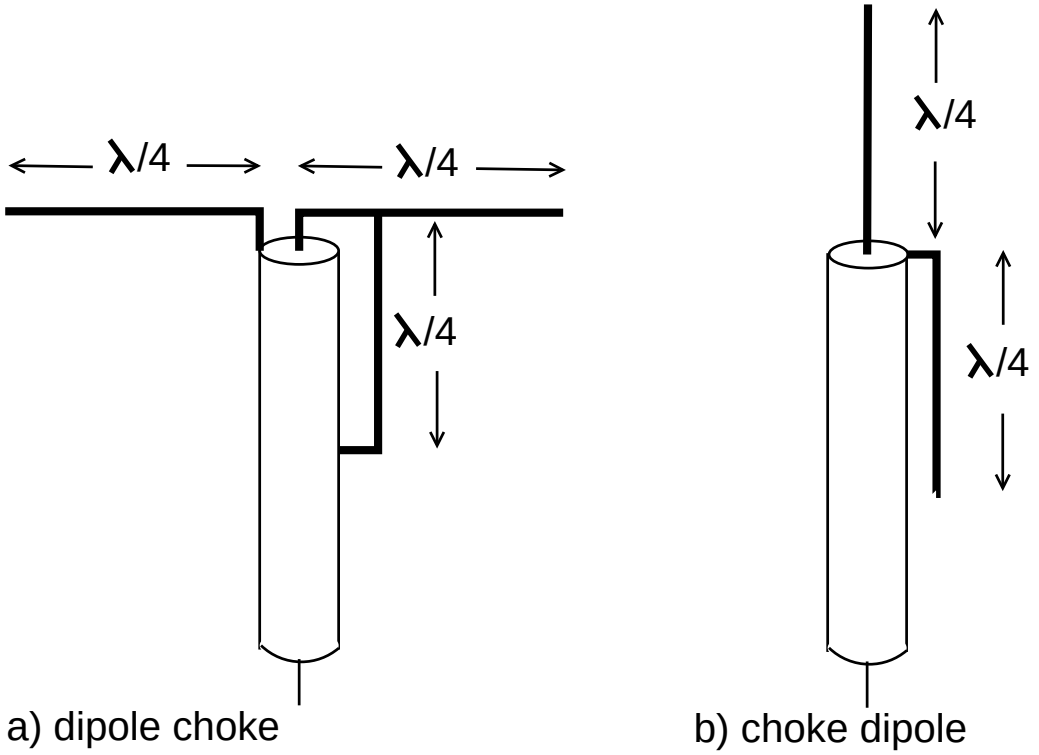

Figure 47: A transmission line choke BALUN and a choke dipole.

Consider a dipole that is fed by a coaxial cable. A BALUN can be formed at the dipole centre by using the coaxial outer as part of a transmission line, as shown in Figure 47a. This will be a parallel wire transmission line with unequal radius wires, the outer of the coax and a parallel wire. Without the $\lambda/4$ parallel wire, current will flow up the cable inner and into both the left dipole arm and down the cable outer. However, for the right hand arm the current will simply flow from the dipole arm into the cable inner. This can cause an imbalance of current on the dipole which is removed by choking off the flowing on the dipole outer. We have seen before that this can be achieved by wrapping the coaxial cable round a ferrite ring. With a $\lambda/4$ parallel wire in place, however, a current flows up the wire from the cable outer that balances the current flowing down the cable. Since the wire and cable outer constitute a shorted $\lambda/4$ transmission line, it will present an infinite impedance at the dipole centre and hence not affect the dipole operation. It should be noted that the parallel wire is sometimes replace by a $\lambda/4$ metal tube that surrounds the cable and in this case we have what is known as a *Bazooka BALUN*.

One of the problems with a dipole is that, unless the feed can be kept orthogonal to the dipole, it can interact with the dipole and change both its radiation pattern and input impedance. Fortunately, we can use the idea of a choke in order to overcome this problem. In figure 47b we show a dipole that is fed by a coaxial cable. In this configuration, the lower dipole arm forms a choke with infinite impedance at its lower end and therefore no current will flow along the outer of the feed cable. As with the dipole choke, the parallel wire can be replaced by a tube that surrounds the cable and in this case will be a coaxial

transmission line with its inner conductor being the outer of the feed cable.

Helical Dipoles

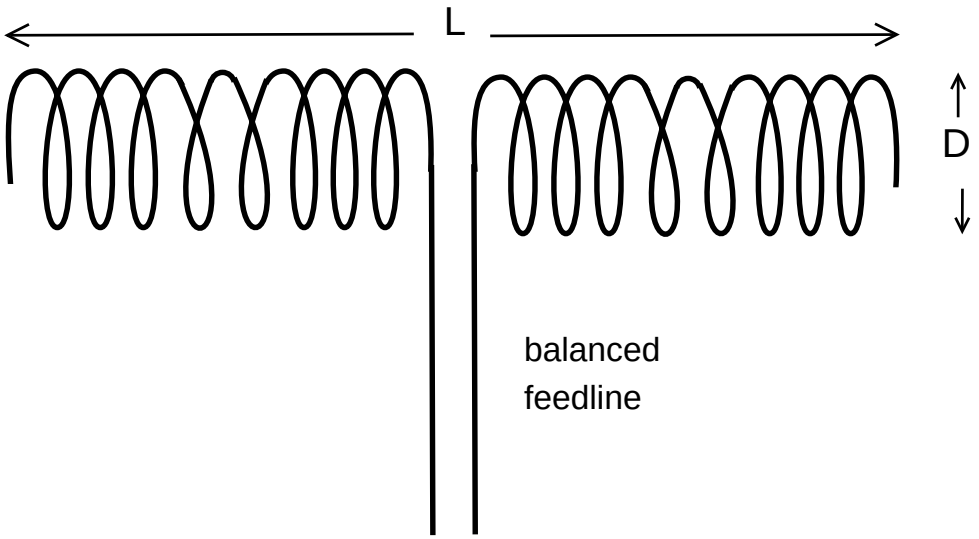

Figure 48: Shortened dipole with arms consisting of helical windings.

At low frequencies the size of a dipole (or even a monopole) can become too large for practical purposes and we need to find ways of shortening the antenna. As mentioned in chapter 9, we can shorten an antenna by using a helical winding instead of a straight wire. In the case of a helical wire, the wave speed c will be given by

$$c = \frac{c_0}{\sqrt{1 + 20(nD)^{2.5}\left(\frac{D}{\lambda_0}\right)}} \tag{54}$$

where λ_0 is the free space wavelength, n is the number of turns per centimetre and D is the helix diameter in centimetres (see Kandoian and Sichel in *IRE National Convention Record*, part 2, Antennas and Components, 1953, pages 42-47). It will be noted that $\lambda/\lambda_0 = c/c_0$ where λ is a wavelength on the helix and λ_0 is the wavelength in free space, i.e. the slower the wave on the winding the shorter the effective wavelength. In theory, we could make very small resonant antennas using helical windings, but there is a downside. Wheelers result tells us that the smaller we make an antenna,the smaller will be its bandwidth. Consequently, bandwidth is an important issue when miniaturising antennas.

Exercise

A dipole is to operate at a frequency of 14MHz, but should not exceed 4m in length. Design a suitable helical dipole with winding diameter no greater than 10cm (made from slinky springs perhaps).

Active Monopoles and Dipoles

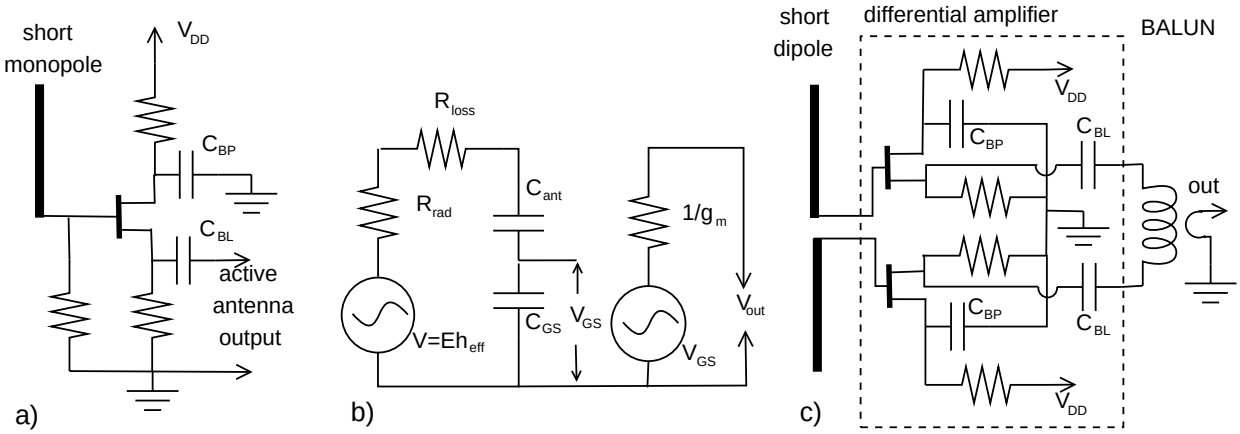

Figure 49: Active monopole and dipole antennas.

As we have noted in chapter 8, an electrically small antenna has an extremely high Q and therefore a small bandwidth. However, the advent of high frequency semiconductors has opened up another possibility, the *active antenna*. Figure 49a shows an example of a simple active antenna that is based upon a short monopole and source follower amplifier. Figure 49b, shows a model of this amplifier. The antenna is represented as a voltage source V_{ant} with impedance

$$Z_{ant} = R_{rad} + R_{loss} + jX_{ant} = 40\left(\frac{\pi l}{\lambda}\right) + \frac{l}{6\pi a\delta\sigma} - j\frac{60}{\beta l}\left(\ln\left(\frac{l}{a}\right) - 1\right) \qquad (55)$$

where l is the rod length, a is its radius and $\beta = \omega/c_0$. The antenna impedance has resistive parts (the radiation and ohmic losses) and a capacitive reactive part $C_{ant} = l/60c_0\left(\ln\left(\frac{l}{a}\right) - 1\right)$. It will be noted that the input to the JFET is also capacitive and so the voltage is fed into the amplifier through a capacitive voltage divider. For a short dipole, we will have a high Q and can therefore neglect the voltage drop across antenna resistance in comparison with the voltage drop across its reactance. Further, $V_{ant} = h_{eff}E$ where E is the electric field the is incident upon the antenna and h_{eff} is the effective length (half the physical length for a short monopole). As a consequence, the voltage appearing at the open circuit output of the source follower will be approximately

$$V_{out} \approx Eh_{eff}\frac{C_{ant}}{C_{ant} + C_{GS}} \qquad (56)$$

and is clearly independent of frequency. Consequently, by means of electronics, we have turned an inherently narrow band antenna into a frequency independent antenna. The electronics will bring its own problems, intermodulation for example, but extremely effect active antennas are possible with modern transistors. Obviously, it is also possible to build an active dipole and Figure 49c shows an example of such an antenna.

Exercise

Design a simple active monopole using a J310 FET ($V_T = -3V$ and $K = 5 \times 10^{-3} A/V^2$) for an output impedance of 50Ω.

Active Loop Antennas

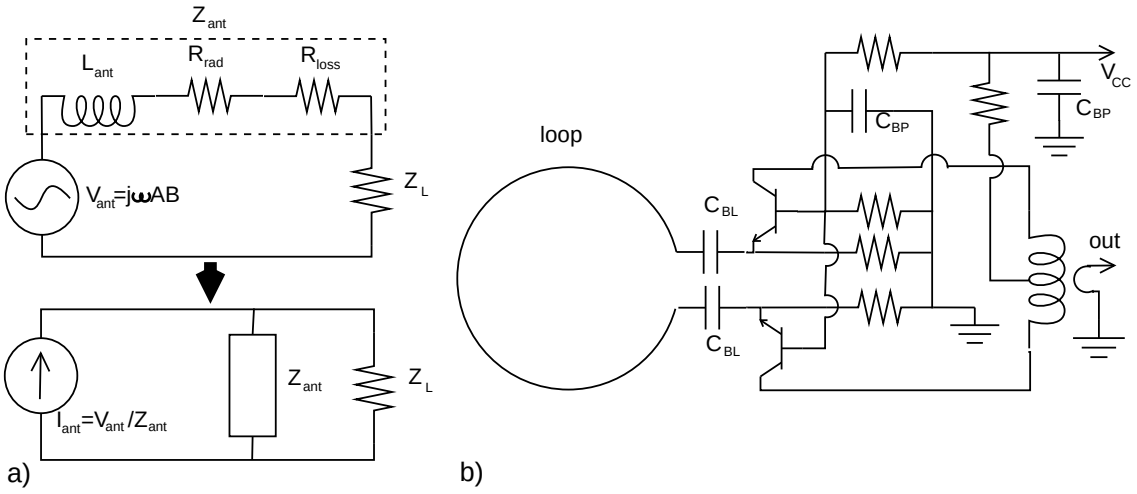

Figure 50: Active loop antennas.

Small loops can also be made into effective frequency independent antennas, but their operation is very different. Figure 50a shows the equivalent circuit of a loop that is connected to a load R_L. The antenna is represented as a voltage source V_{ant} with impedance

$$Z_{ant} = R_{rad} + R_{loss} + jX_{ant} = 20\beta^4 A^2 + \frac{l}{2\pi a \delta \sigma} + j\frac{\omega \mu_0}{2\pi} l \left(\ln\left(\frac{4l}{\pi a}\right) - 1.75 \right) \qquad (57)$$

where A is the area of the loop, $\beta = \omega/c_0$, l is the length of the loop wire and a is its radius. Further, the loop is excited by the magnetic field B of the incoming wave such that $V_{ant} = j\omega AB$ (note that we have assumed that the loop is oriented so that the magnetic field is orthogonal to its plane). As we have seen in chapter 5, we can rearrange the antenna voltage source into a current source, as shown in Figure 50a. For a small loop, the Q will be high and so $Z_{ant} \approx jX_{ant}$ and from this

$$I_{ant} = \frac{V_{ant}}{Z_{ant}} \approx \frac{2\pi AB}{\mu_0 l} \frac{1}{\ln\left(\frac{4l}{\pi a}\right) - 1.75} \qquad (58)$$

i.e., the current source is frequency independent. The trick now is to make the load impedance as low as is practical and then the lions share of this frequency independent current will flow into the load. A possible implementation of these ideas is shown in Figure 50b. The low load impedance is achieved by the use of common base amplifiers. Once again, electronics has turned an inherently narrow band antenna into a frequency independent antenna. In the figure, the outputs of the two common base amplifiers are combined through a transformer, but this could also be achieved through a differential amplifier with the appropriate bandwidth.

Design of a Patch Antenna

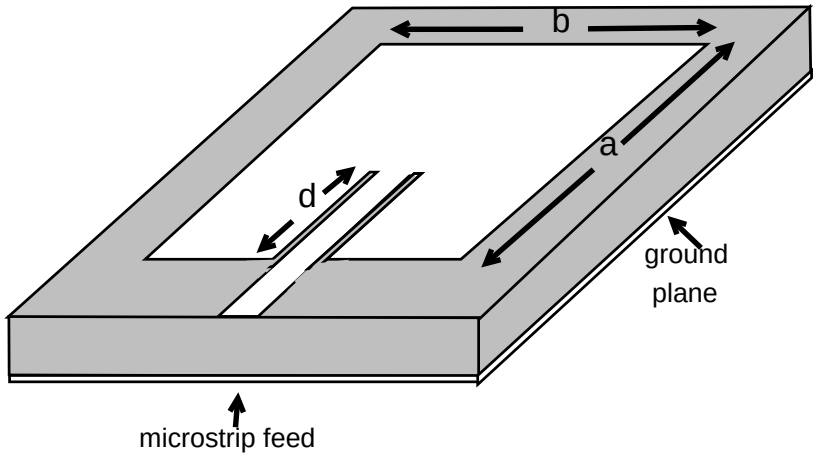

Figure 51: A rectangular patch antenna with microstrip feed.

We will consider the design of a patch antenna for operation at 1.5GHz and with input impedance 50Ω (see Figure 51). We assume that the antenna is built from printed circuit board with 1.56mm FR4 substrate ($\epsilon_r = 4.4$) and has a microstrip feed. For frequency $f = 1.5GHz$, will need the length a to be half a wavelength with respect to the substrate, i.e. $a = c_o/2f\sqrt{\epsilon_r} = 3 \times 10^8/2 \times 1.5 \times 10^9 \times \sqrt{4.4} = 0.0477$ metres ($4.77cm$). Due to end effects, the value of a will need to be shortened by $\Delta \approx 0.42h(\epsilon_r + 0.3)/(\epsilon_r - 0.258)$, i.e. $\Delta = 0.74mm$. As a consequence $a = 4.62cm$. To prevent lateral modes forming under the patch, we need to choose b to be significantly less than a (we will choose $b = 4cm$ in the current design). For a microstrip feed of 50Ω, we will need a width $5.7mm$. The impedance at the edge of the patch is given by $R_{edge} = 60\lambda_o/b$. Then, since $\lambda_0 = 20$cm and $b = 4$cm, we obtain that $R_{edge} = 300\Omega$. At distance d from the edge of the patch, a feed will encounter an impedance

$$R_{in} = R_{edge} \cos^2\left(\frac{\pi}{a}d\right) \tag{59}$$

Consequently, the feed will need to penetrate a distance d into the patch where d satisfies $50 = 300\cos^2(\pi d/4.77)$ (i.e. $d = 1.69cm$). Since the microstrip feed penetrates into the patch, this will require a gap (i.e. no metal) between the microstrip feed and the patch itself. A gap equal to the substrate thickness is usually sufficient.

Exercise

Redesign the above patch antenna for a frequency of 2.5GHz.

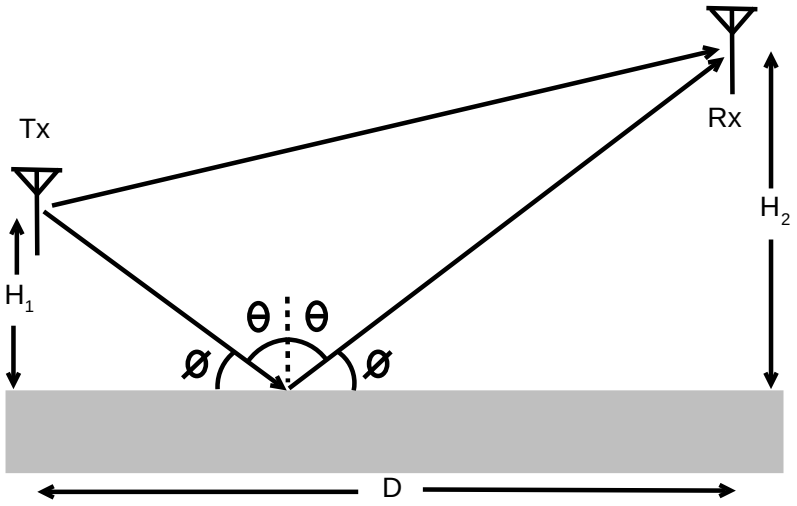

Figure 52: The effect of ground reflections upon propagation.

Extensions of the Friis Equation

If the communication between two radio stations involve ground reflections, Friis equation needs to be modified, i.e.

$$P_R = P_T G_R G_T \left(\frac{\lambda}{4\pi D}\right)^2 \left|1 + R_g \exp\left(-4j\pi \frac{H_1 H_2}{\lambda D}\right)\right|^2 \tag{60}$$

The reflection coefficient R_g will depend not only on the angle θ, but also on the polarisation and the properties of the ground. For vertical polarisation,

$$R_g = \frac{\frac{\cos\theta}{\eta_r^2} - \sqrt{\frac{1}{\eta_r^2} - \sin^2\theta}}{\frac{\cos\theta}{\eta_r^2} + \sqrt{\frac{1}{\eta_r^2} - \sin^2\theta}} \tag{61}$$

where η_r is the relative impedance of the ground. In most propagation problems, the angle θ is close to $\pi/2$ and so the above expression can be approximated by

$$R_g \approx \frac{\phi - \eta_r\sqrt{1-\eta_r^2}}{\phi + \eta_r\sqrt{1-\eta_r^2}} \tag{62}$$

where $\phi = \pi/2 - \theta$. It is clear that at low elevations (i.e. low values of ϕ) $R_g \approx -1$. However, as ϕ rises, there comes a point where R_g changes sign and heads towards a value of 1 (i.e. the reflection coefficient for a perfectly conducting plane). The angle at which the sign changes is known as the *Brewster's angle*. In the case of lossy ground, the impedance in the above formulas will need to be replaced by the effective relative impedance

$$\eta_{er} = \eta_r \frac{1}{\sqrt{1 - j\frac{\sigma}{\omega\epsilon}}} \tag{63}$$

where σ is the conductivity of the ground and ϵ is its permittivity. For typical pastoral land, we have $\sigma = 0.01 S/m$ and $\epsilon = 8.854 \times 10^{-11} F/m$ and so $\eta_{er} = 0.316/\sqrt{1 - j18/f}$

where f is the frequency in MHz. To a first approximation, $\phi \approx (H_1 + H_2)/D$ and so, for most terrestrial propagation, a value of -1 for R_g is appropriate. The exception is at very low frequencies where the effective impedance can become very small. However, at these frequencies the surface wave propagation will far exceed the *space wave propagation* (the propagation that is described by the Friis equation). Another way of writing the Friis equation for space wave propagation is

$$P_R = P_T G_R G_T \frac{1}{L_{fs}} \frac{1}{L_{refl}} \tag{64}$$

where $L_{fs} = (4\pi D/\lambda)^2$ is the loss in free space and $L_{refl} = 1/\left|1 + R_g \exp\left(-4j\pi \frac{H_1 H_2}{\lambda D}\right)\right|^2$ is the additional loss due to ground reflections.

We would also like a Friis equstion for surface wave propagation. As we have seen in chapter 9, an alternative way of looking at the propagation problem is as a 2 port network. In chapter 8, we saw that the mutual impedance between receive and transmit antennas in free space is given by

$$Z^0_{TR} = j\omega\mu_0 h^T_{eff} h^R_{eff} \frac{\exp(-2j\pi \frac{D}{\lambda})}{4\pi D} \tag{65}$$

However, in chapter 8, we also found that the mutual impedance through surface wave propagation is

$$Z_{TR} \approx \frac{\eta_0 h^R_{\text{eff}} h^T_{\text{eff}}}{2\pi \tilde{\eta_r}^2 D^2} \exp(-2j\pi \frac{D}{\lambda}) = Z^0_{TR} \frac{2c_0}{j\omega \tilde{\eta}^2_r D} \tag{66}$$

where $\tilde{\eta}_r = \eta_r \sqrt{1 - \eta_r^2}$. Noting that $V_R = Z_{TR} I_T$, it can be seen that the Friis equation for surface waves will take the form

$$P_R = P_T G_R G_T \frac{1}{L_{fs}} \frac{1}{L_{sw}} \tag{67}$$

where $L_{sw} = |\omega \tilde{\eta}^2_r D/2c_0|^2$ is the additional loss due to the surface wave mode (note that η_r will need to be replaced by the effective permittivity η_{er} in the case of a ground with non zero conductivity).

Exercise

For antennas at heights of 10m, and the pastoral land described above, compare the propagation loss of the space and ground wave modes for a variety of distances D and frequencies f.

System Calculations for Passive Radar

In our current radio rich environment, a possible approach to radar is to use target illuminations by existing transmitter (a broadcast transmitter for example). This is what is known as *passive bistatic radar* since its operator does not require the radar to produce its own illuminations. In deciding whether such a radar can detect a target, the major

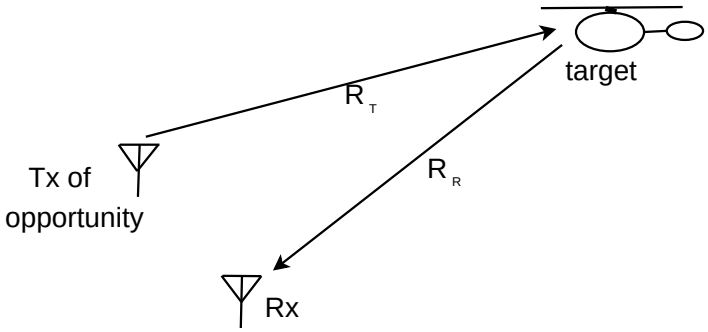

Figure 53: Passive bistatic radar.

calculation will be that of the SNR of the radar return at the receiver. From the radar equation

$$SNR = \frac{P_T}{N} G_R G_T \left(\frac{\lambda}{4\pi R_T}\right)^2 \left(\frac{\lambda}{4\pi R_R}\right)^2 \frac{4\pi\sigma}{\lambda^2} \tag{68}$$

where N is the total noise being received through the antenna (we assume the receiver has been designed to be externally noise limited). An example of a suitable illuminator of opportunity is the DAB transmitters that have now mainly replaced FM transmitters. Most of these transmitters operate around a frequency of 200MHz ($\lambda = 1.5m$) and have a bandwidth of about 1.5MHz. Their large bandwidth makes them ideal for aircraft observation as they will exhibit range resolution of the order of 200m. For a typical DAB transmitter we will have an effective radiated power (i.e. $P_T G_T$) of the order of 10kw and we will assume the receive antenna has a gain of 10dB. For DAB frequencies, a typical level of noise is $10^{-20} W/Hz$ and so the radar returns will need to compete with a noise level of $1.5 \times 10^{-14} W$. Consider a target consisting of a small jet for which $4\pi\sigma/\lambda^2 = 100$ is a typical value. If we assume that $R_T = 12km$ and $R_R = 10km$, the radar equation will yield an SNR of 9.4 and detection is possible.

Although the above calculation suggests that the target can be detected, there is a major problem with passive radar in that the direct signal from the illuminator can swamp the radar receiver. Such signal are known as *direct signal interference* (DSI). At VHF frequencies, the space wave will dominate over the surface wave and so the power in the DSI will be

$$\begin{aligned} P_R^{DSI} &= 4P_T G_R G_T \left(\frac{\lambda}{4\pi D}\right)^2 \sin^2\left(\beta \frac{H_T H_R}{D}\right) \\ &\approx P_T G_R G_T \left(\frac{\lambda}{4\pi D}\right)^2 \frac{16\pi^2 H_R^2 H_T^2}{\lambda^2 D^2} \end{aligned} \tag{69}$$

where D is the distance between transmitter and receiver and H_T and H_R are the heights of the transmitter and receiver respectively.

To reduce the direct signal, the antennas of both receiver and transmitter will normally be designed so they they have a null in each others direction. However, it is sometimes possible to use an obstruction, a hill or a building, to hide the transmitter from the receiver. Although this will reduce the direct wave, there will still be power that reaches the receiver through the mechanism of diffraction. From chapter 9, the mutual impedance

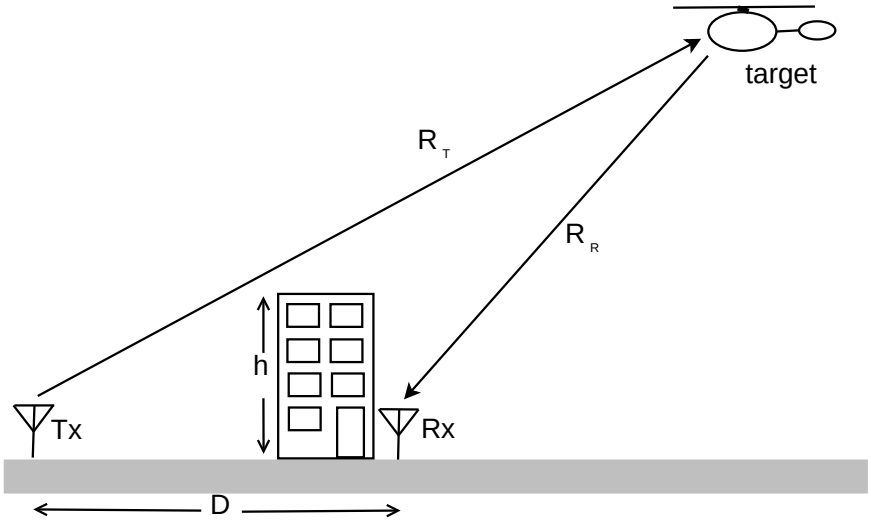

Figure 54: Reduction of DSI through an obstruction.

between the receive and transmit antennas will be

$$\begin{aligned} Z_{TR}^{DSI} &= \frac{j\omega\mu_0}{4\pi D}\sqrt{\frac{j}{\pi}}h_{\text{eff}}^{T}h_{\text{eff}}^{R} \\ &\times \exp\left(-j\beta R_{TR}\right)\int_{\nu}^{\infty}\exp\left(-jY^2\right)\,dY \end{aligned} \tag{70}$$

where $\nu = \sqrt{\beta/2D_TD_RD}\,(D_Th_R + D_Rh_T)$, h_T is the height of the obstruction above the transmitter, h_R is the height of the obstruction above the receiver, D_T is the distance of the transmitter from the obstruction, D_R is the distance of the receiver from the obstruction, $D = D_T + D_R$ and R_{TR} is the distance between the antennas. We will consider the simplified situation where the receiver and transmitter are at ground level, the obstruction is midway between transmitter and receiver and h is the height of the obstruction above the ground. We will also assume $h \gg \sqrt{\lambda D}$ and then $\nu = 2h\sqrt{\pi/\lambda D}$ will be large. For large ν, $\int_{\nu}^{\infty}\exp\left(-jY^2\right)\,dY \approx \exp\left(-j\nu^2\right)/2j\nu$ and so

$$Z_{TR}^{DSI} = Z_{TR}^{0}\frac{\exp\left(-j\nu^2\right)}{2\sqrt{j\pi}\nu} \tag{71}$$

and from this we see that

$$P_R^{DSI} = P_TG_RG_T\frac{1}{L_{fs}}\frac{1}{L_{diff}} \tag{72}$$

where $L_{diff} \approx 16\pi^2h^2/\lambda D$ and L_{diff} is the additional loss that is caused by the obstruction.

Exercise

Calculate the level of DSI at the Receiver site and determine what height of obstacle is required for the DSI to be reduced to the level of the target return. (Note that DSI does

not need to be completely removed as it can be discriminated from the target in range-Doppler space. The main issue is the dynamic range that the DSI will demand of the radar receiver.) Investigate the effect of moving the receiver much closer to the obstacle ($D_R \ll D_T$).