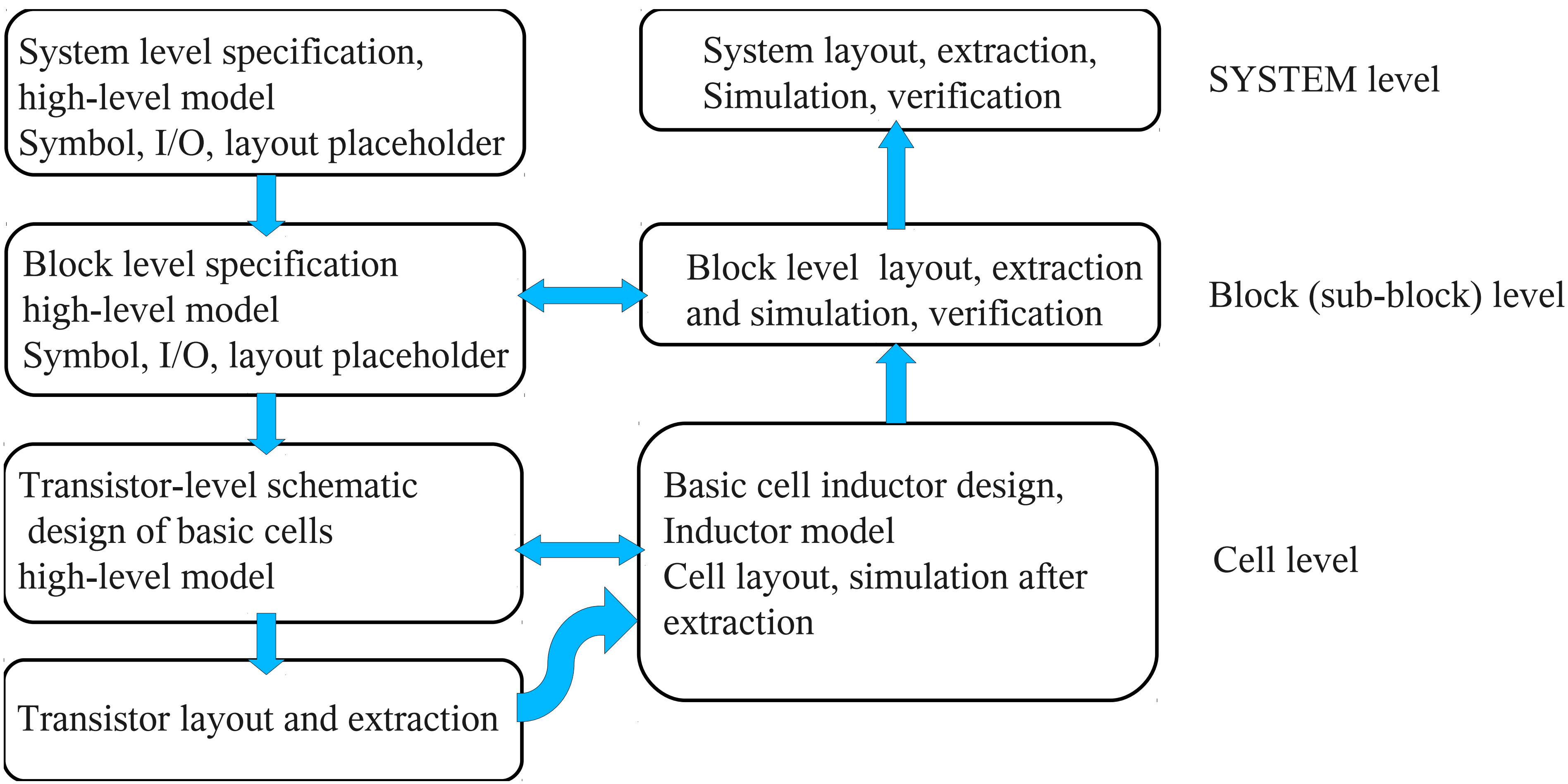
Chapter 13. SoC Design Flow

Outline

- Design flow for HF ICs
- Examples of mm-wave ICs

Top-down design flow for mm-wave SoCs



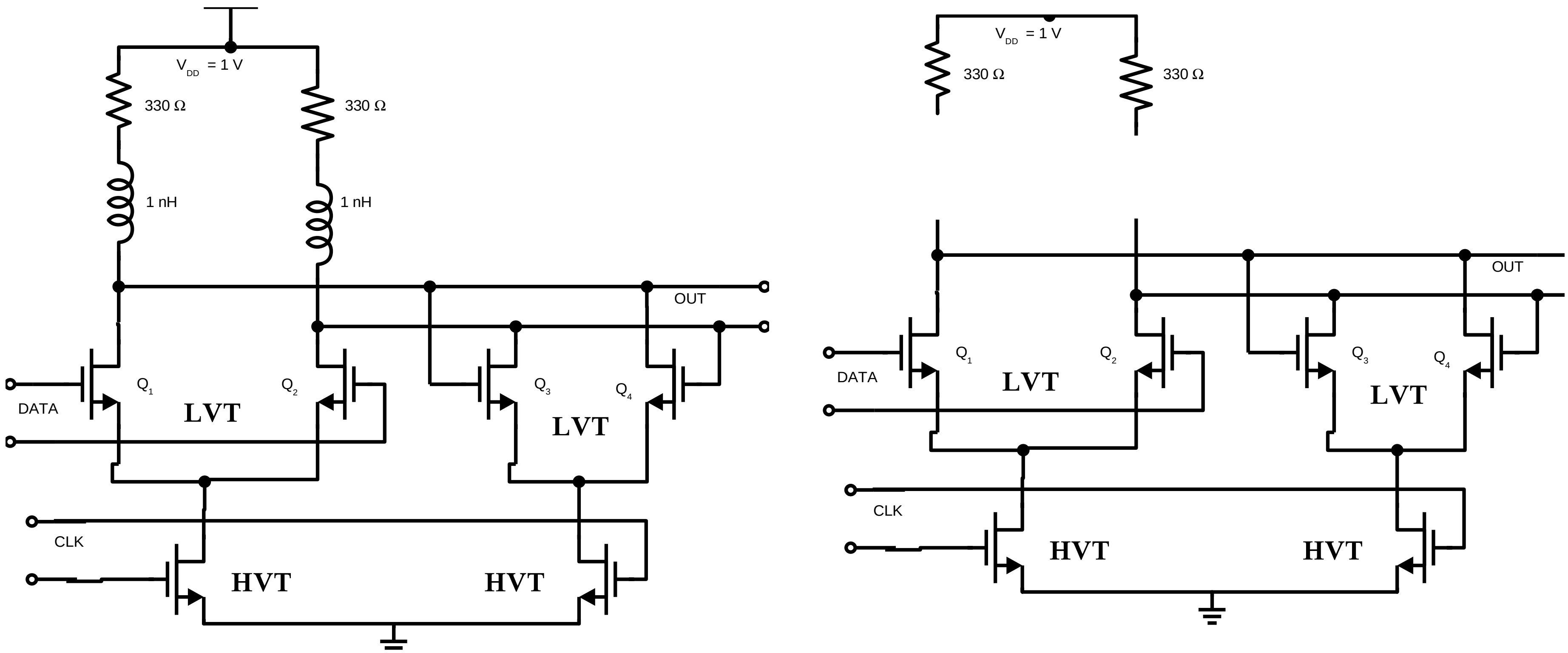
Design flow for HF ICs in nanoscale CMOS

- Check MOSFET model for sanity:
  - peak f_T current density = 0.3mA/μm ... 0.4 mA/μm
  - Add R_G and check f_{MAX}, NF_{MIN} and J_{OPT} = 0.12-0.15 mA/μm
- Transistor/varactor cell optimization: W_f to balance R_S, R_G and minimize C_{gd} and other parasitics. Fix W_f and vary just N_f.
- Schematic level design with R_G added to MOSFET digital model
- Transistor(cascode,CMOS inverter) layout optimization: choice of metal stack on drain and source depending on: CS, CG, CD, cascode, CMOS inv
  - monitor f_{MAX}, NF_{MIN}, gain
  - Parasitic resistance seems to be the killer in 65nm and beyond

Design flow for HF ICs in nanoscale CMOS (ii)

- Include RC-extracted transistor(cascode/CMOS inv) layout in schematic (expect significant > 20% performance degradation)
- Design inductors and interconnect in EM simulator based on schematic-level design with extracted transistors and pad capacitance
- Add metal ground and power mesh to cell and RC-extract cell (without inductors)
- Add inductor and interconnect models to schematic of RC-extracted cell
- Add interconnect modelled in ASITIC between cells

Example: Hierarchical breakout of cell for parasitic extraction

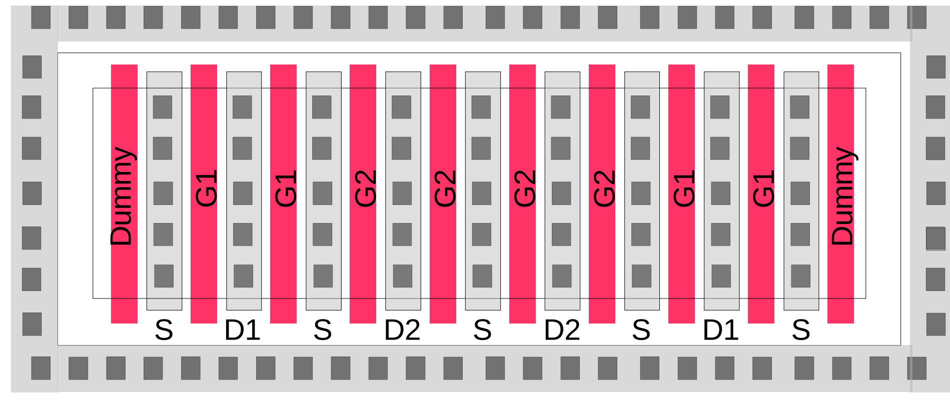


- Minimize cell layout footprint to reduce capacitance
- Extract cell RC
- Model inductors and long interconnect in ASITIC

Layout Issues

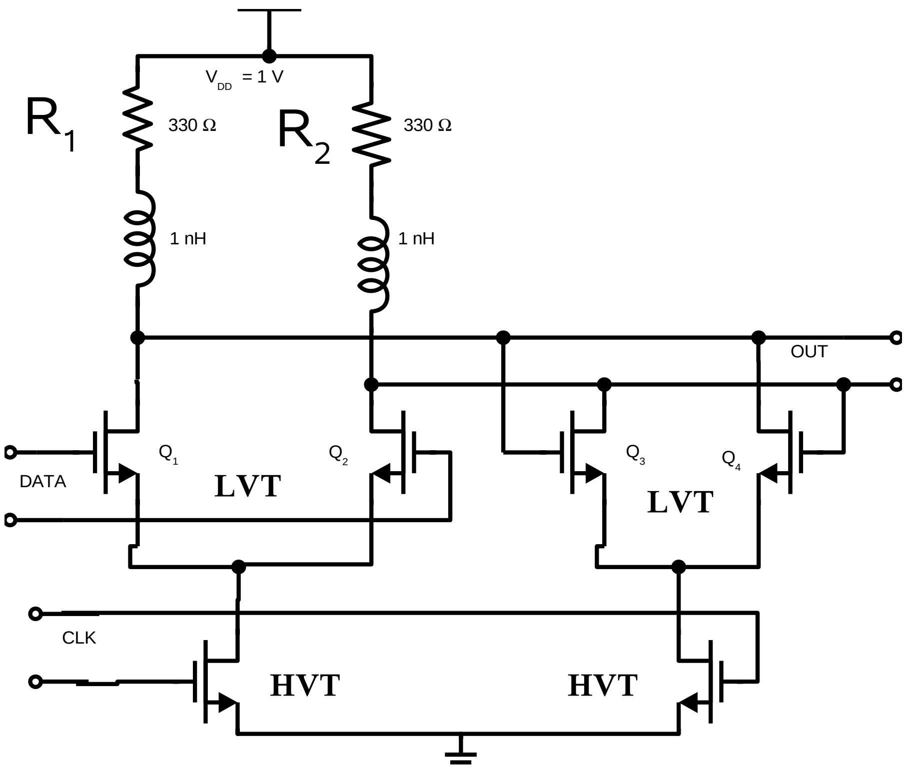
- Specific to mm-waves:
  - For performance: gate finger width in LNA/VCO
- For all applications using nano-scale CMOS:
  - For manufacturability (antenna rules, OPC)
  - For variability (strain, stress, and process variation)

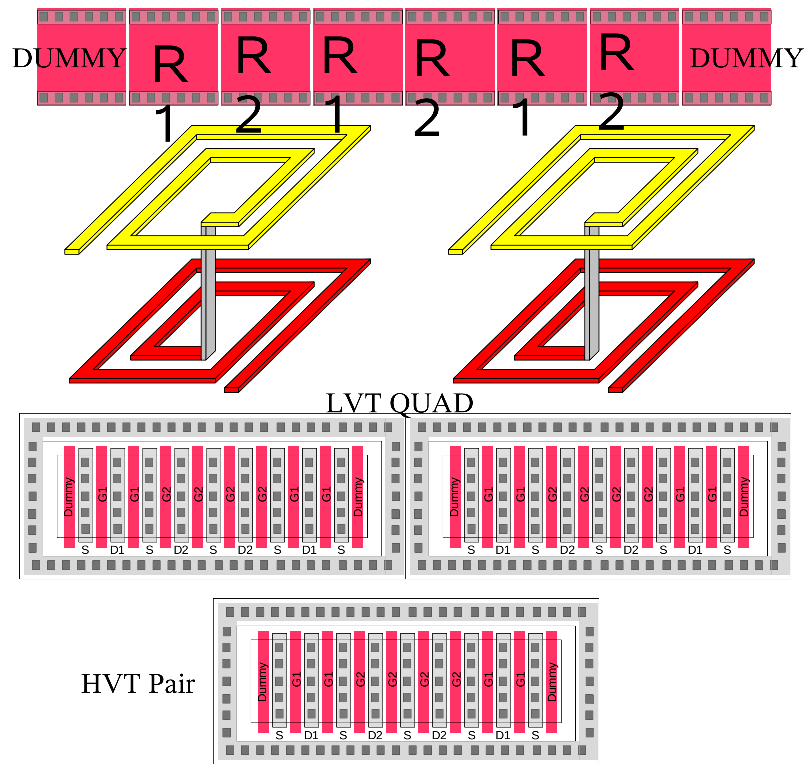
Diff. pair layout in nano-CMOS technologies



- Transistors share the same well and are interspersed symmetrically to minimize impact of process variation
- All fingers have the same orientation, W_f, L, to avoid photolithography problems and strain variation
- Dummy gates are placed on each side to ensure L uniformity, ease photolithographical phase correction, and reduce impact of strain variation

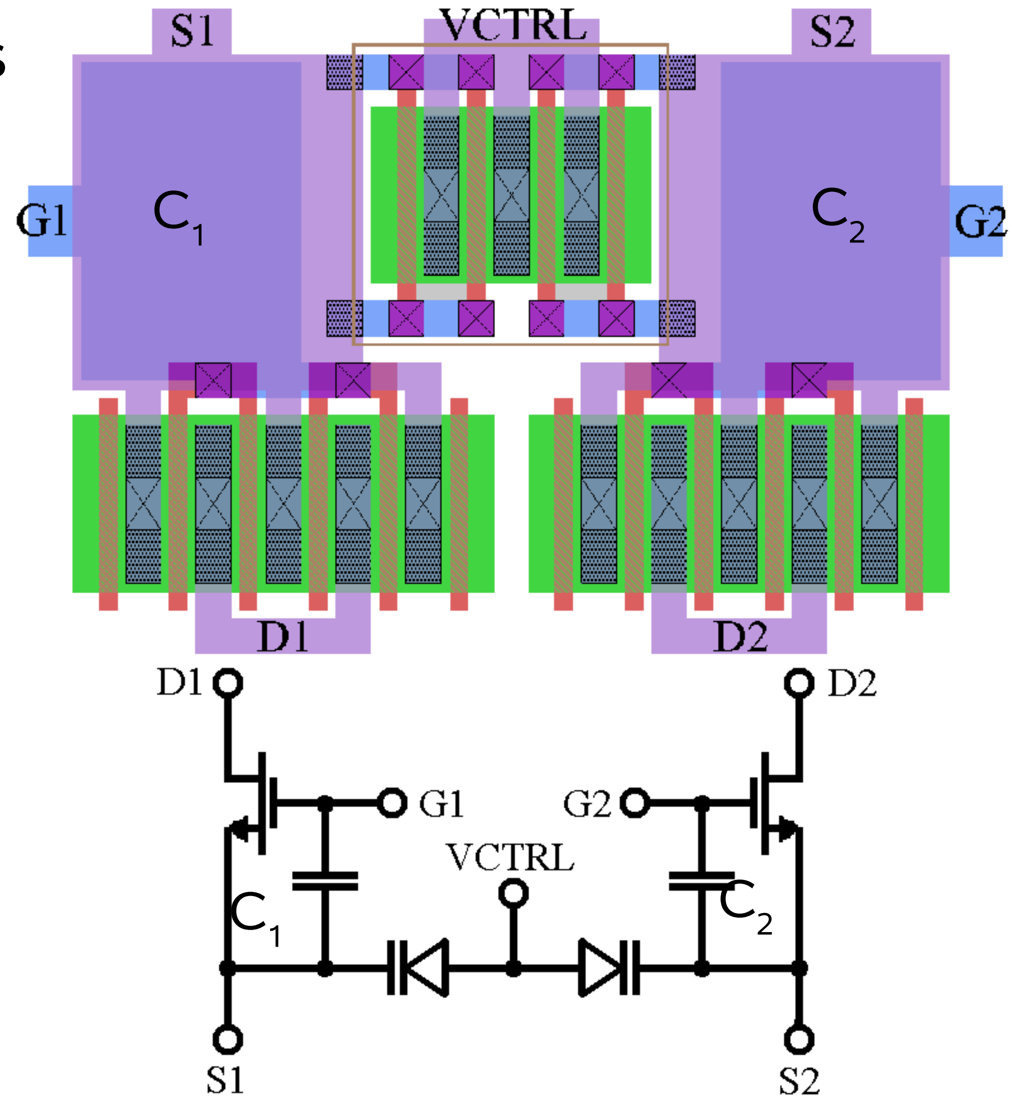
CMOS Latch, Selector, and Gilbert Cell Layout



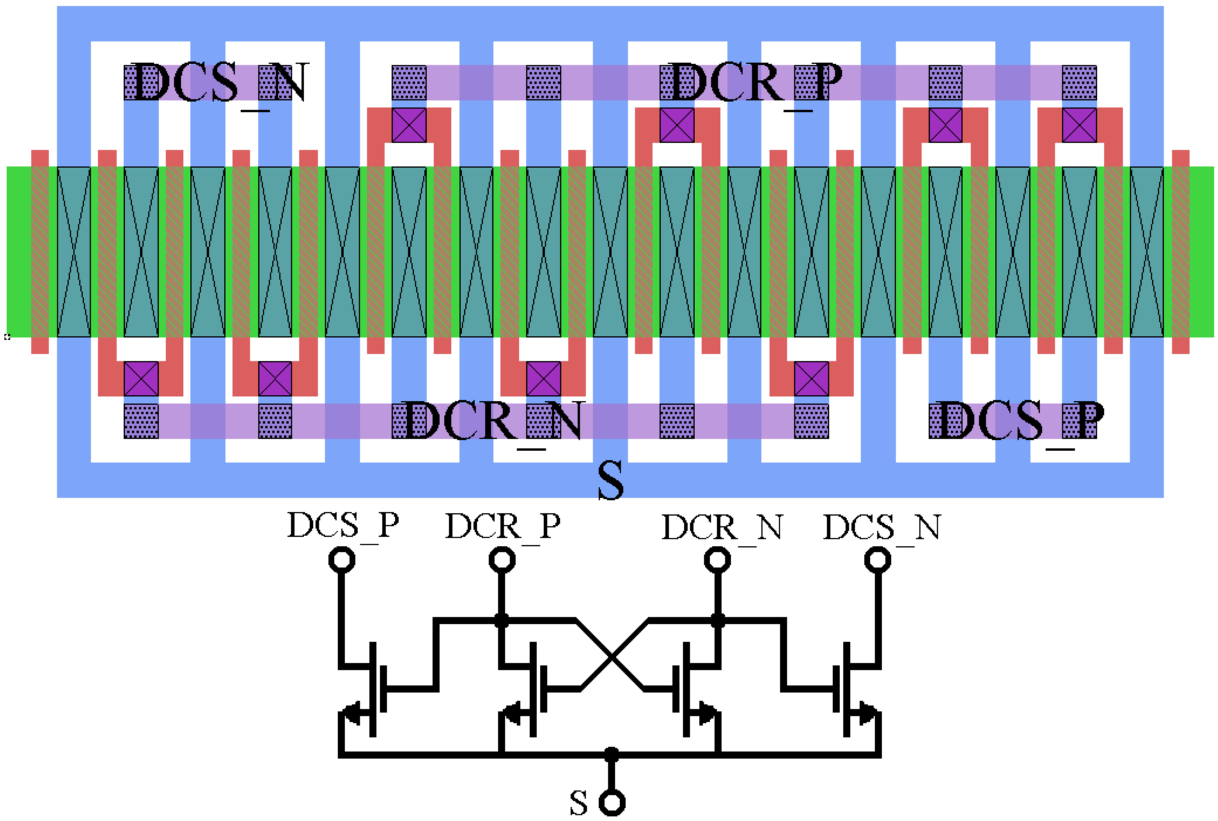


Colpitts VCO Layout

- Components are placed as close as possible to each other
- Merged varactor pair with shared n-well
- Transistor fingers narrow and contacted on both sides (not shown)
- Dummy gates on side to minimize variability due to STI-induced strain



Cross-Coupled VCO Layout
(K. Tang, et al CSICS-06)

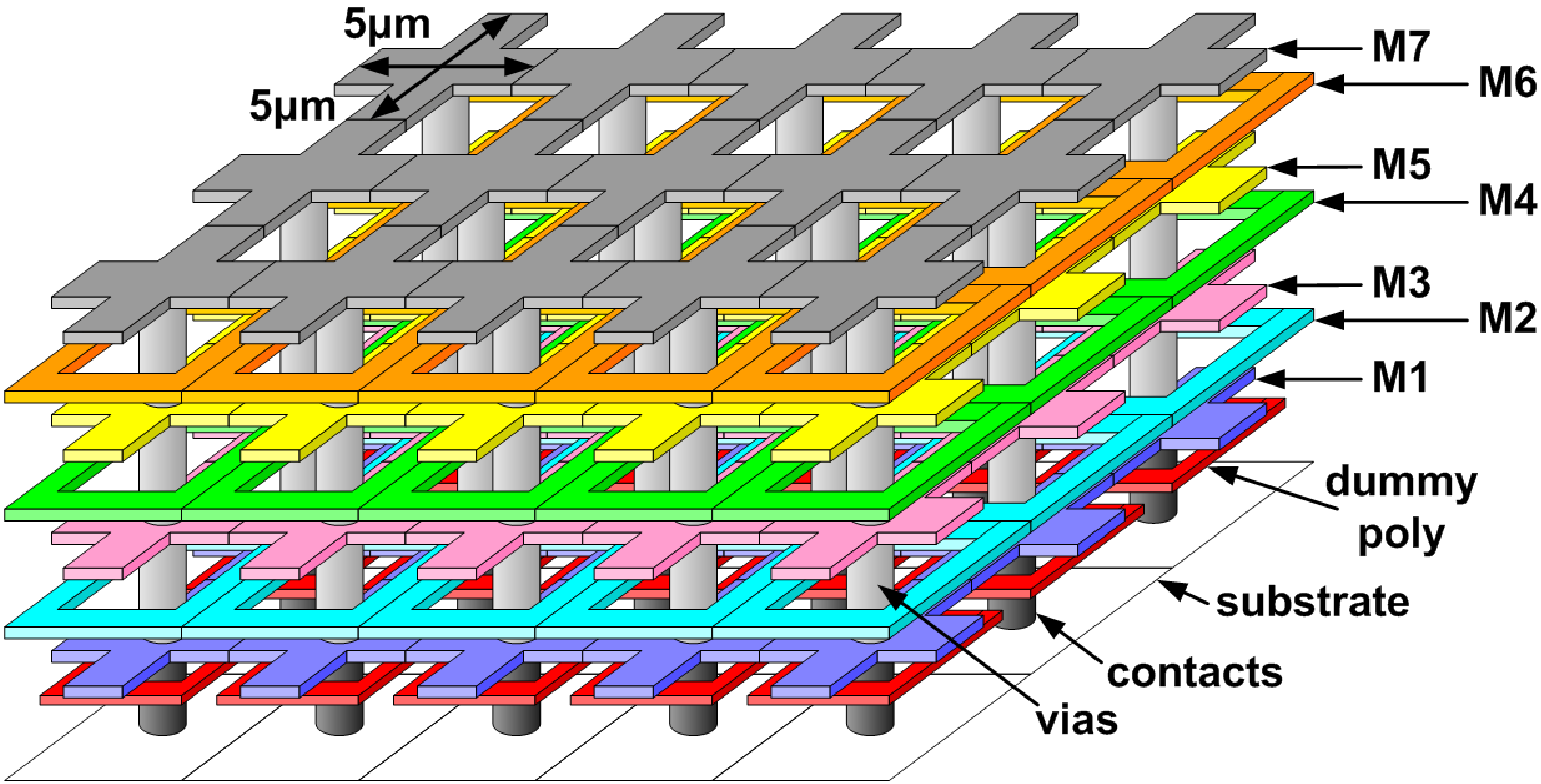


- Merged cross-coupled and buffer pair to minimize interconnect capacitance

Bias and ground distribution and decoupling

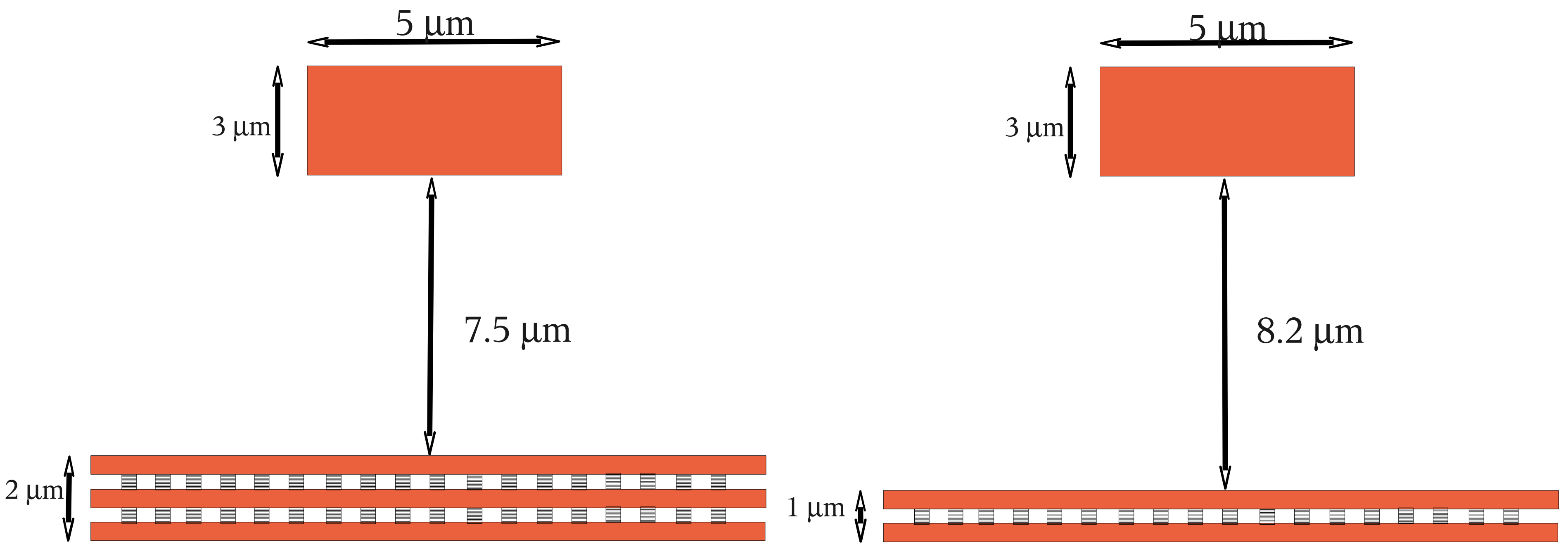
- Fine ground mesh with grounded substrate taps throughout the circuit
- At least two metals shunted together on ground mesh
- Distributed de-coupling of power supply mesh over ground mesh
- Local MIM (0.5pF - 1pF) de-coupling to ground if available
- Careful with MOM caps to ensure high Q
- 45 degree angles no longer allowed in 45nm

Bias Distribution (E. Laskin, ISSCC-08)

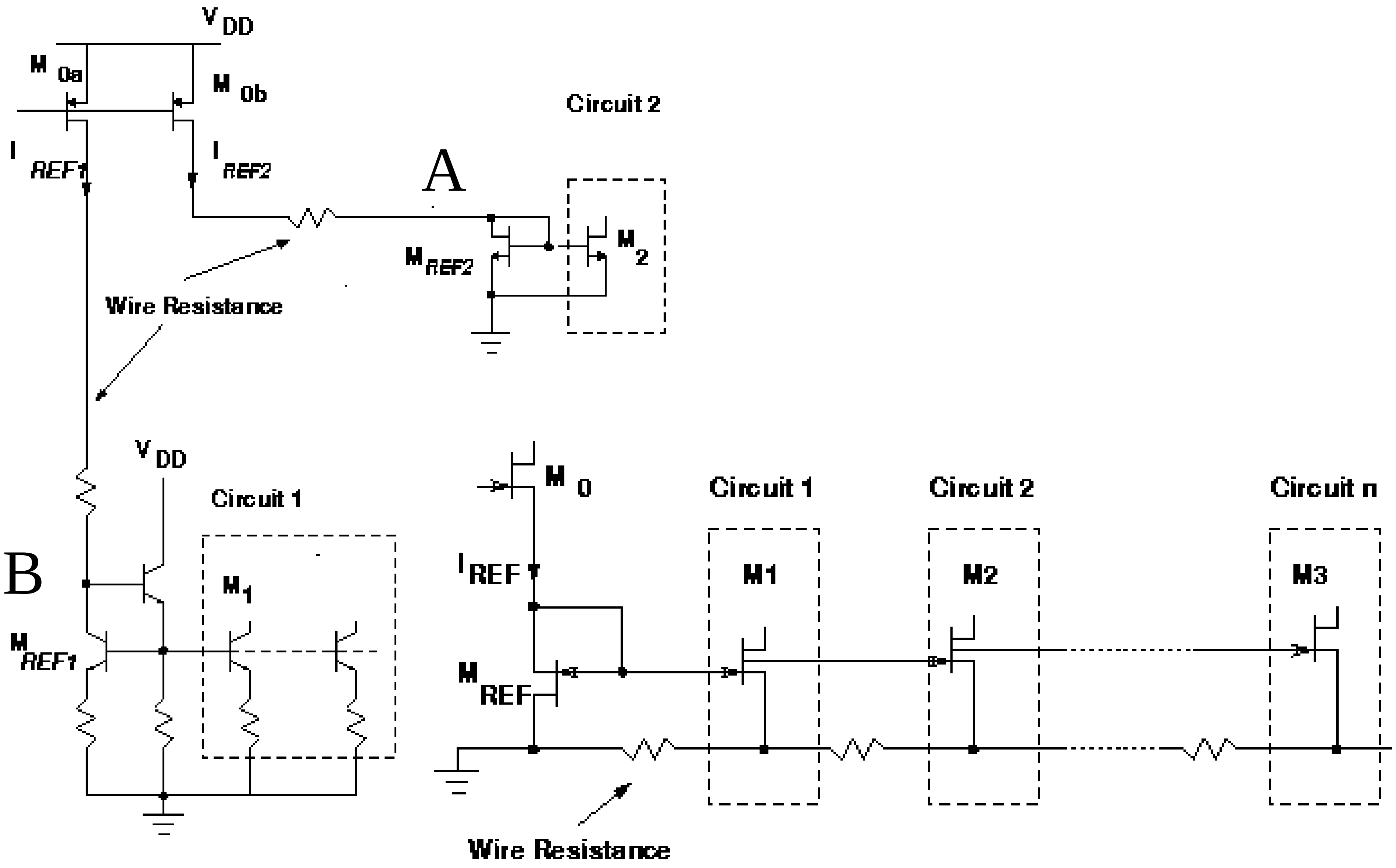


- Metal mesh distributes ground, V_{DD}, bias to all cells
- Substrate contacts, distributed decoupling, low R, L
- Meets all density rules

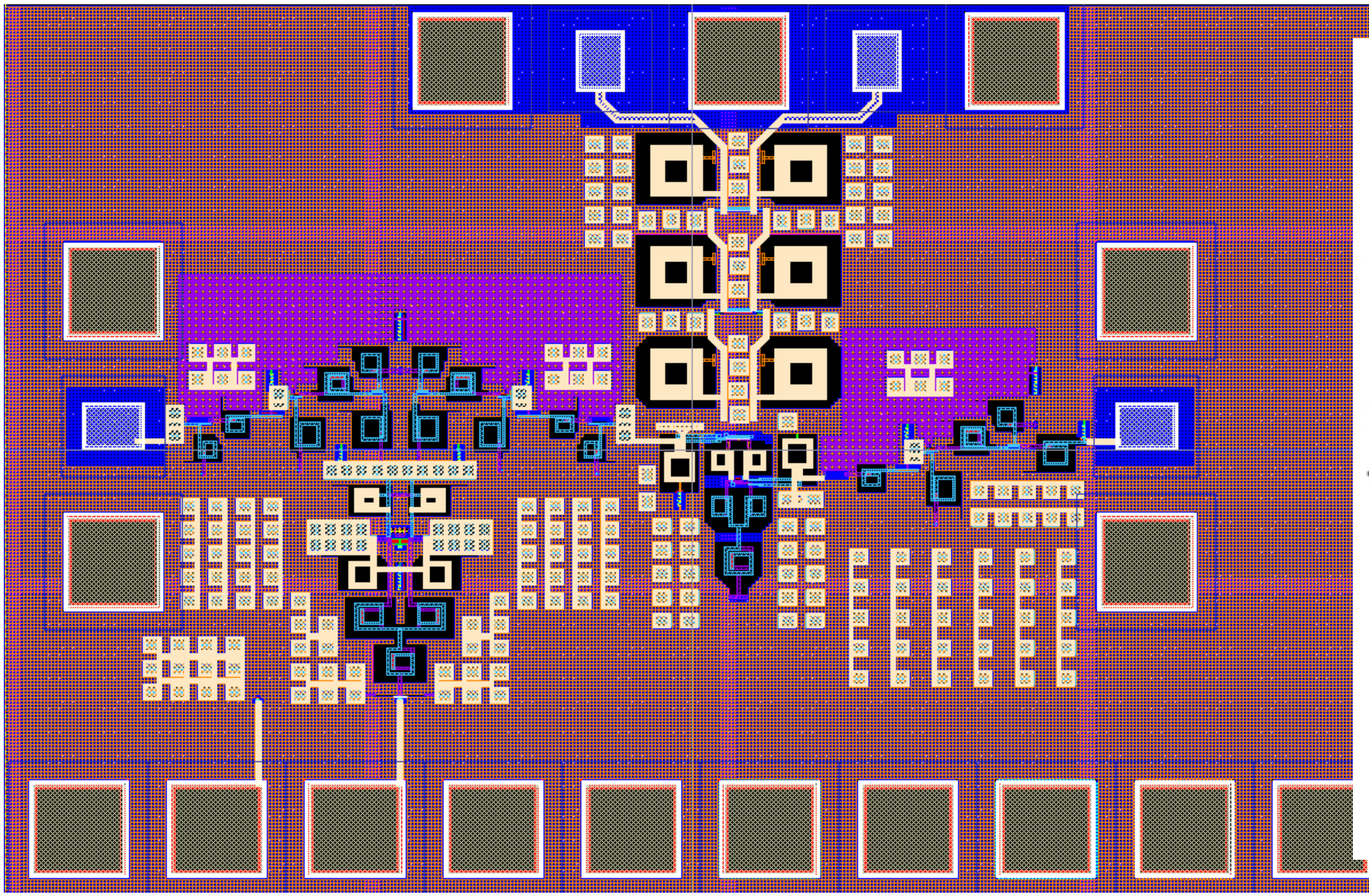
Signal distribution : t-line groundplane loss

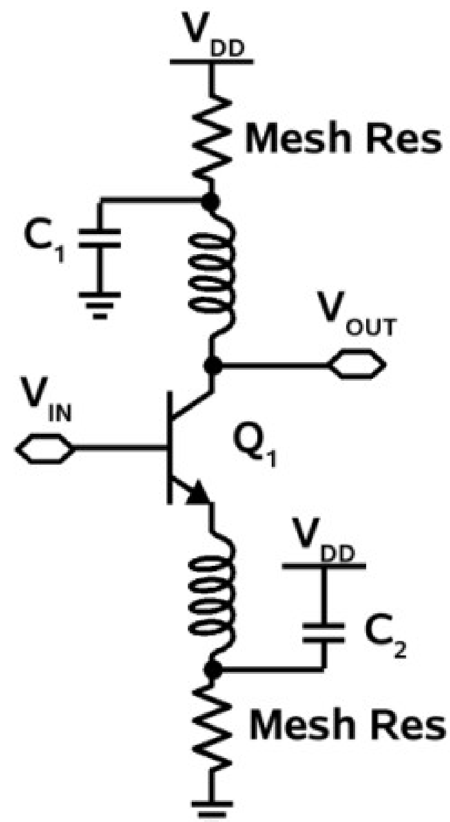


Local supply distribution and de-coupling

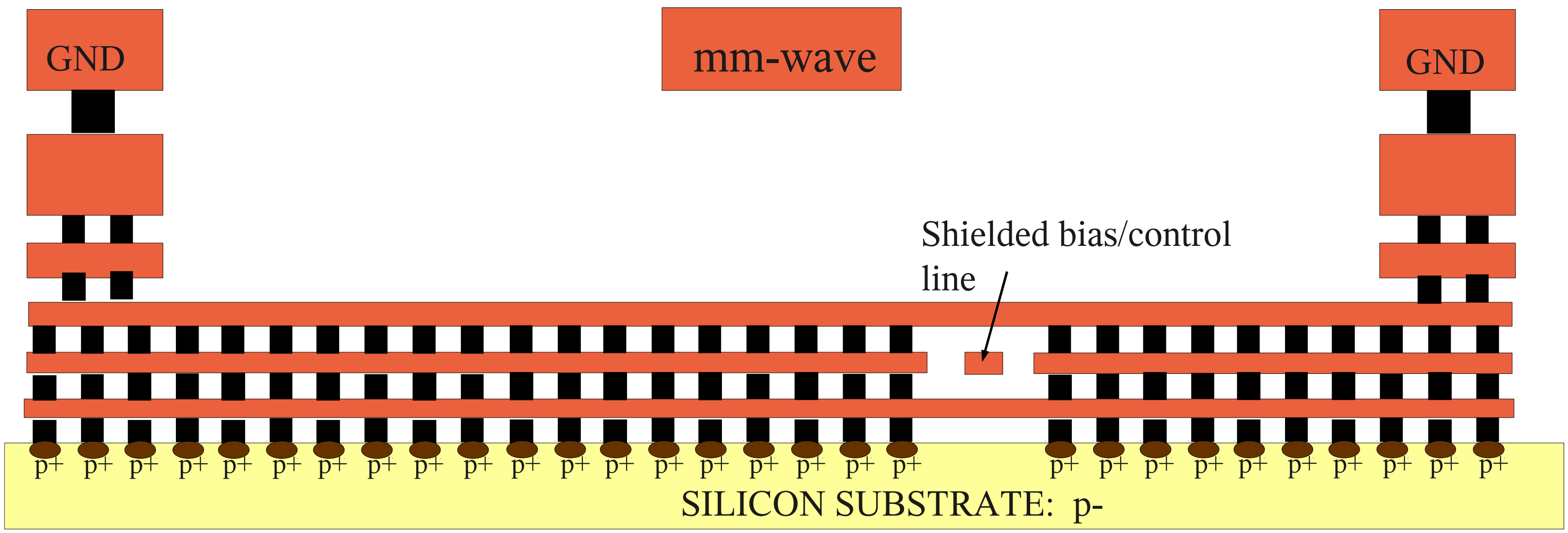


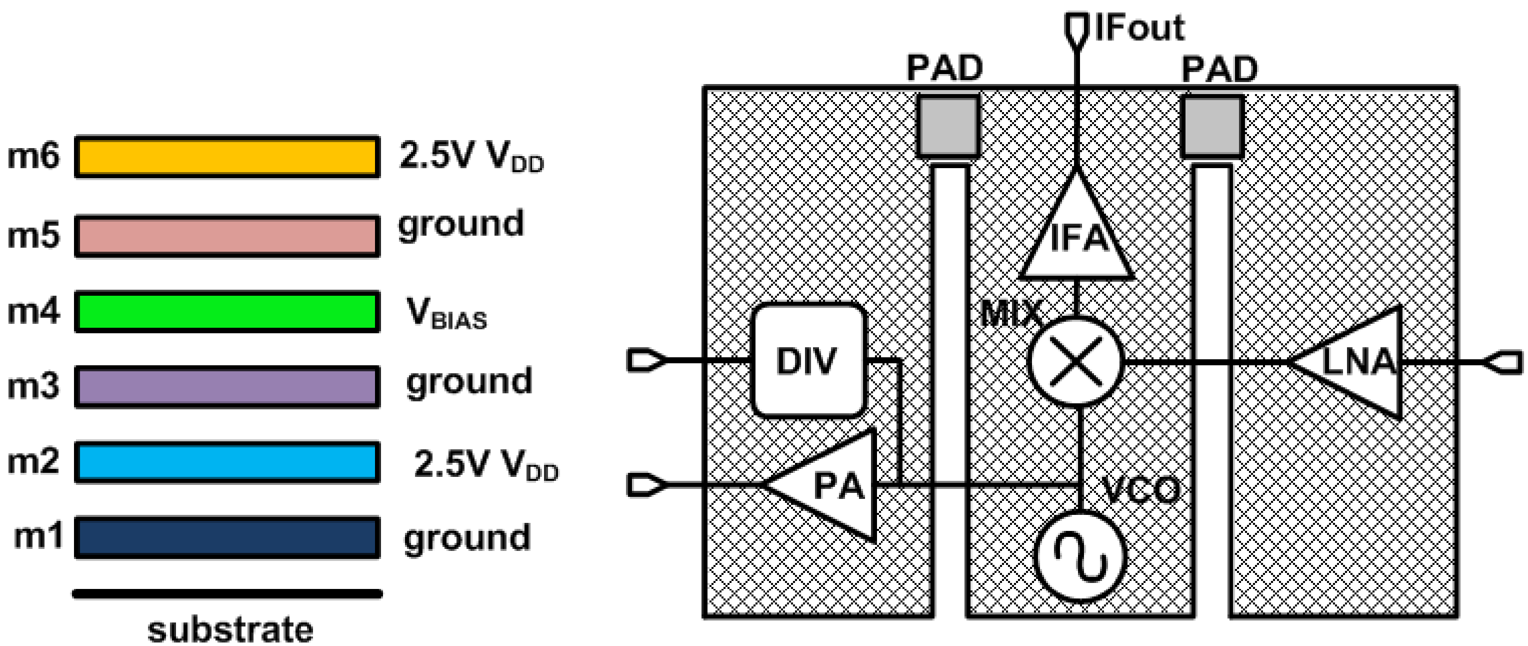
Bias de-coupling in 100-GHz transceiver





Signal and block-to-block isolation strategies

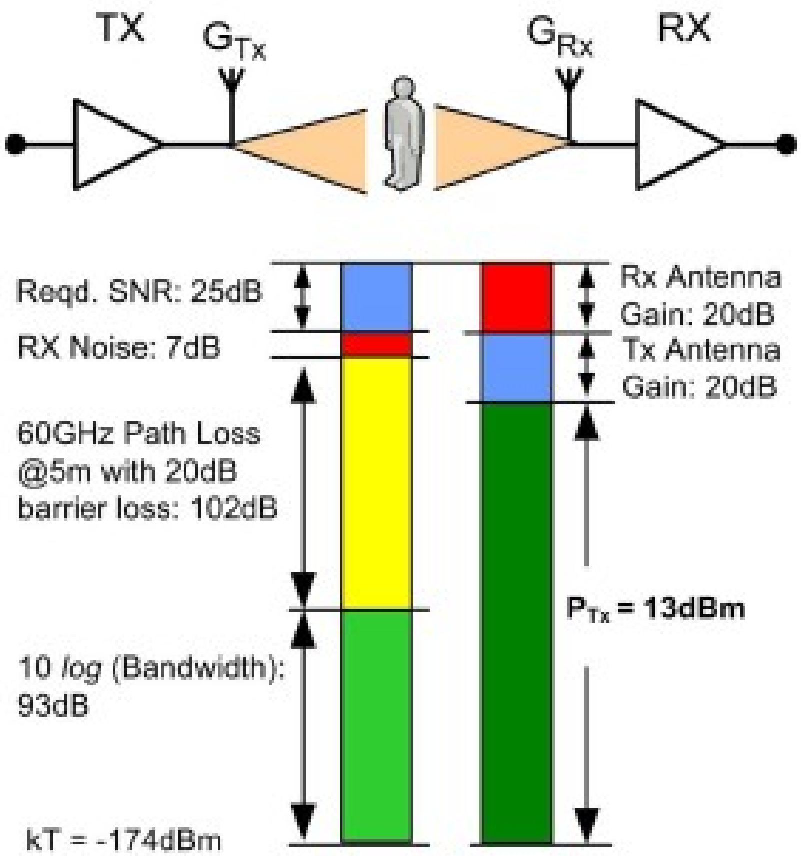




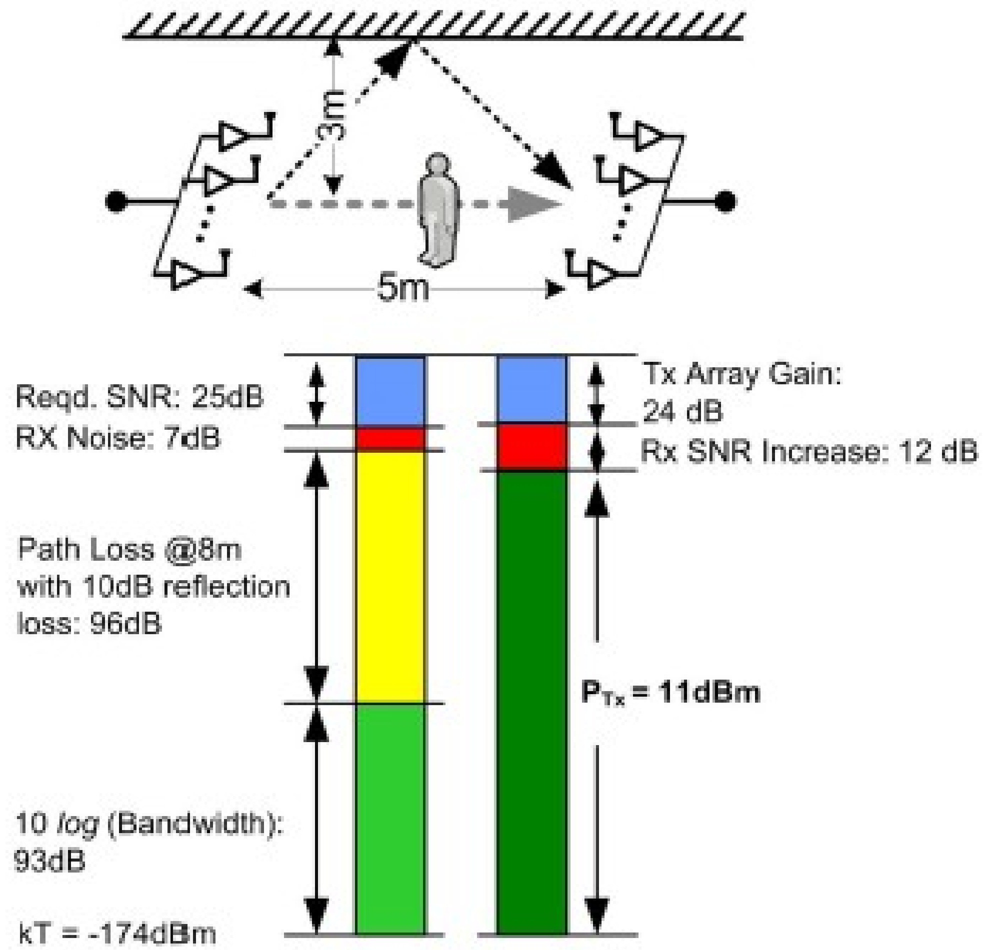
Mm-wave transceiver examples

- 60-GHz CMOS and SiGe BiCMOS wireless phased arrays
- 77-GHz SiGe BiCMOS automotive radar transceiver
- 70-80 GHz SiGe BiCMOS active imaging array with digital beamforming
- 140 to 170-GHz SiGe BiCMOS sensor transceivers with on-die BIST and antennas

60-GHz 1.5-5 Gb/s wireless links

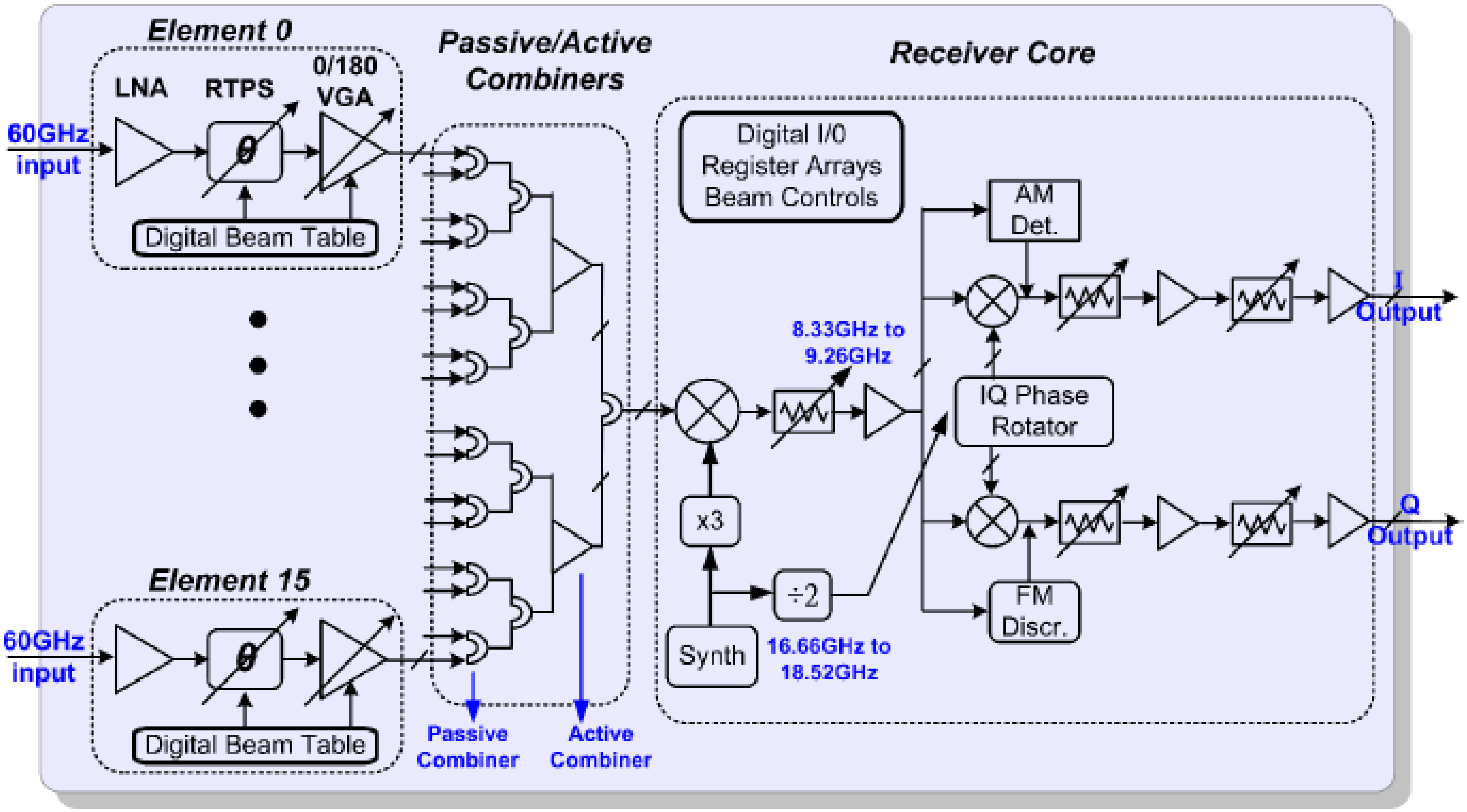


Single-element with high-gain antenna

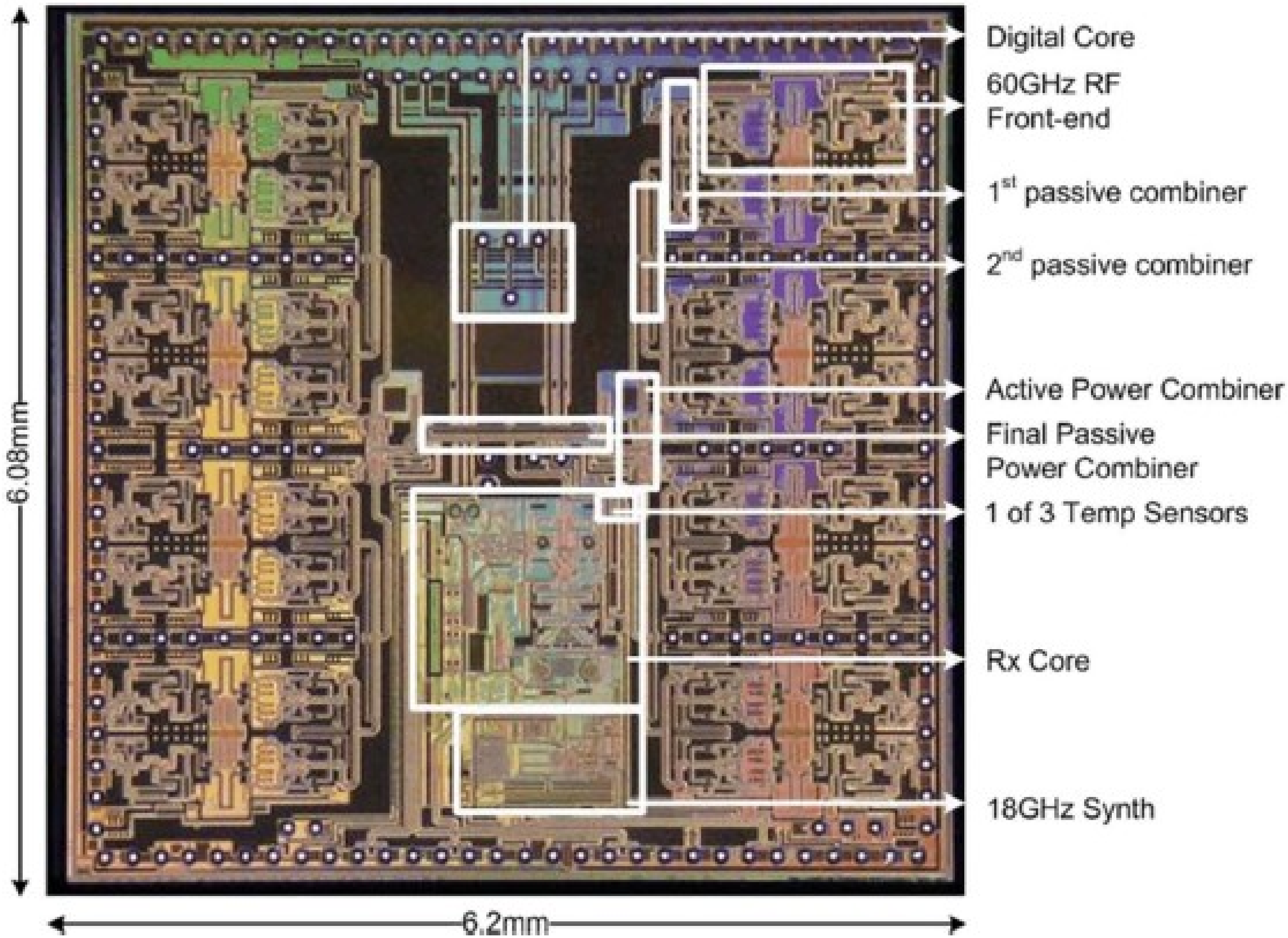


Phased-array Rx and Tx – using reflectors to establish wireless link

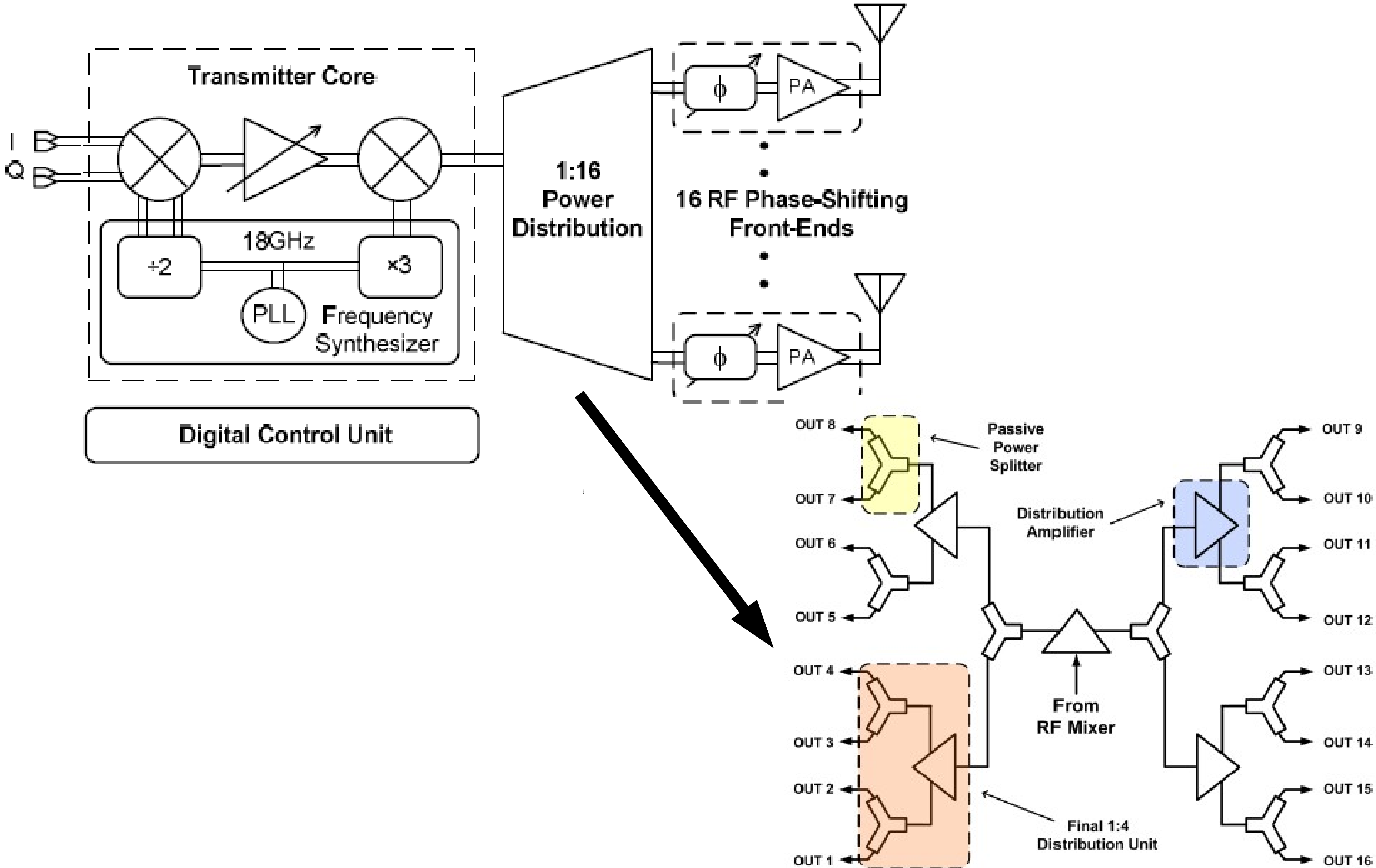
SiGe BiCMOS 60-GHz phased array receiver



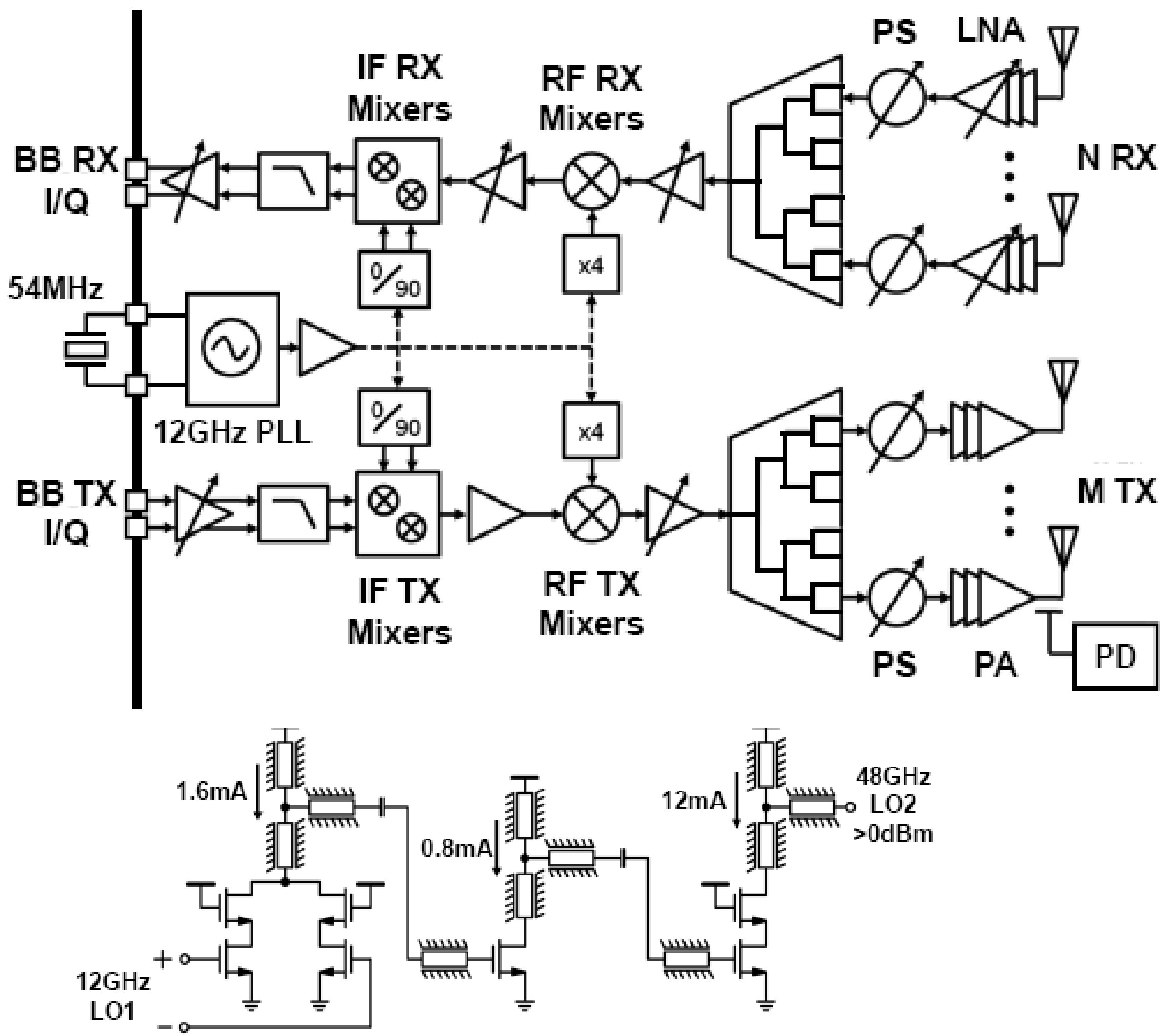
SiGe BiCMOS 60-GHz phased array receiver



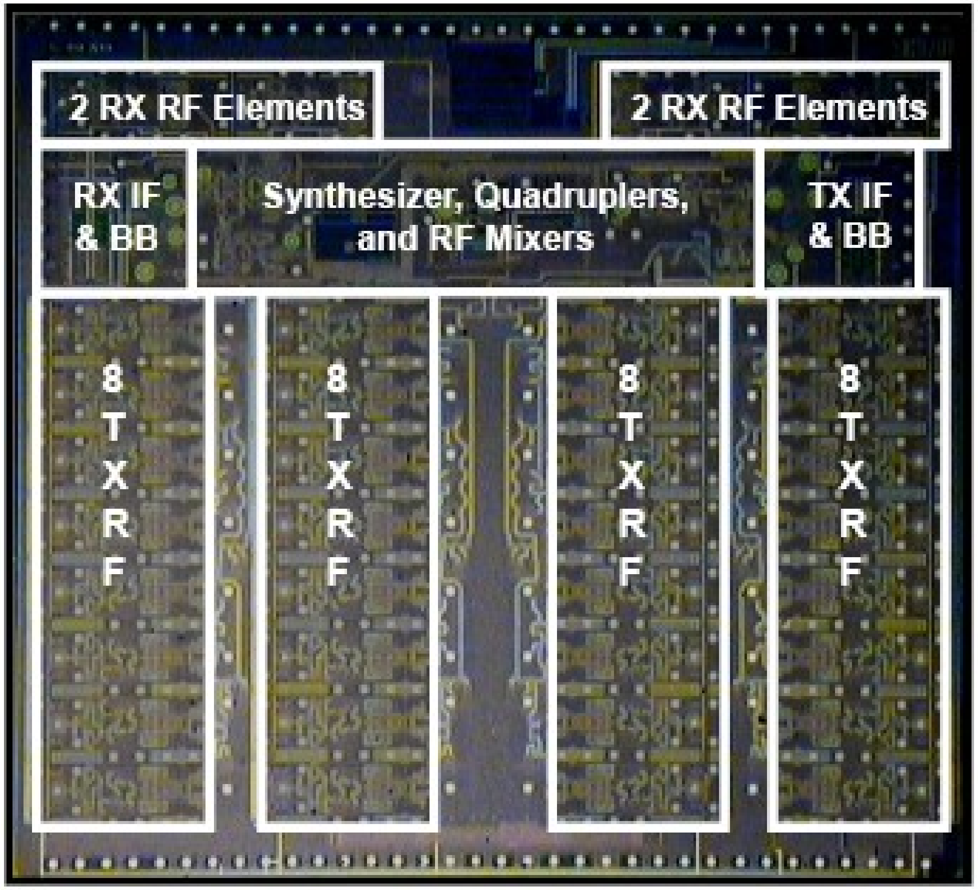
SiGe BiCMOS 60-GHz phased array transmitter

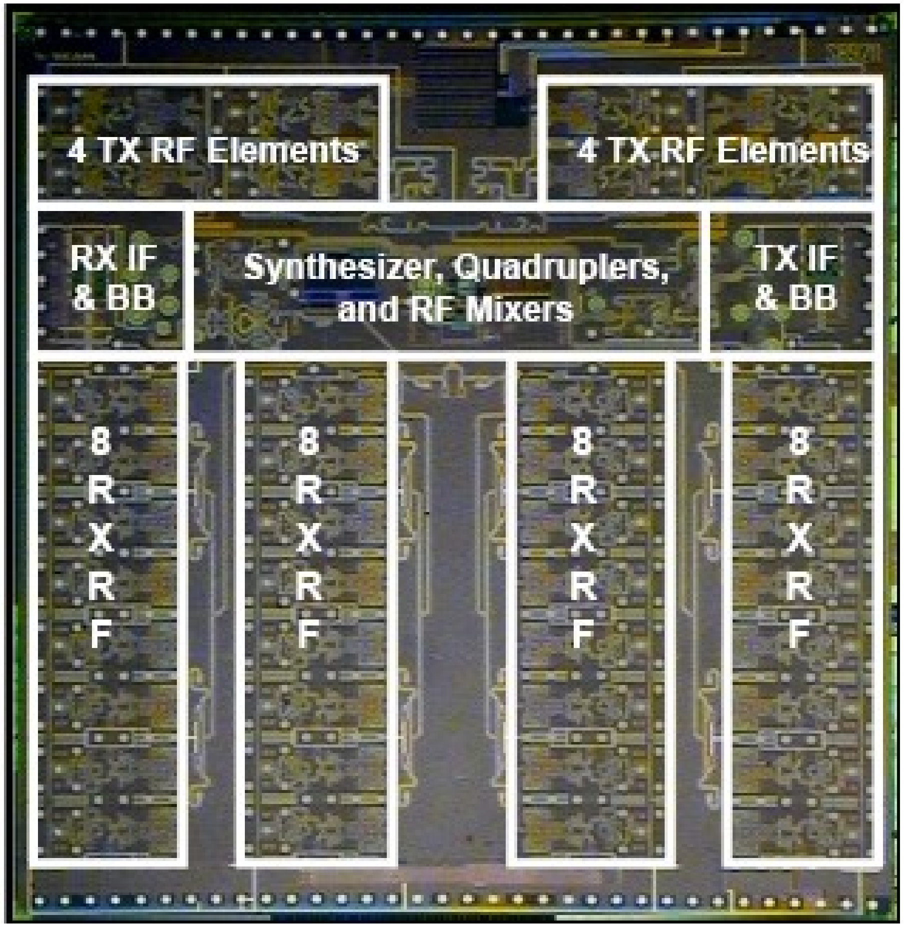


65-nm CMOS 60-GHz receiver phased array



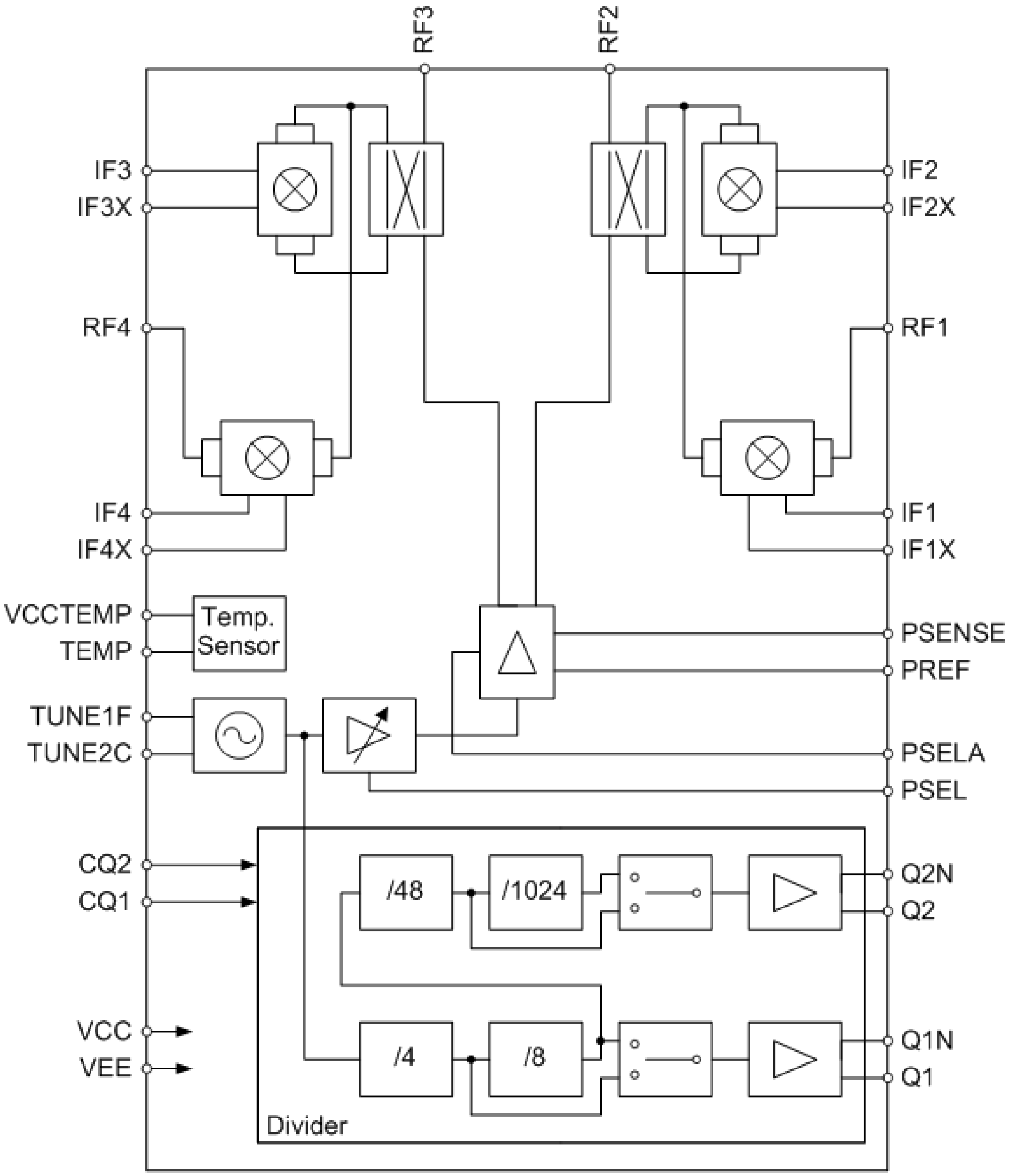
65-nm CMOS 60-GHz receiver phased array

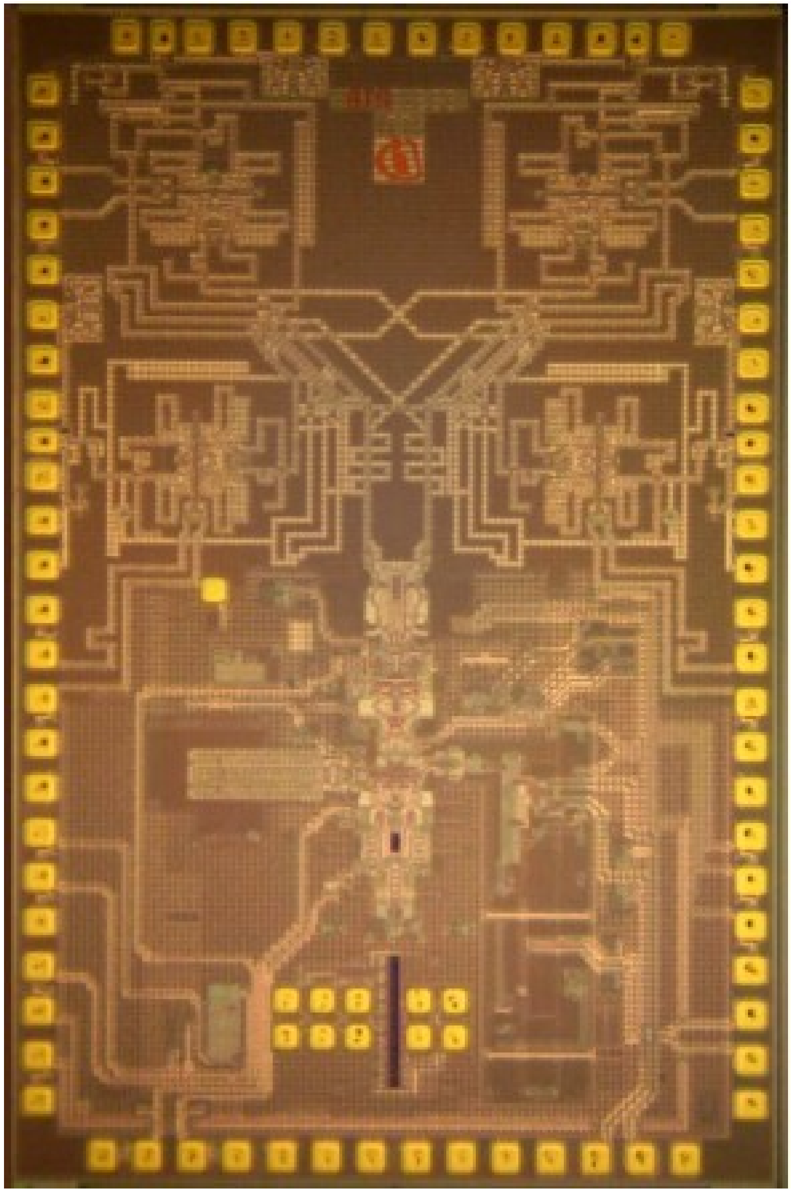




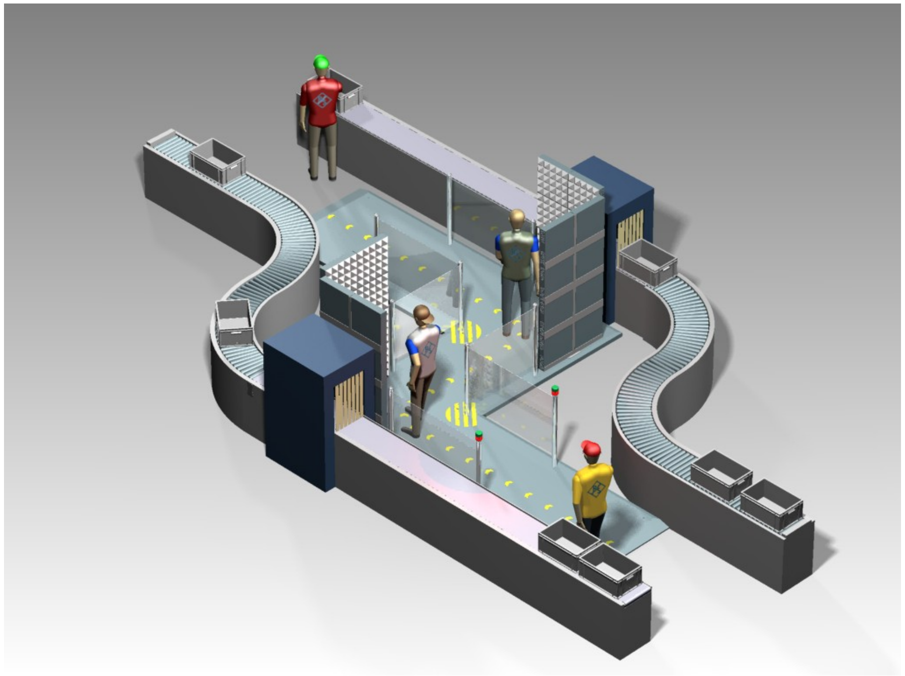
77-GHz Automotive Radar

[5]

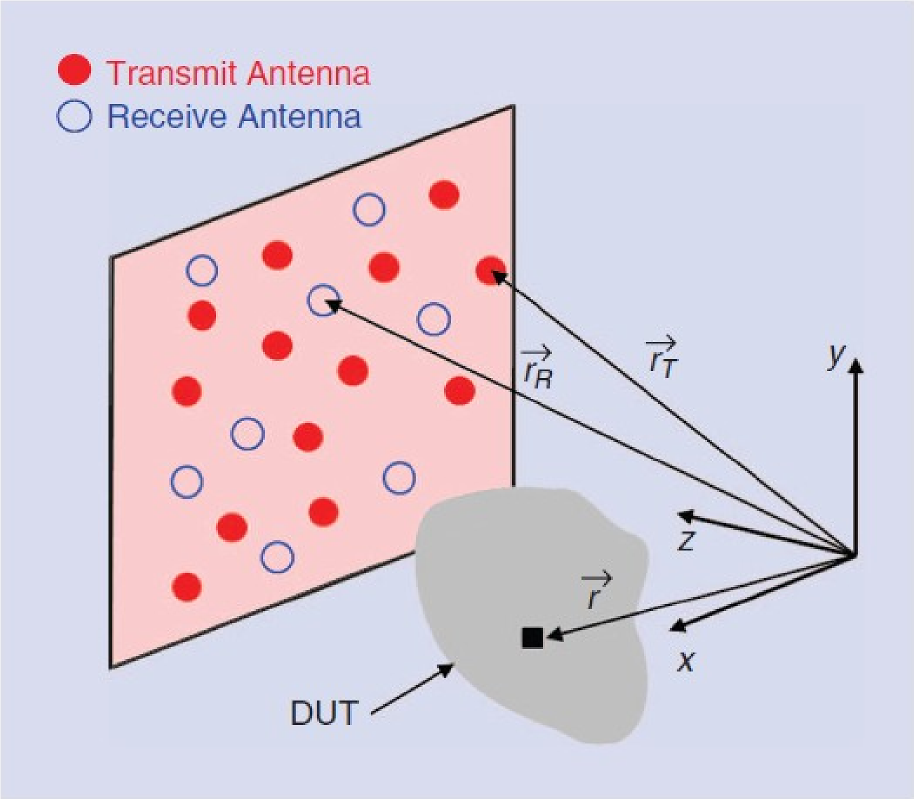




W-Band active imaging array with digital beamforming

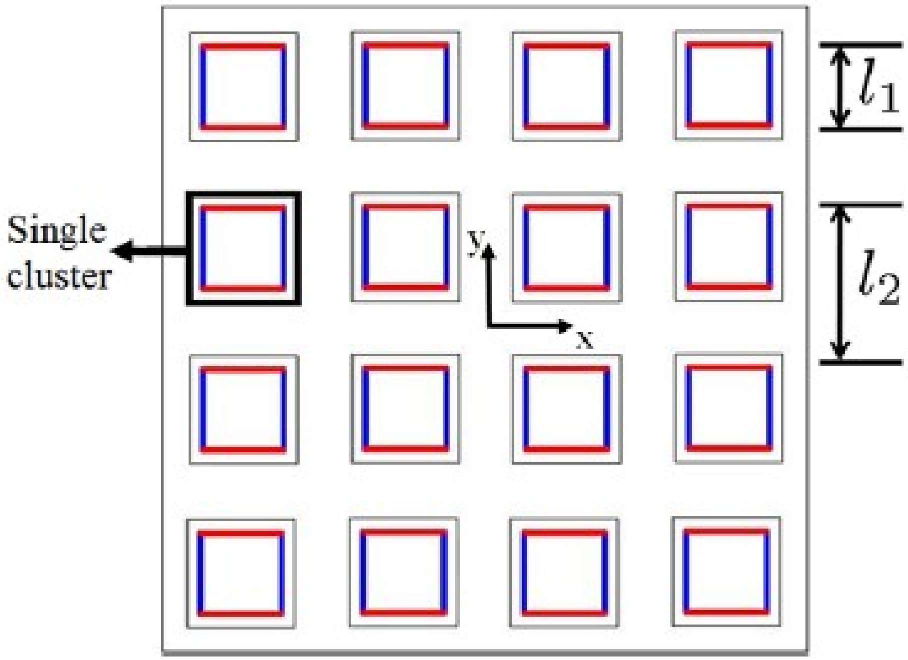


[7]



[S.S. Ahmed et al, IEEE Microwave Magazine October 2012]

Antenna array clusters



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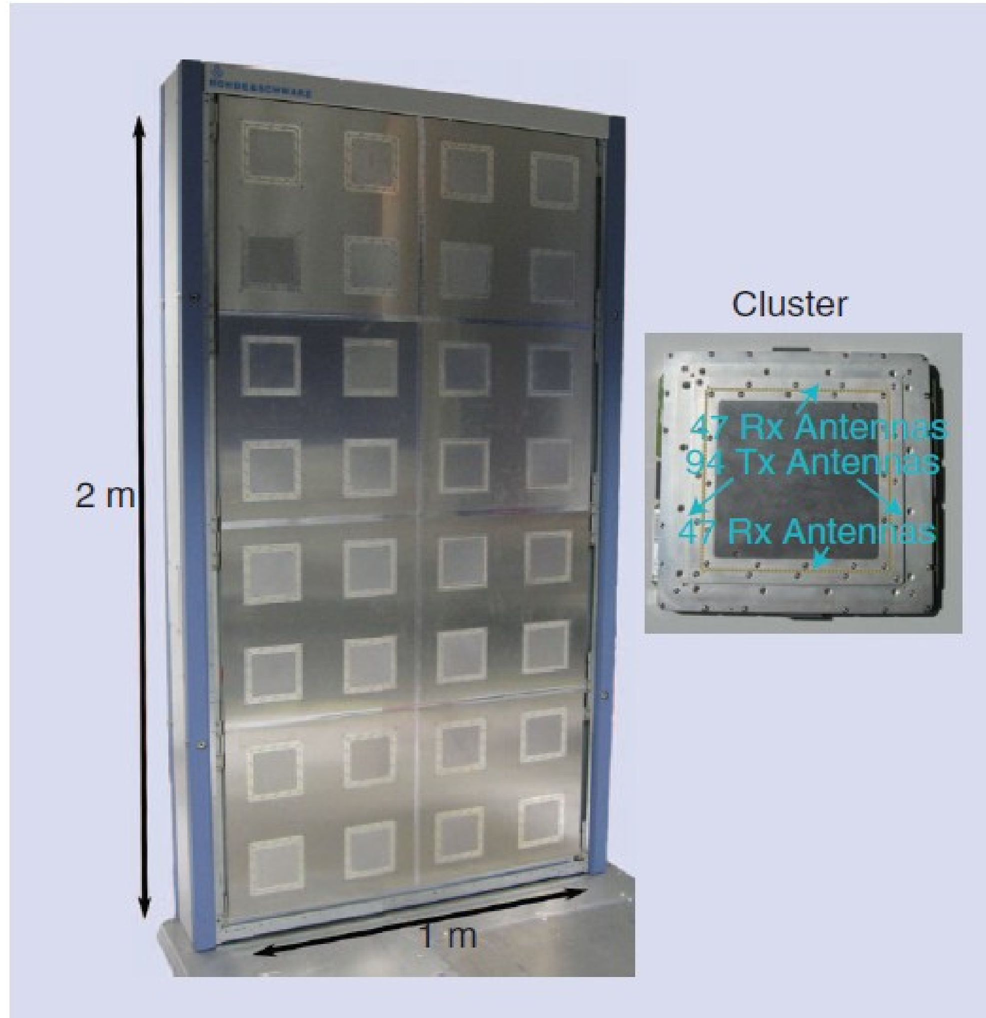
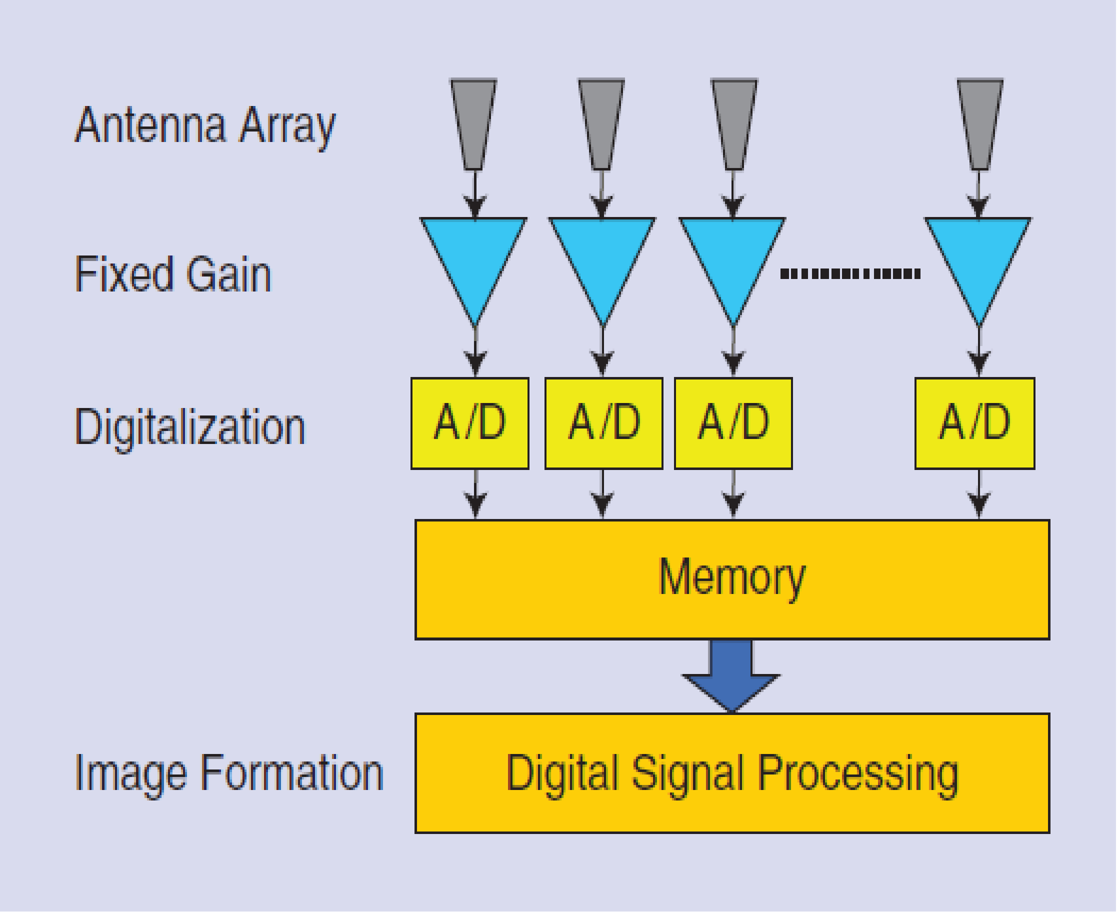


Figure 11. *Photograph of QPASS system (without cover) [55]. On the right, a cluster unit is shown [55].*

[S.S. Ahmed et al, IEEE Microwave Magazine October 2012]

Digital beamforming array concept



[S.S. Ahmed et al, IEEE Microwave Magazine October 2012]

Blcok diagram of single array

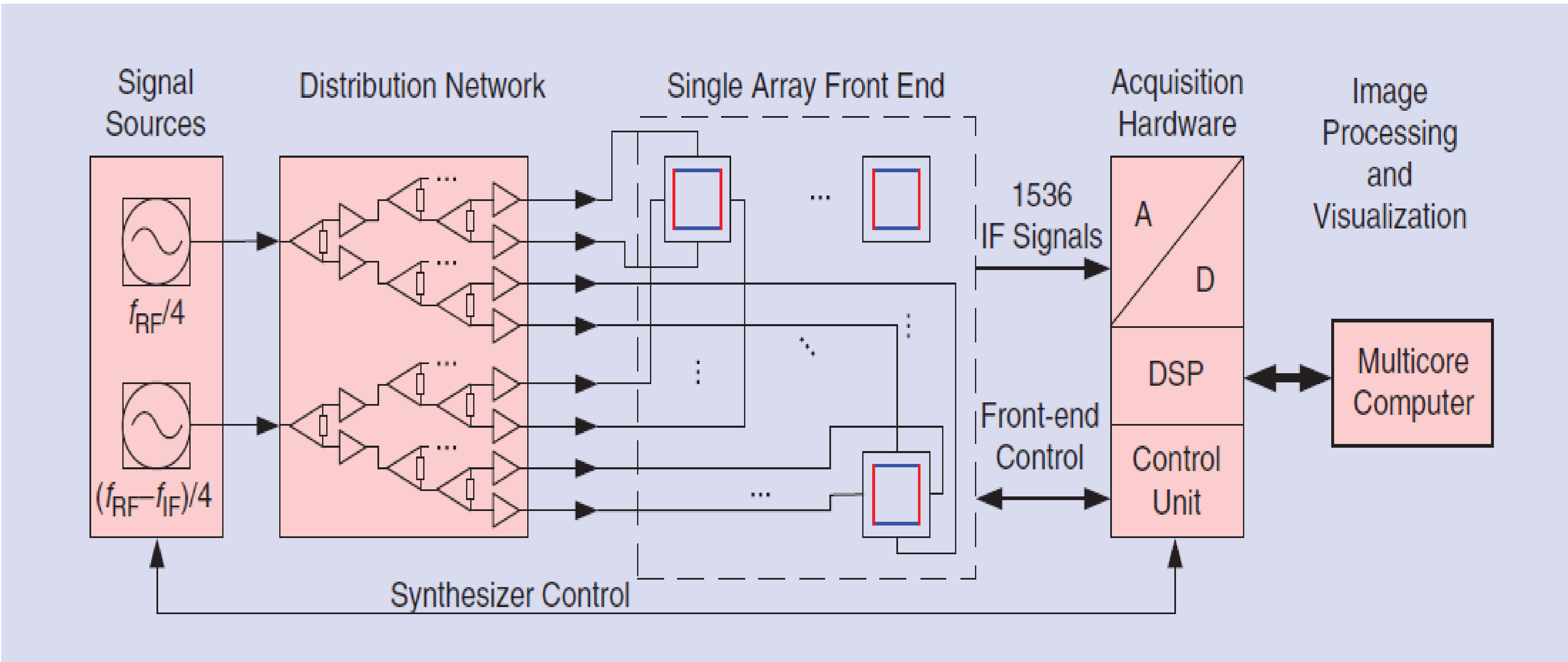
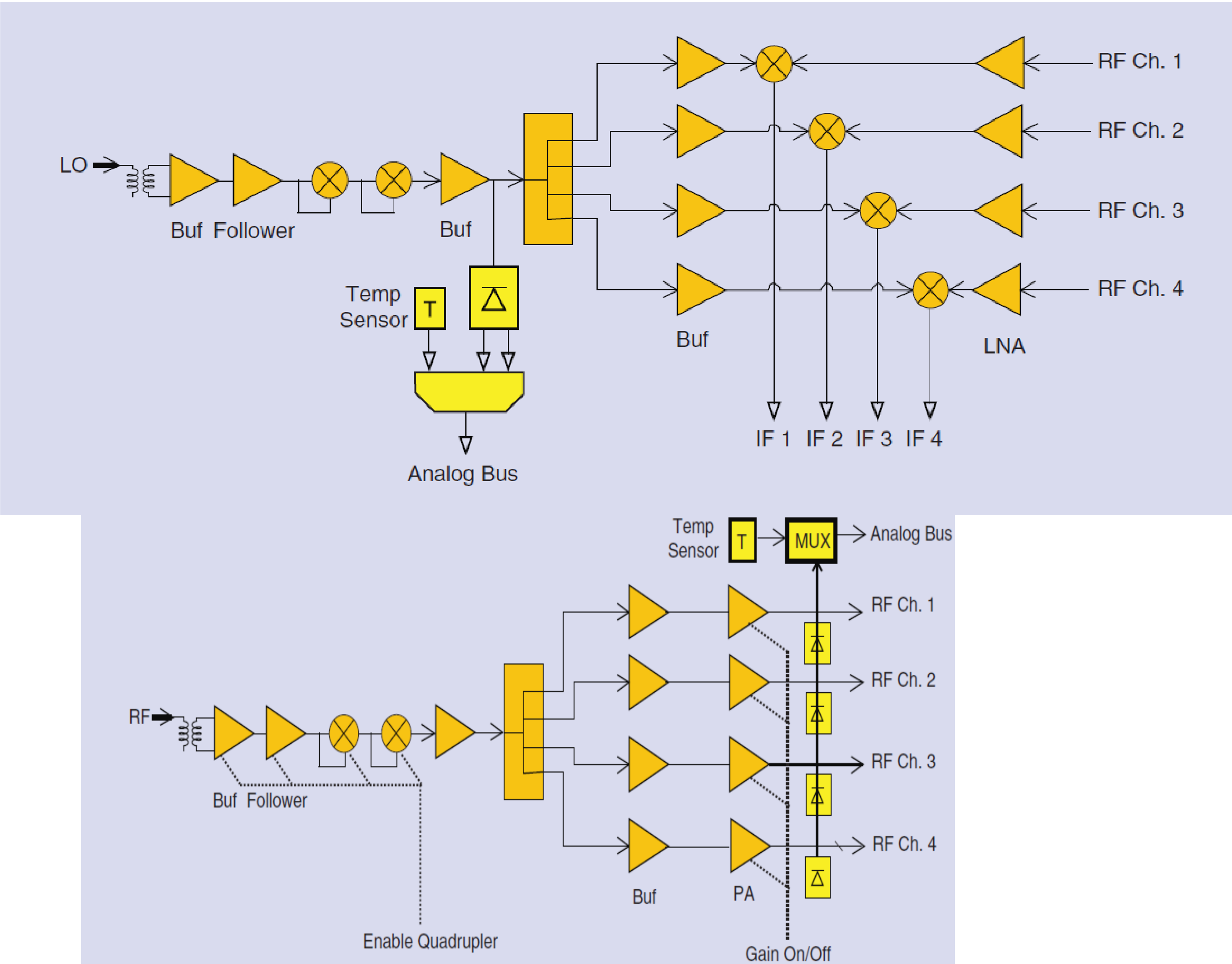


Figure 12. *System block diagram of a single array.*

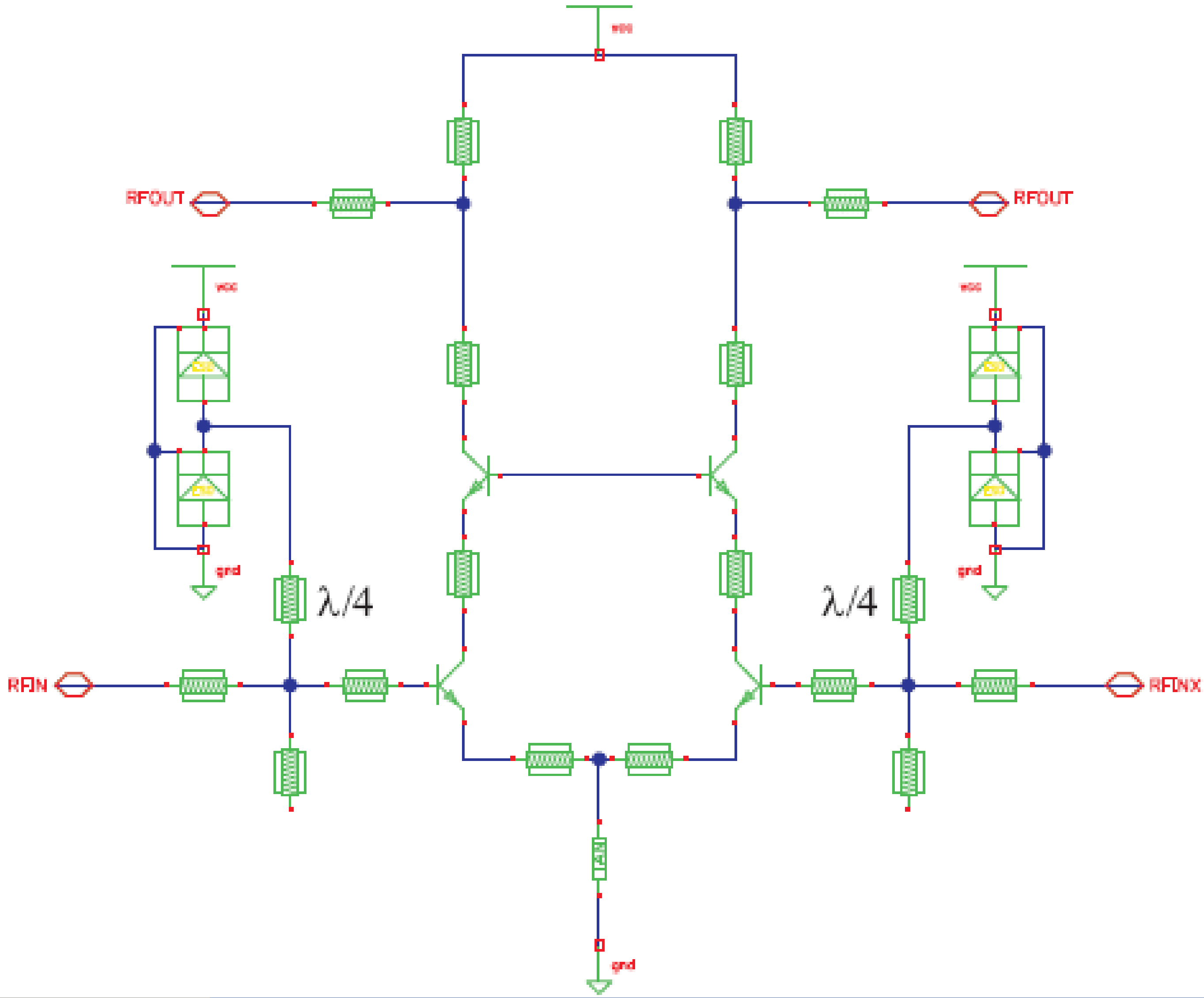
[S.S. Ahmed et al, IEEE Microwave Magazine October 2012]

RX and TX array elements



[7]

Differential LNA with ESD protection



Chip packaging

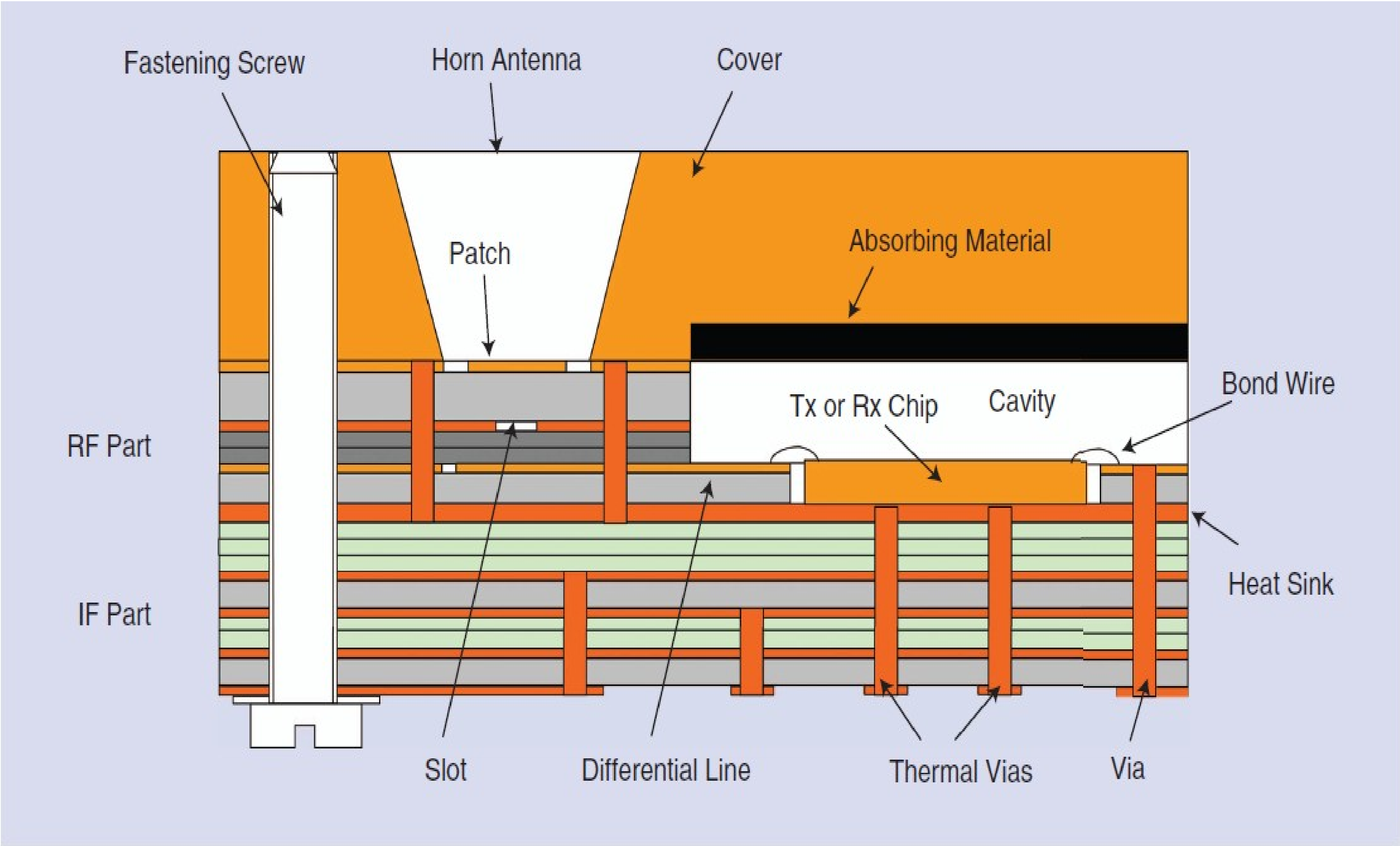
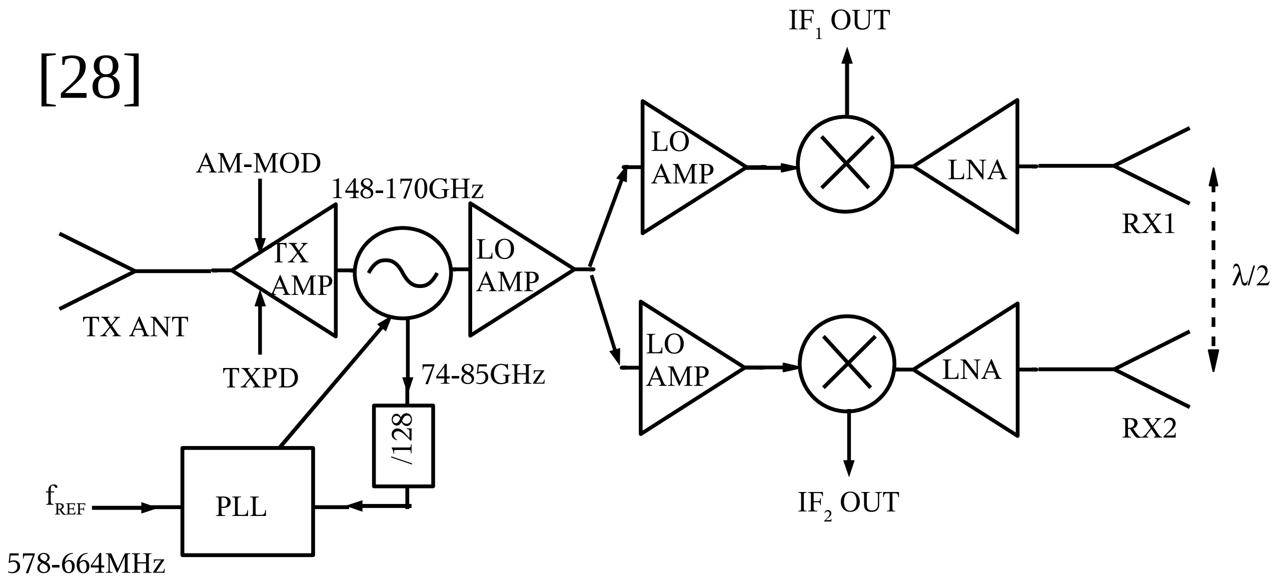
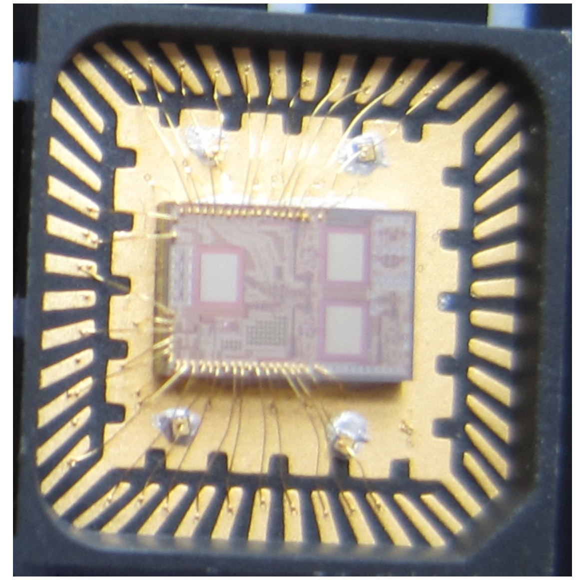


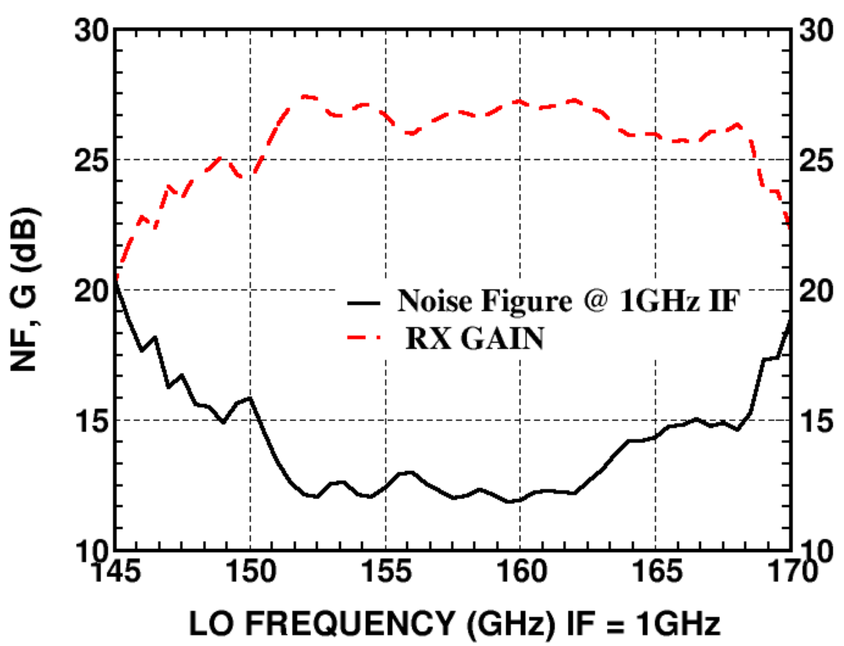
Figure 13. *Cut view of the multilayer PCB illustrating the integration of MMIC and the antenna structure inside the housing of the cluster.*

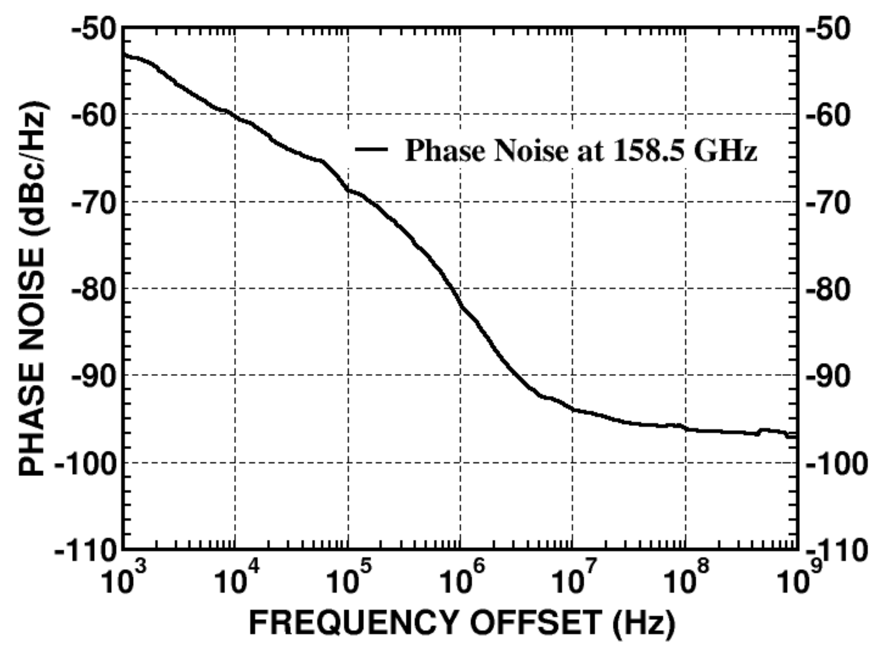
Push-push 150-170GHz Doppler transceiver

[28]

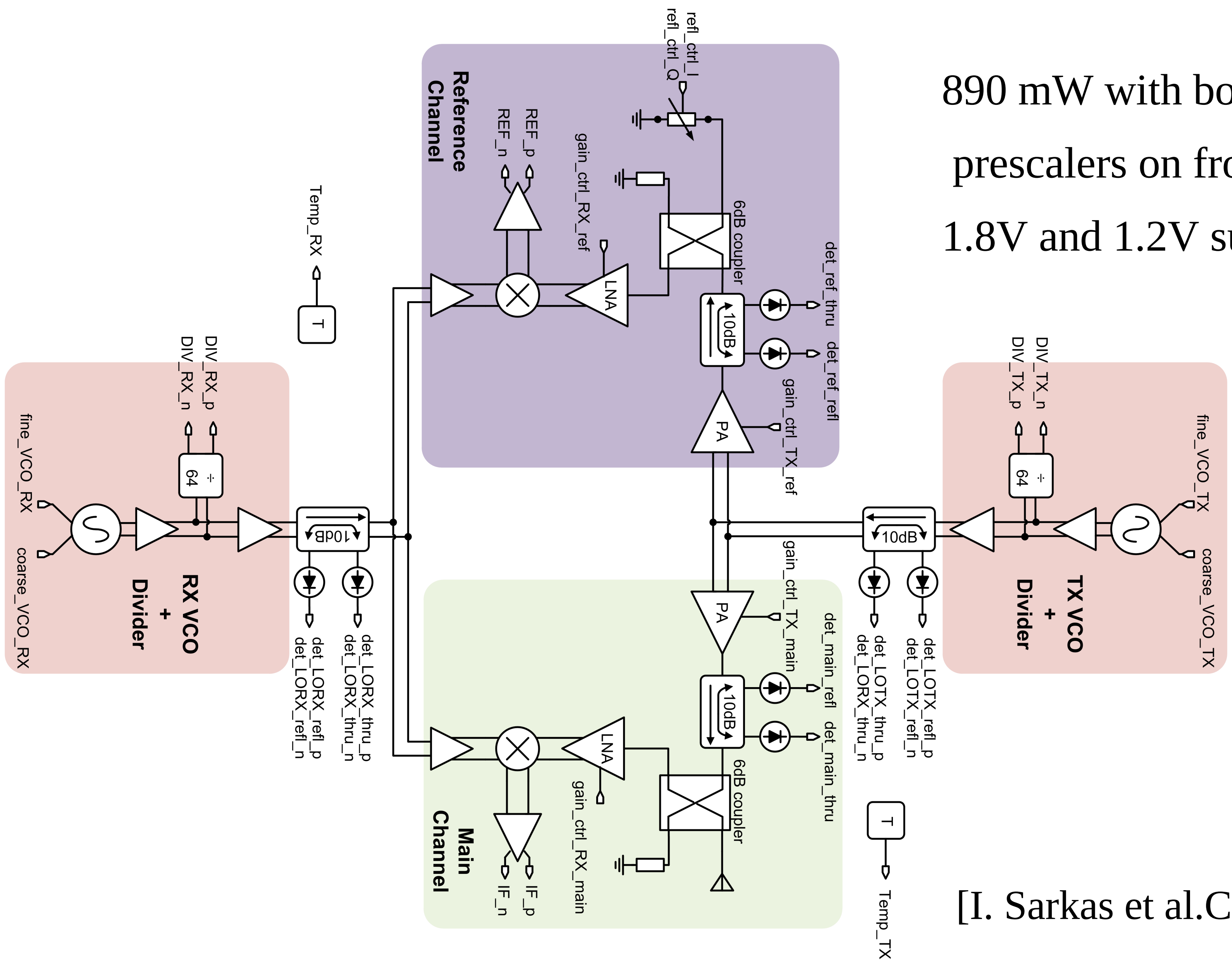








Monostatic 120/150 GHz distance sensors



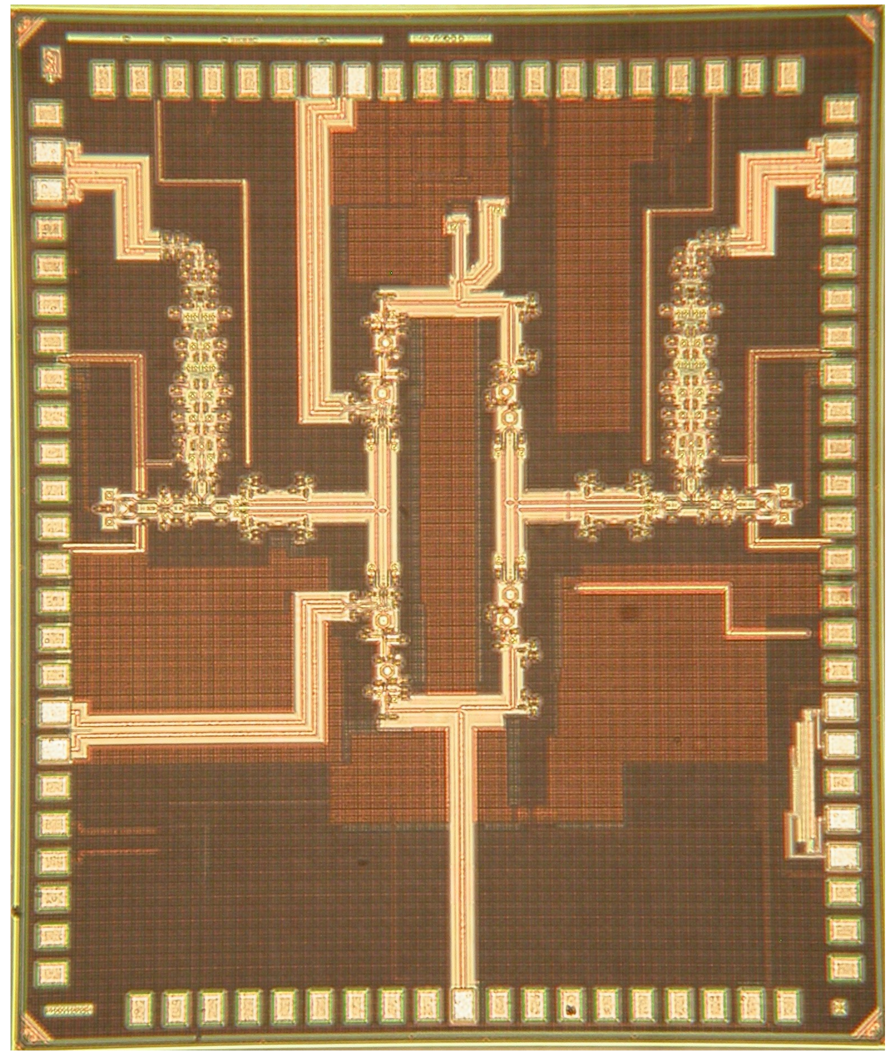
890 mW with both prescalers on from 1.8V and 1.2V supplies

[I. Sarkas et al.CSICS 2012]

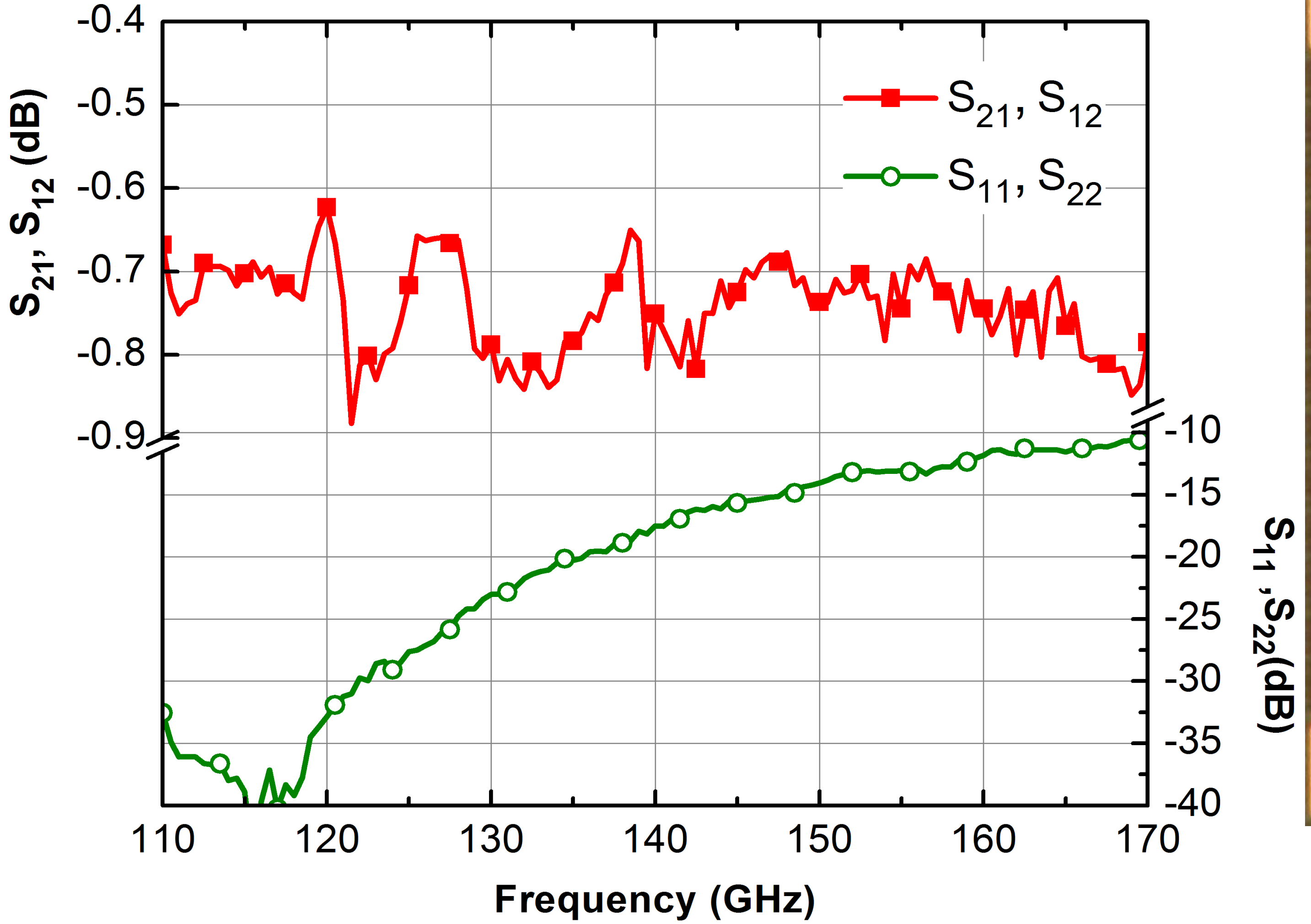
Layout and performance summary

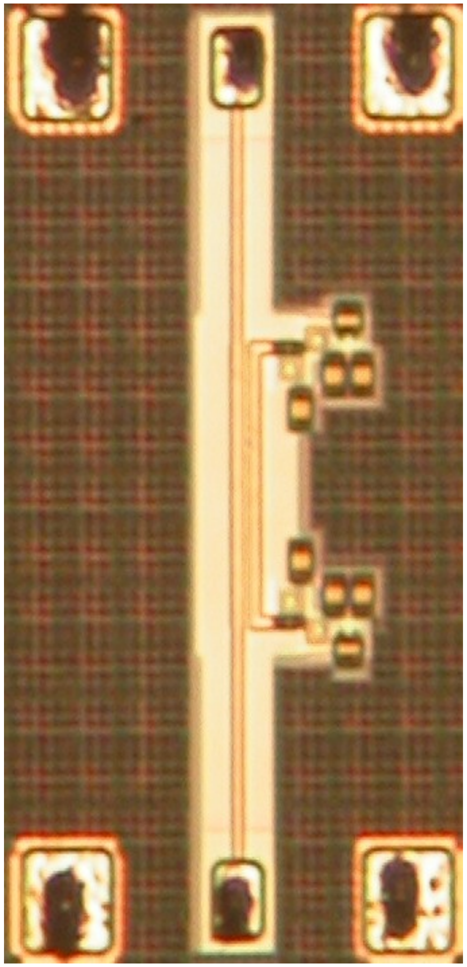
- 130nm SiGe BiCMOS technology, HBT f_T/f_{MAX}= 230/280 GHz
- Tuning range 143-152 GHz
- NF<10 dB, P_{out} >-6 dBm
- PN < -83 dBc/Hz at 1MHz
- P_{DC} = 800 mW

2.6mm×2.3mm

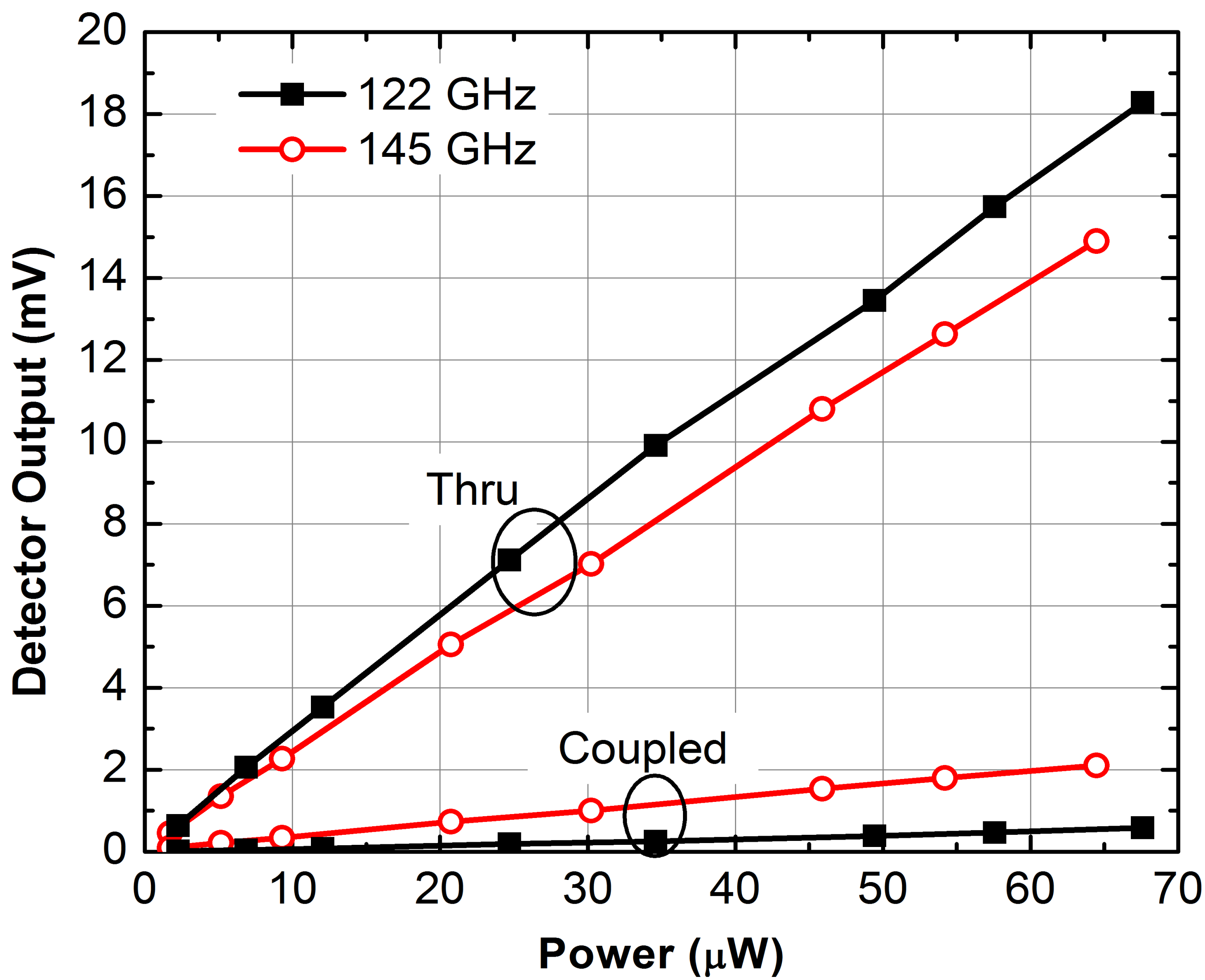


Coupler with detectors

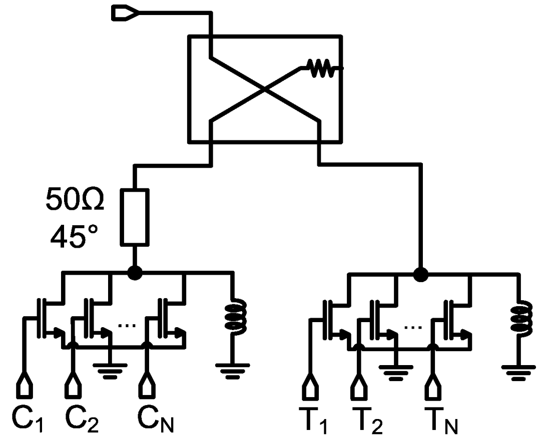


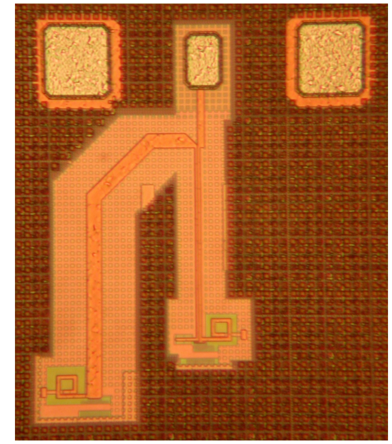


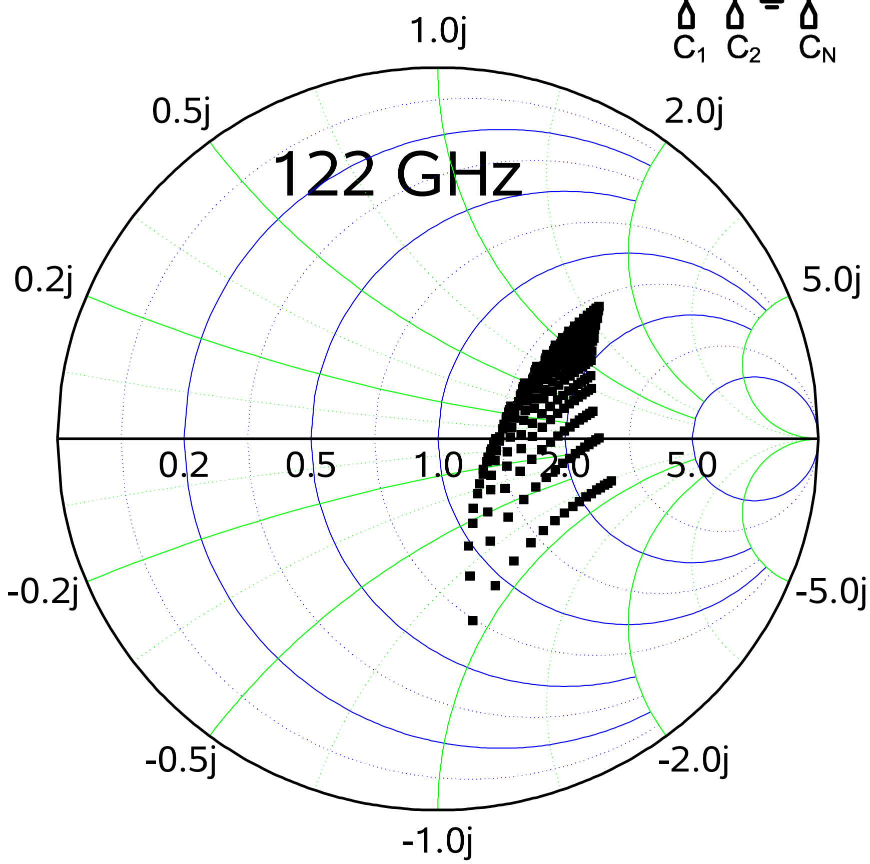
Coupler with detectors: Linearity

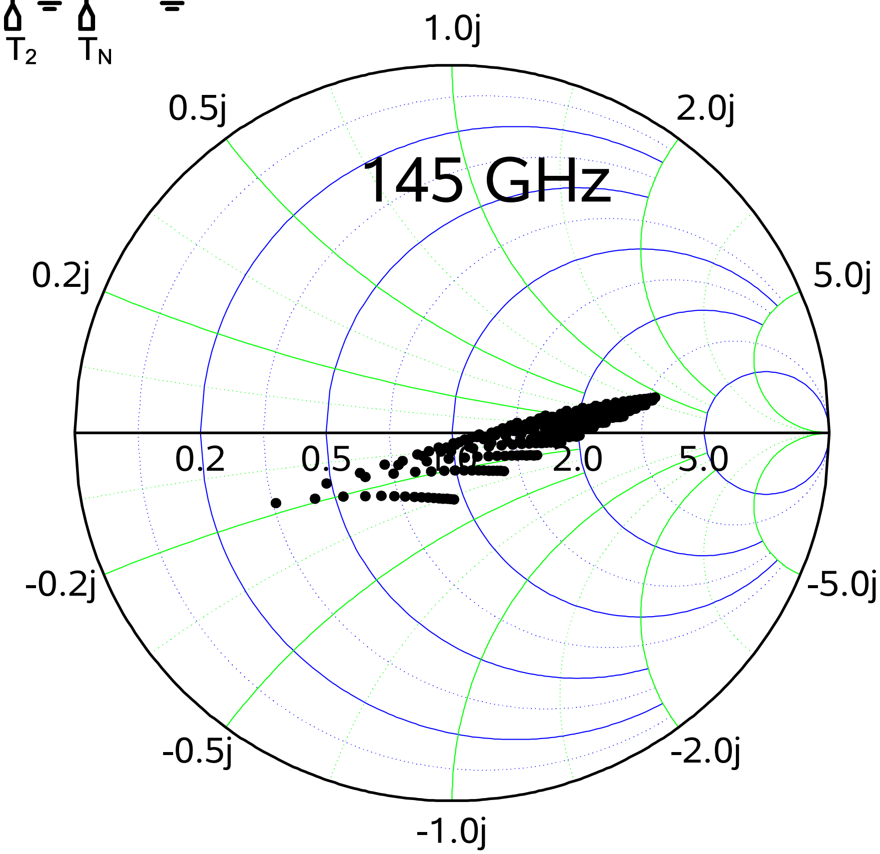


Digital Tuner States

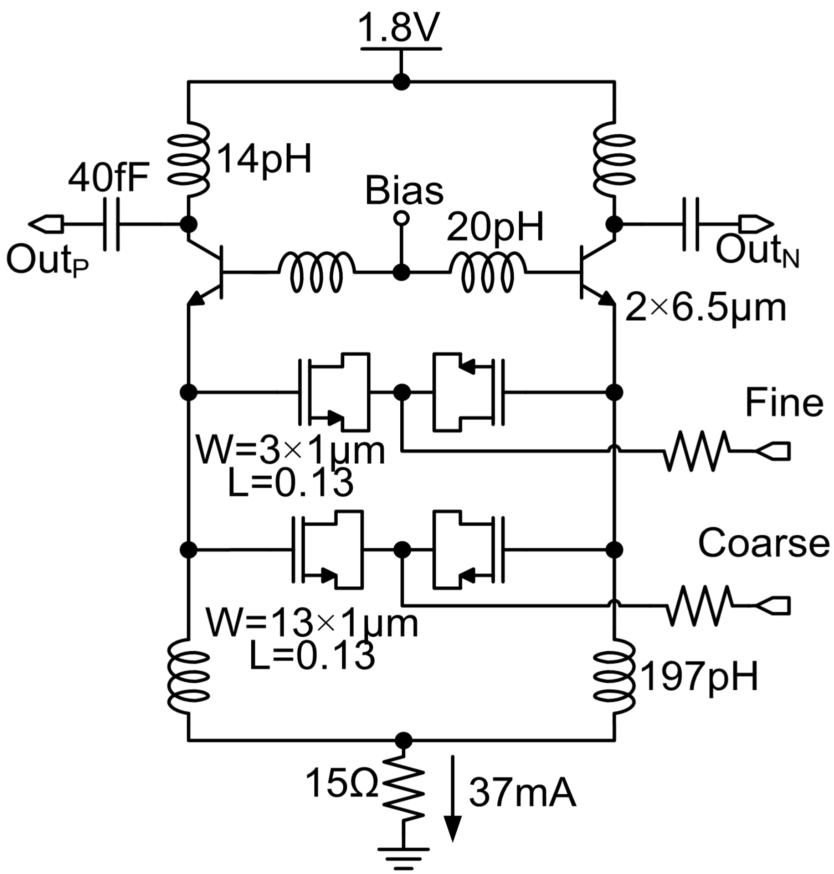


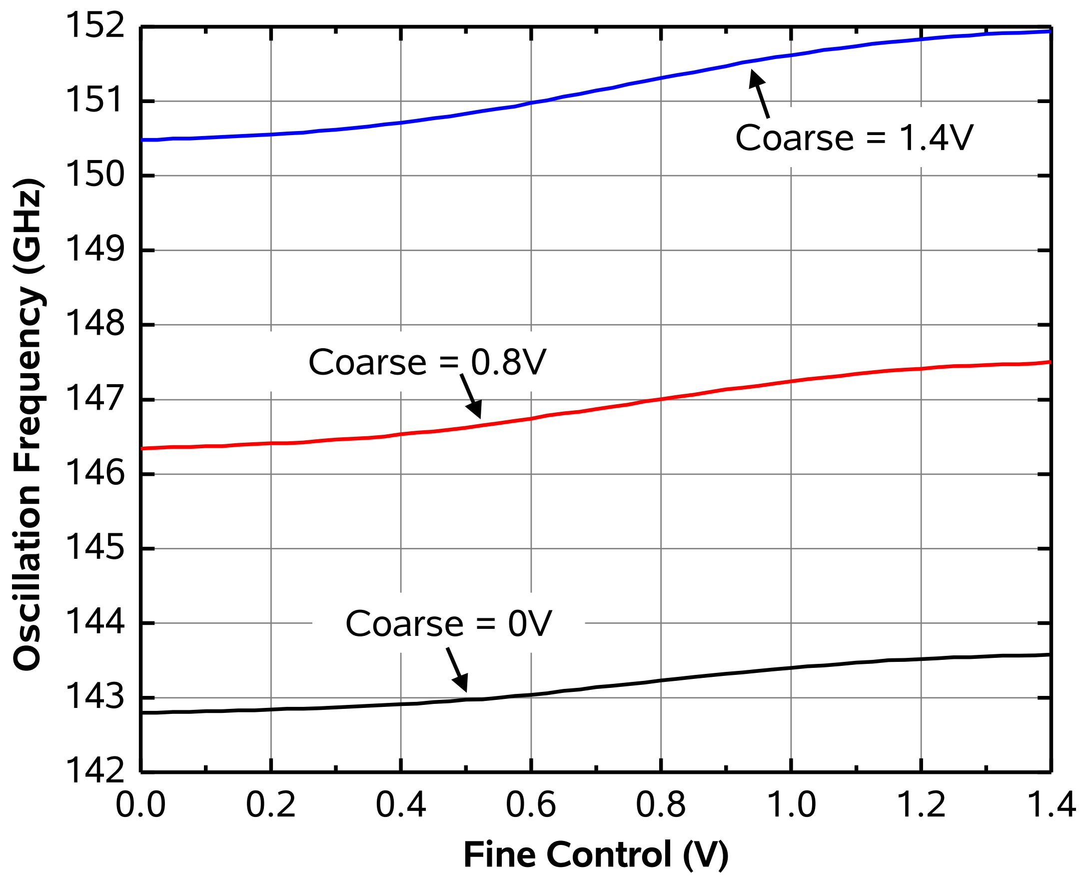






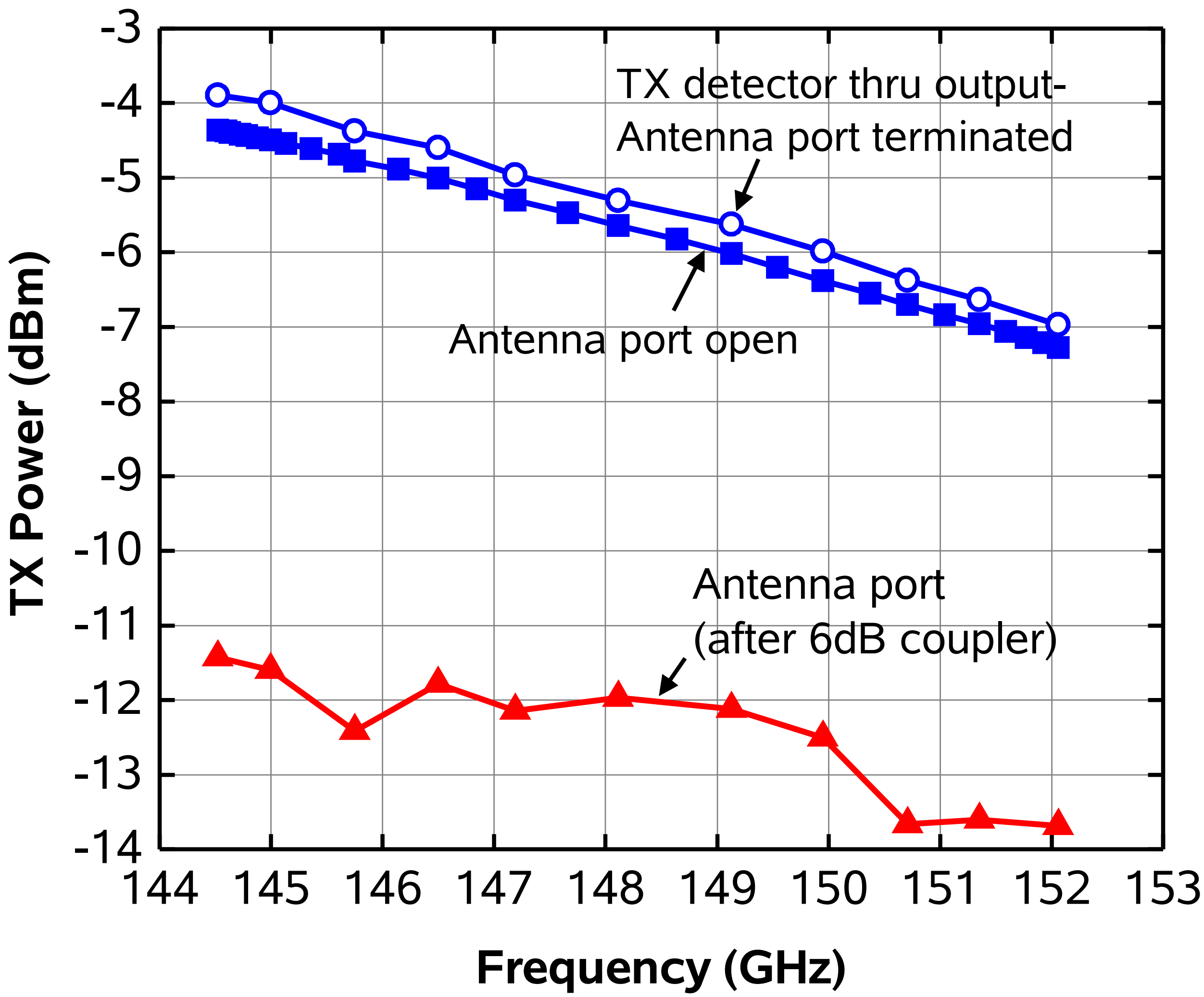
145 GHz fundamental frequency VCO





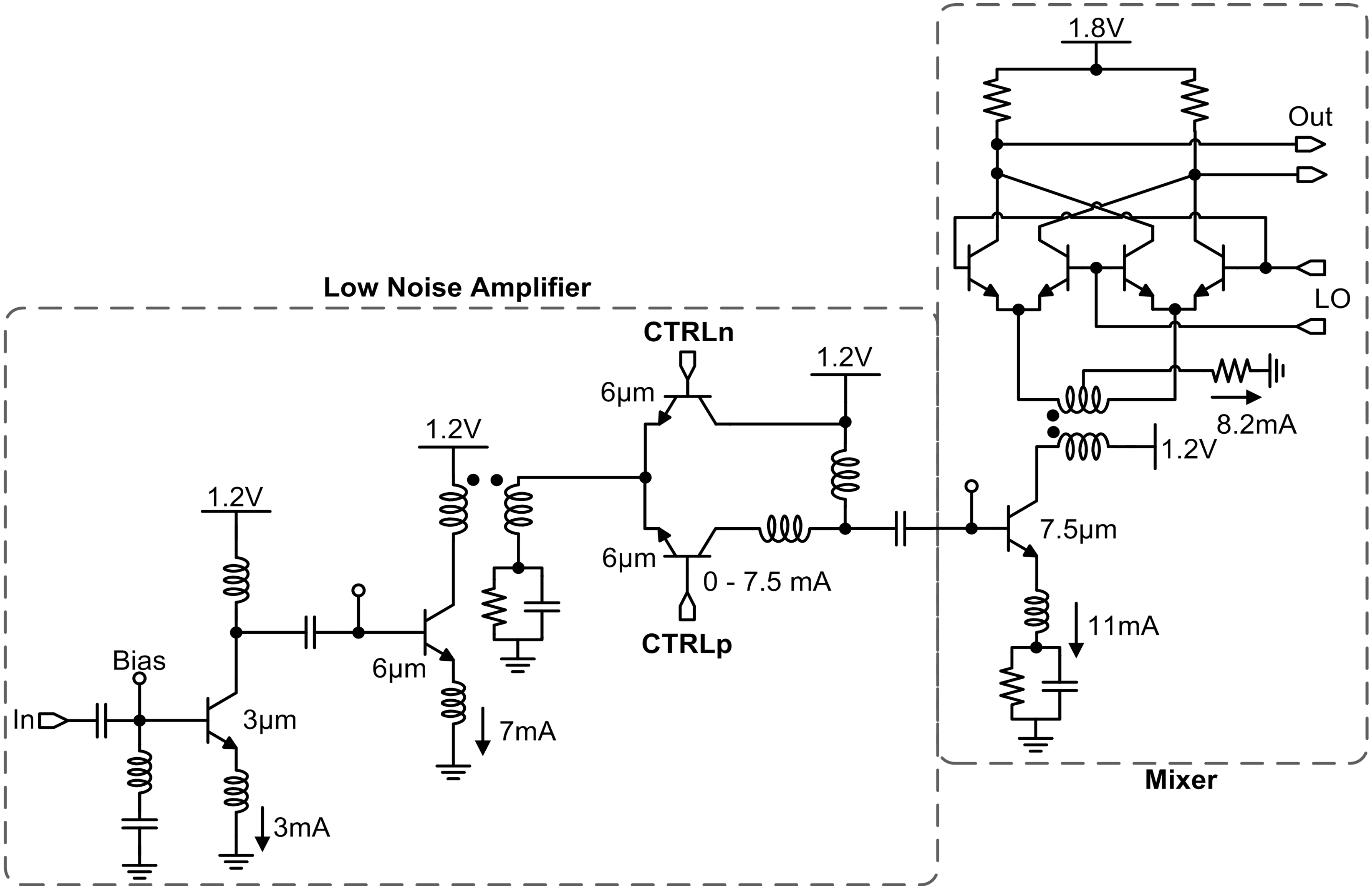
- 143-152 GHz tuning range
- PN=-103 dBc/Hz @10MHz offset
- P_{DC} = 72 mW

Measured output power

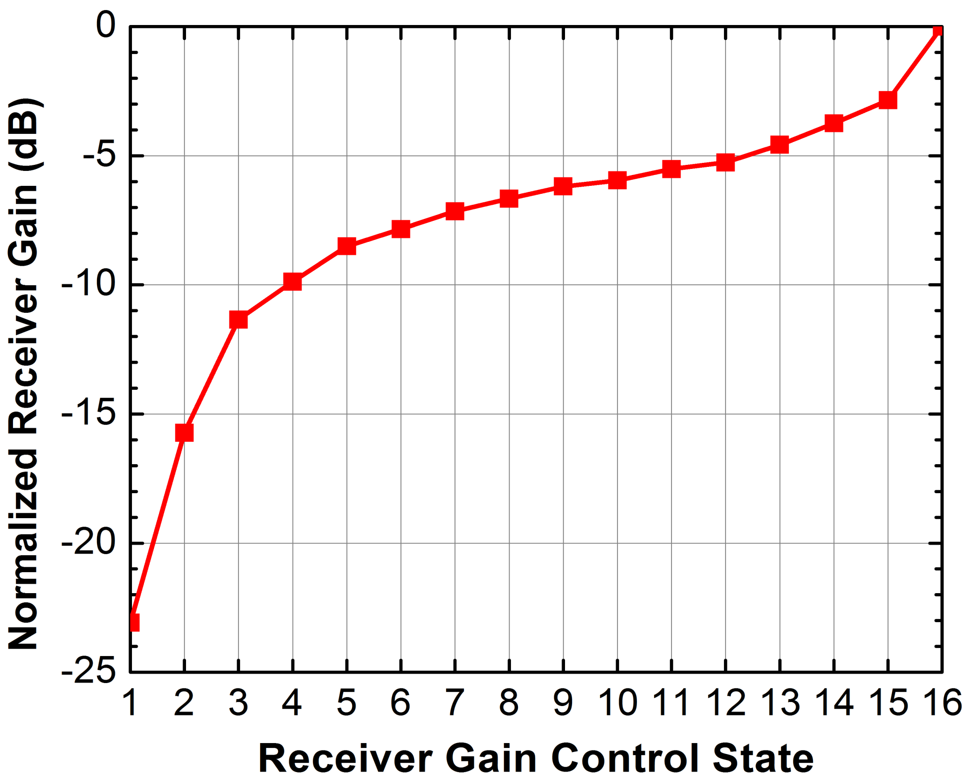


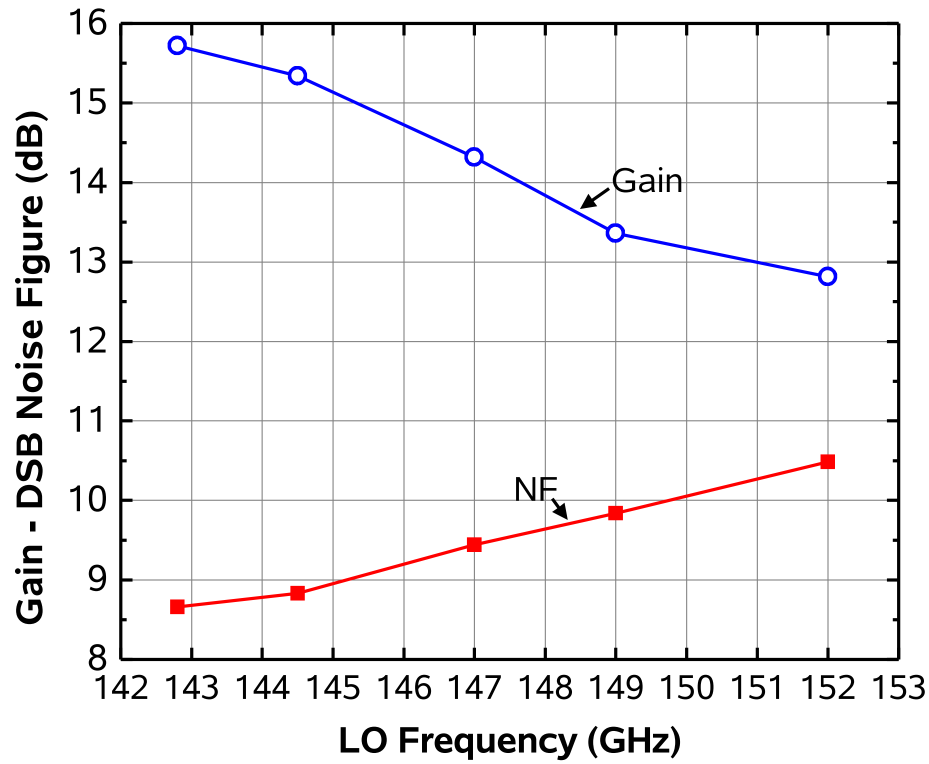
•Power at antenna port measured with ELVA power sensor
•On-chip and external measurements track very well

Receiver schematics



Receiver Gain and Noise Figure

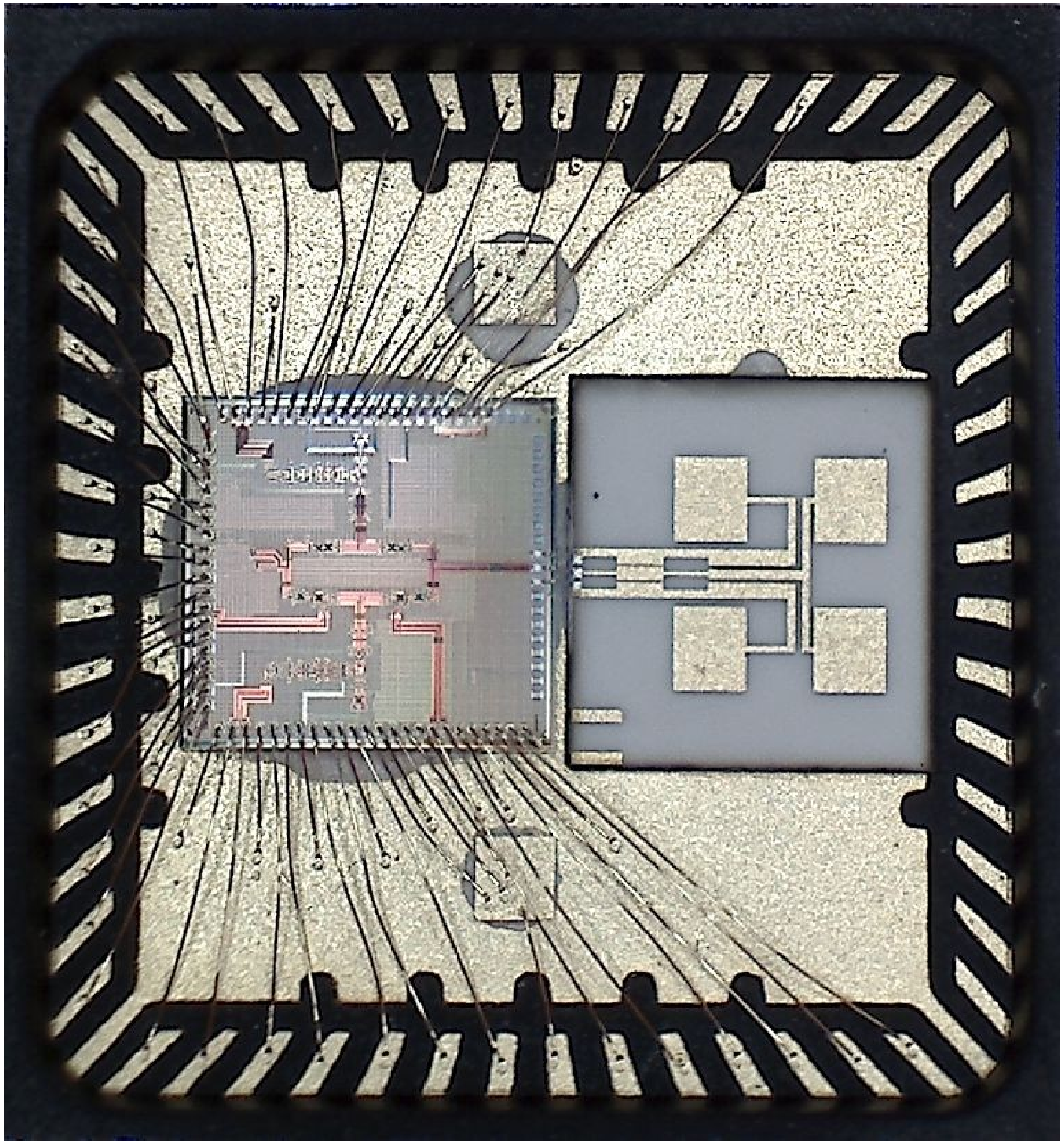




13-15 dB gain, 23 dB of gain control in LNA

Low noise figure: 8.5-10.5dB

Antenna and die in package



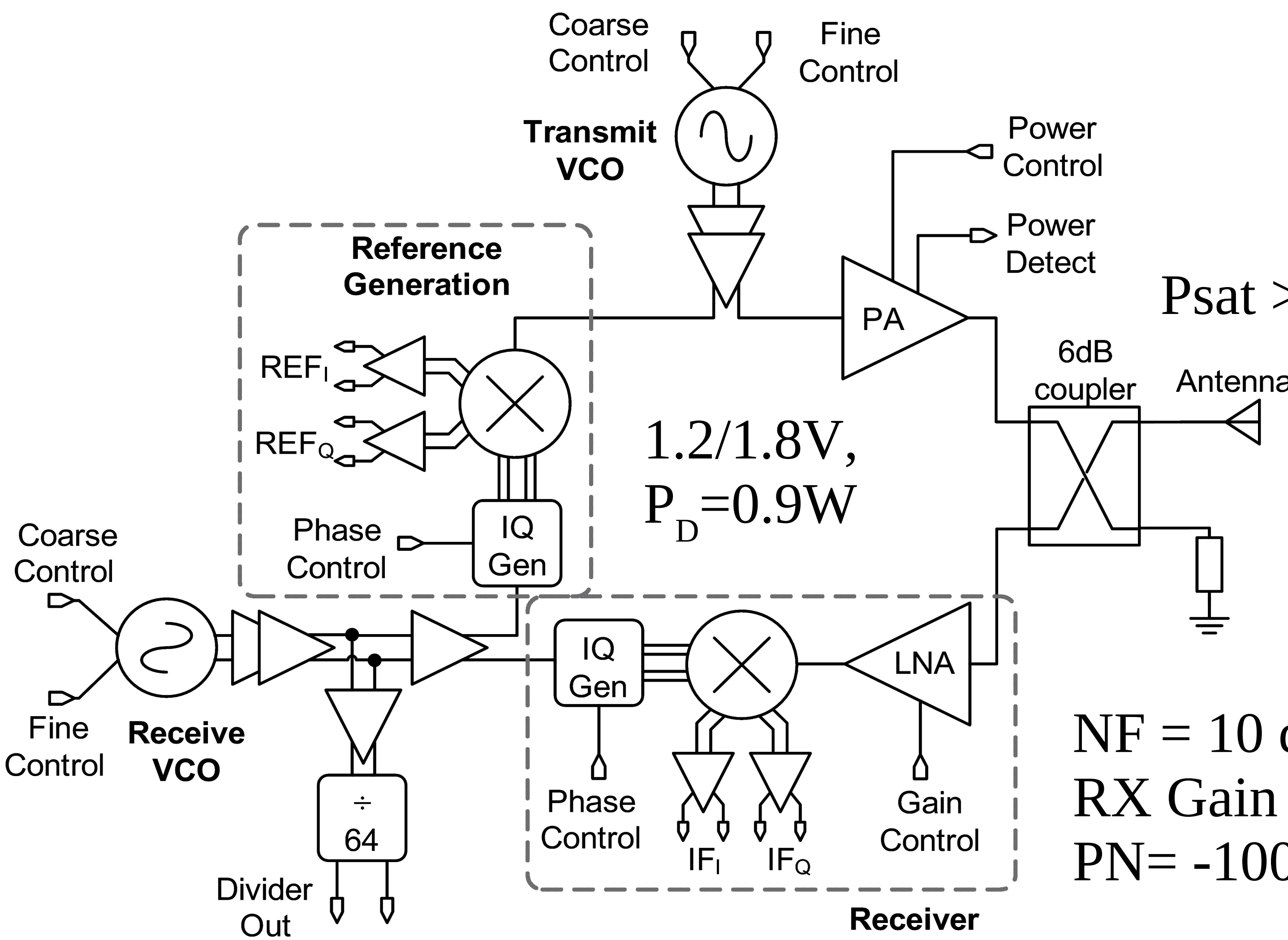
QFN package with

bondwire transition to

antenna on alumina

Courtesy of Robert Bosch GmbH, Karlsruhe Institute of Technology and EU SUCCESS project partners

120-GHz Distance Sensor



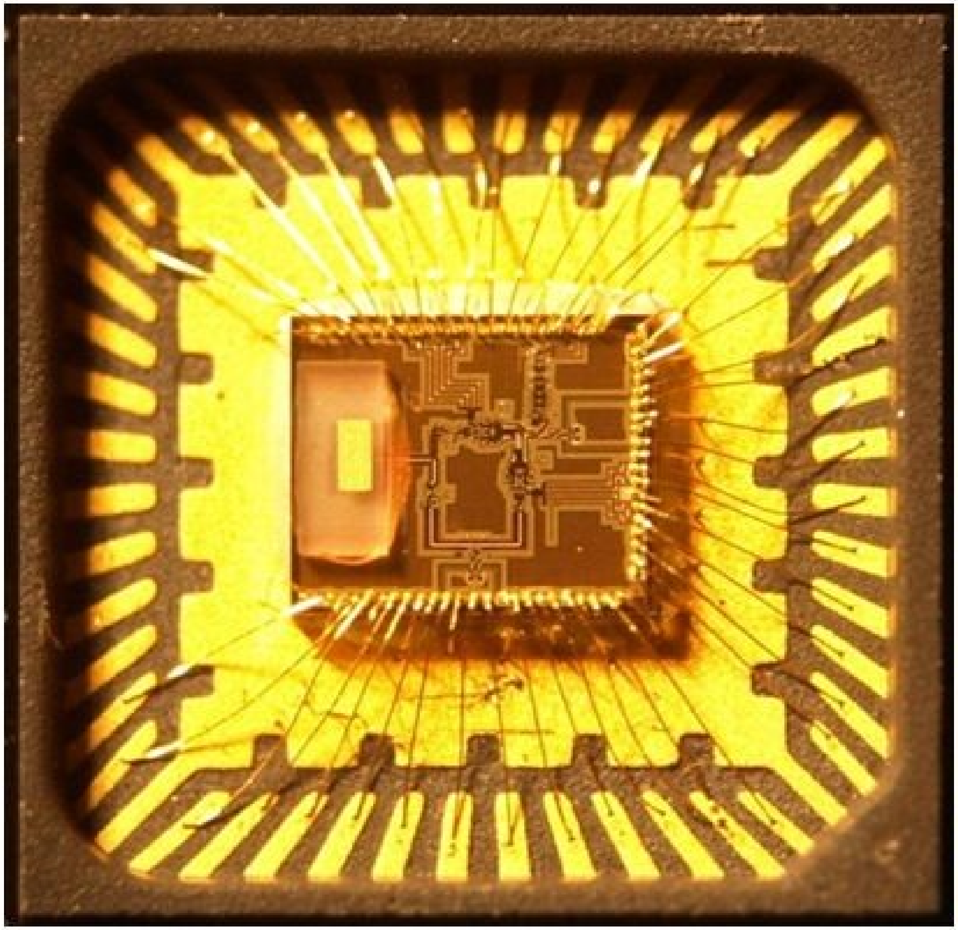
Psat > 3 dBm

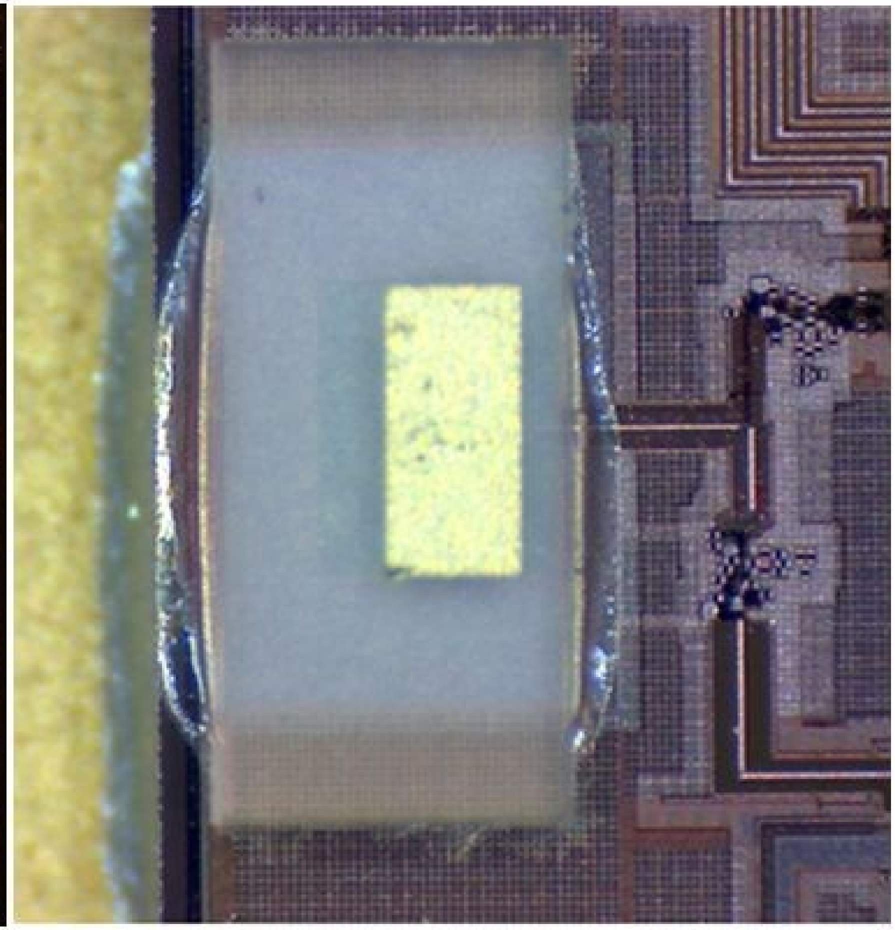
1.2/1.8V,
P_D=0.9W

NF = 10 dB
RX Gain = 12 dB
PN= -100 dBc/Hz

[I. Sarkas et al. Trans. MTT, March 2012]

Layout and Packaging





Chip: 2.2mm×2.6mm Package: 7mm×7mm Dr. J. Hasch

130-nm BiCMOS9MW: SiGe HBT f_T= 230 GHz, f_{MAX} = 280 GHz

Summary

- Inductors and transformers are scalable to at least 200 GHz
- Accurate modelling of passives is as critical as transistor models
- Transistor layout is critical to nanoscale CMOS circuit performance
- Layout parasitics can degrade CMOS IC performance by as much as one technology node
- HF SoC performance critically dependent on
  - supply distribution and de-coupling strategies
  - Signal and block-to-block isolation strategies
- Examples of mm-wave ICs above 60 GHz

TX/RX Packaging