Problem for Chapter 19 of 'Ultra Low Power Bioelectronics'

Problem 19.1

In this problem, we will investigate the dc-current feedback cancelation scheme of the microphone front-end circuit of Figure 19.3. Draw a simple feedback block diagram with the drain current of the JFET transistor as the input and v_{OUT} as the output.

a) Verify that the loop transmission for the feedback loop in this diagram can be approximated as $L(s) = -G_M / (sC_{DC} g_m^{M1} R_f)$ as stated on Page 539.
b) What is the unity-gain frequency corresponding to $L(s)$?
c) Find an expression for the closed-loop transfer function from $V_{in}(s)$ to $V_{out}(s)$.
d) How should we place the unity-gain frequency with respect to the signal of interest and why?
e) Explain how this feedback loop attenuates the $1/f$ noise of M_1 and the JFET input transistor in Figure 19.3.

Problem 19.2

With the help of the block diagram from Problem 19.1, draw a new block diagram that relates the input $v_{electret}$ to the output v_{OUT}. Add thermal noise sources from R_S and R_f in the block diagram and calculate the SNR at the output in the passband. Comment on how each noise source contributes to the total noise at the output and how the gain of the circuit affects the overall SNR.

Problem 19.3

Derive Equation (19.2) and (19.3). To arrive at your answers, you can assume that the transconductor G_1 and G_2 are operating in the subthreshold regime, and that all the bipolar transistors in Figure 19.5 are matched.

Problem 19.4

Equation (19.13) is an example of a 'stochastic-resonance' phenomenon seen in thresholding systems: an optimum threshold maximizes signal-to-noise ratio at the output for a given fixed noise at the input. Explain physically why a fixed threshold but variable noise at the input would also lead to stochastic resonance: an optimum amount of noise at the input maximizes signal-to-noise ratio at the output.

Problem 19.5

In this problem, we will examine the operation of the micro-power envelope detector shown in Figure 19.7.

a) Assume that the amplifier A is effective at eliminating the dead zone of the current rectifier in Figure 19.7 (a). Draw a small-signal block diagram relating i_{OUT} and v_{IN}.
b) The G_m transconductor is implemented with the topology shown in Figure 19.7 (b). If $I_{B2} = 2\ \mu$A and the input differential pair transistors are operating in subthreshold, determine the value of the capacitance C that allows input signals, v_{IN}, with frequency higher than 100 Hz to pass through the rectifier. You may assume that all current mirrors have a 1:1 ratio in Figure 19.7 (a).
c) If v_{IN} is a 1 kHz sine wave, with an amplitude of 50 mV superimposed on a DC voltage V_{DC} ($v_{IN} = 0.05\sin\left(2\pi \times 10^3 t\right) + V_{DC}$) and the bias conditions in

part b are valid, sketch i_{REC} (in Figure 19.7 (a)) as a function of time t in the range $0 \leq t \leq 4$ ms. Clearly label the amplitude of i_{REC}.

Problem 19.6

This problem requires the use of a circuit simulator such as SPICE. Simulate the half-wave rectifier circuit in Figure 19.7, using a 0.5 μm transistor model. You can use an ideal OTA (use a VCCS source) for the G_m transconductor and an ideal Op-Amp for the dead-zone-reduction amplifier. Set the G_m of the OTA and the capacitance C according to Problem 19.5 (b). Simulate the circuit for a few different frequencies, both below 100 Hz and well above 100 Hz. Comment on the operation of the circuit and on whether its performance matches your expectations.

Problem 19.7

In this problem, we will analyze the operation of the logarithmic ADC shown in Figure 19.10.

a) Calculate that value of v_- right at the end of the auto-zeroing phase. Assume that the input diode has a current-voltage characteristic described by $I_D = I_s e^{V_D/\phi_t}$ where I_D is the diode current, I_s is the process-dependent saturation current of the diode, and ϕ_t is the thermal voltage. Express your answer in terms of I_{REF}, I_s, I_{OS}, ϕ_t and G_m. Comment on how to choose the value of I_{OS} such that the input voltage utilizes the whole linear range $[-V_L, V_L]$ of the transconductor.

b) During the integration phase, calculate the charging current on C_{int} as a function of the parameters of part a) and of the input current I_{IN}. Note that the switch $\overline{DEINT}$ is still closed during this phase.

Problem 19.8

Derive Equation (19.16), which pertains to the operation of Figure 19.12 and explain why it leads to constant-G_m biasing in subthreshold operation.

Problem 19.9

Derive Equation (19.18), which pertains to the low-power CMOS imager of Figure 19.18 (a). You can assume, initially, that C_{eff} is linear. Why does C_{eff} not come into play in Equation (19.18)?

Problem 19.10

For an arbitrary probability distribution of noise strengths in a multi-electrode neural-amplifier array as shown in Figure 19.23, derive a mathematical scaling law that illustrates the power savings obtained via an adaptive-power-biasing scheme versus that of a traditional worst-case biasing scheme.