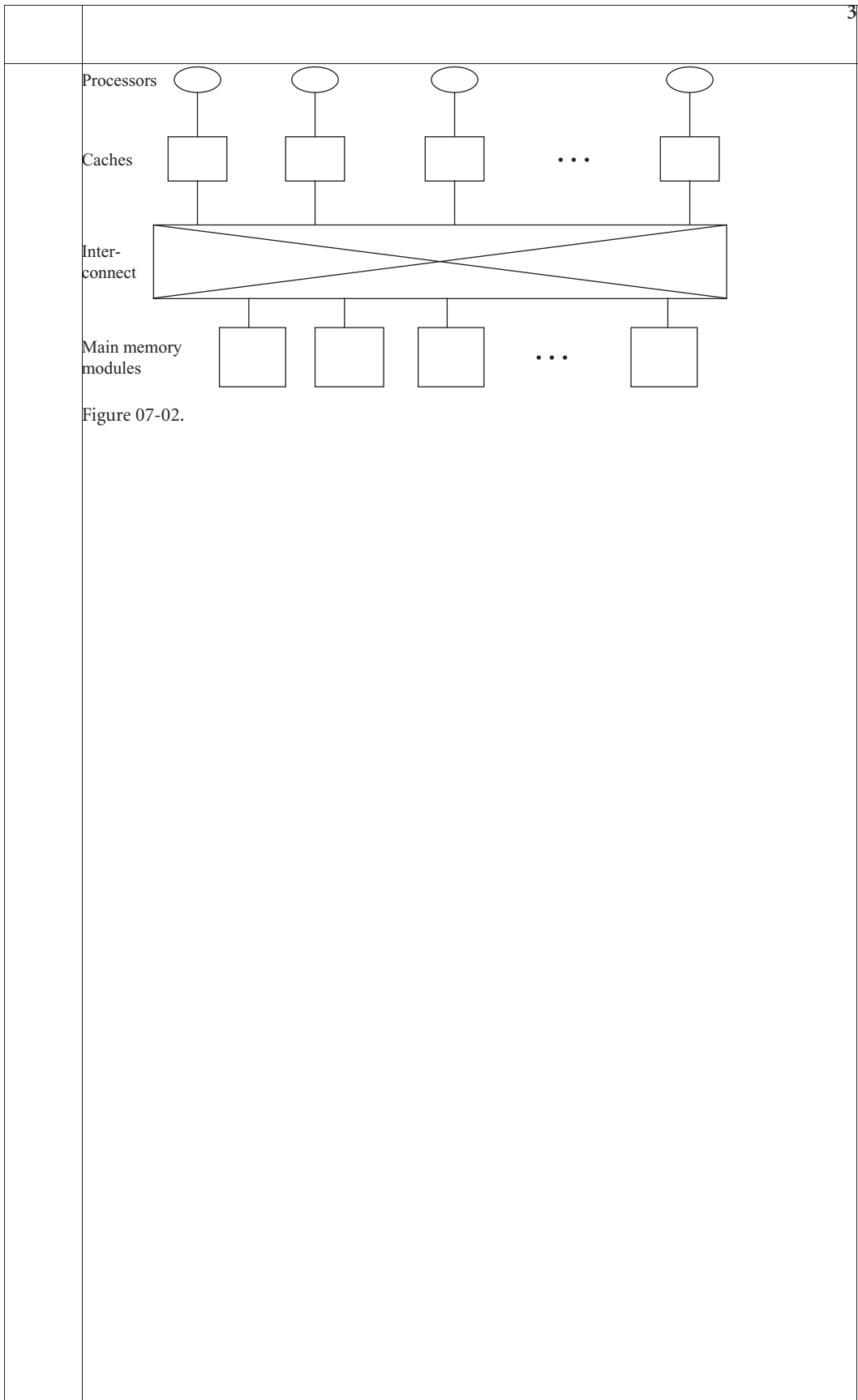


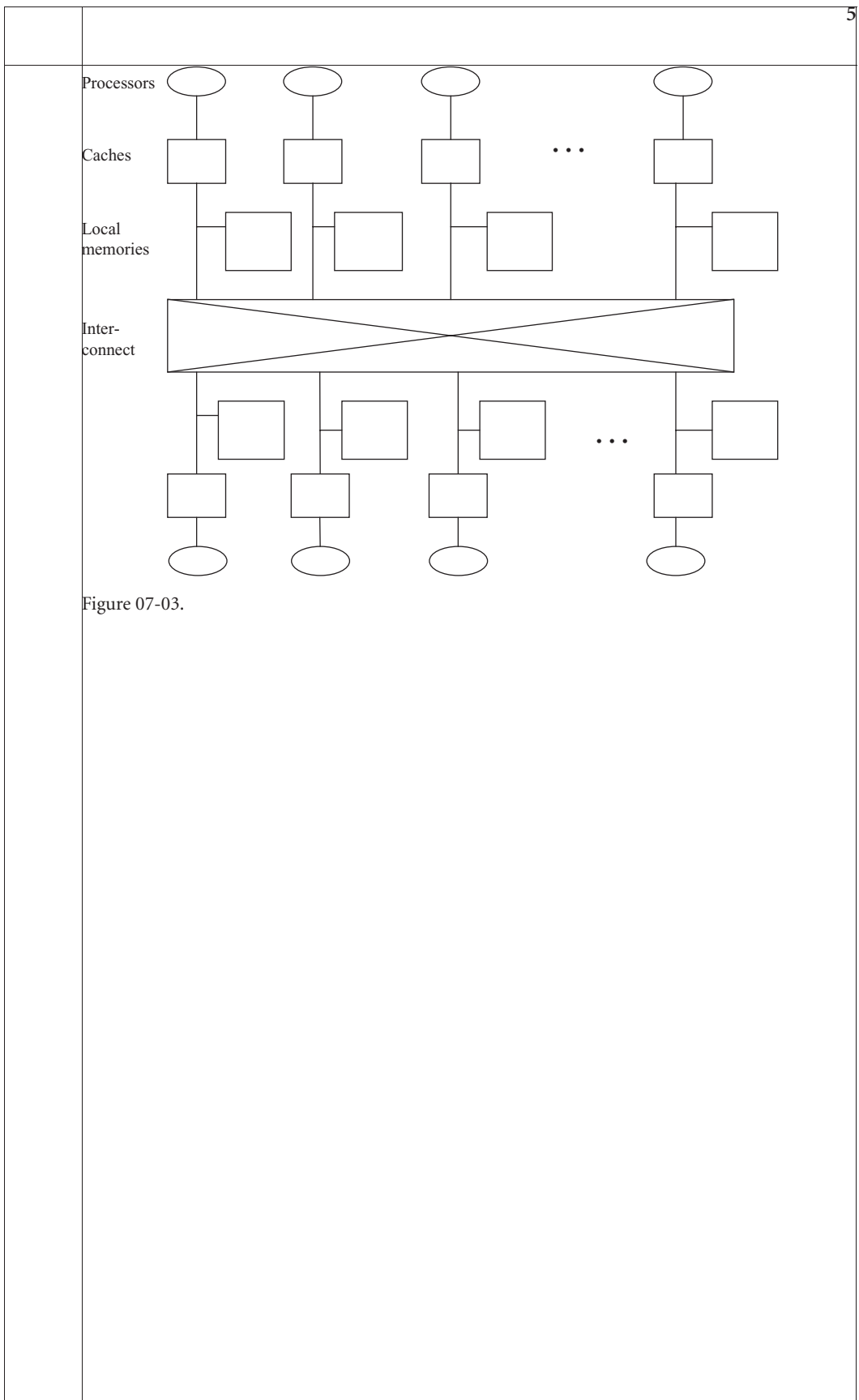
Convert Art

Figure 07-01.



Convert Art

Figure 07-02.



Convert Art

Figure 07-03.

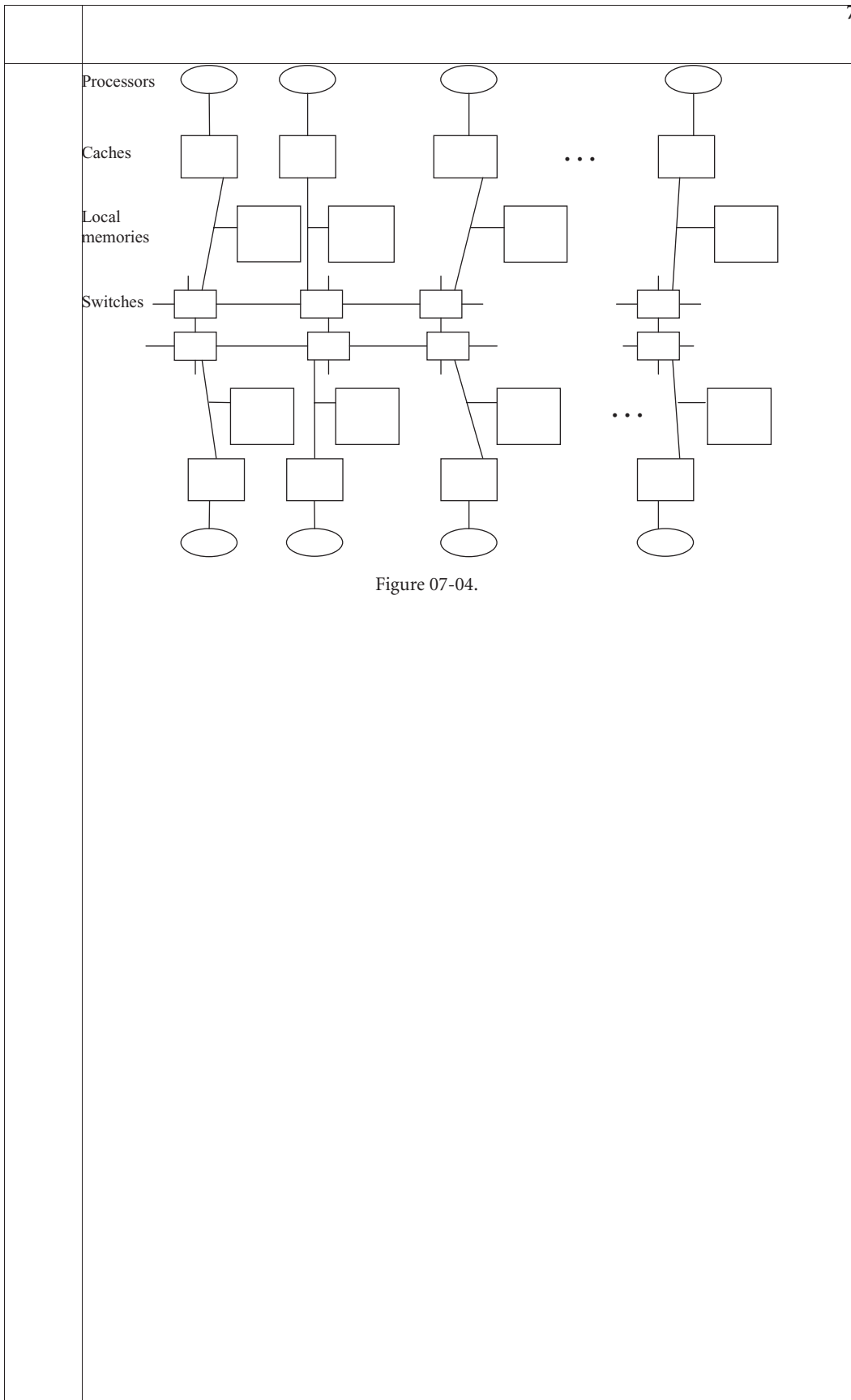
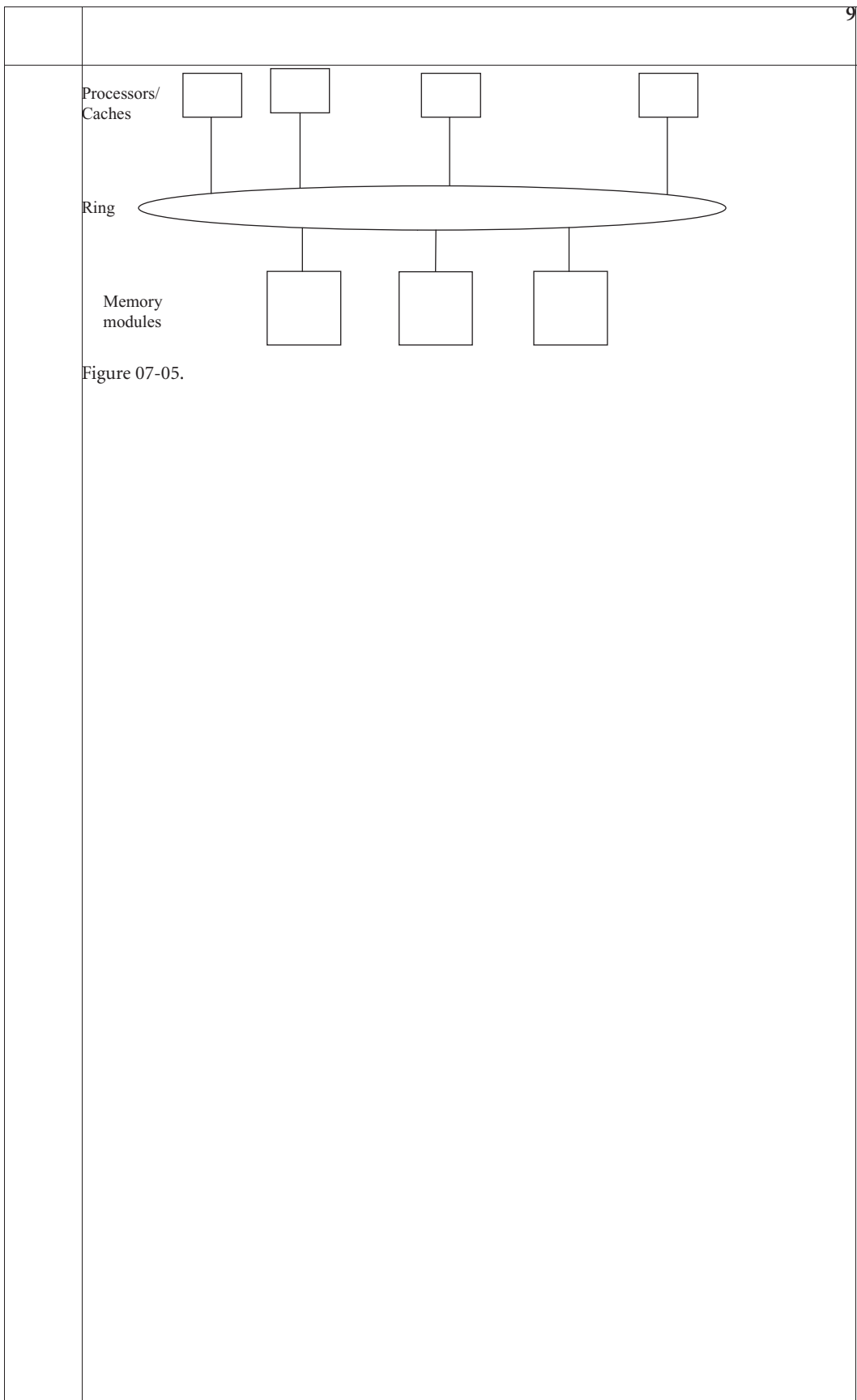


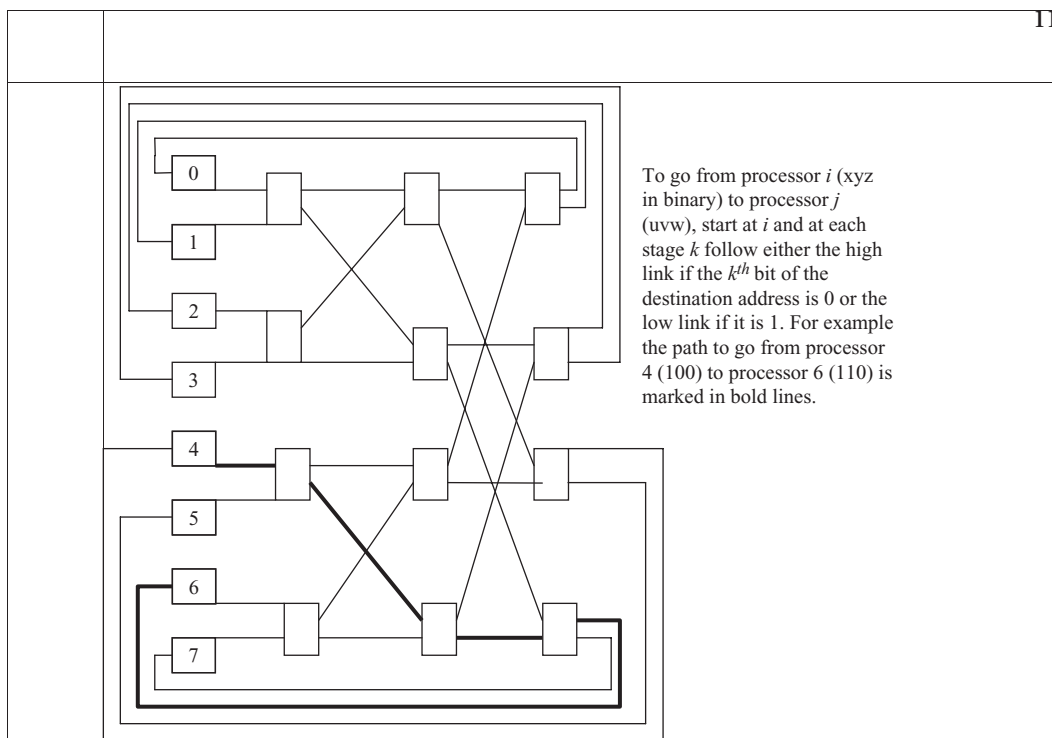
Figure 07-04.

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Figure 07-05.

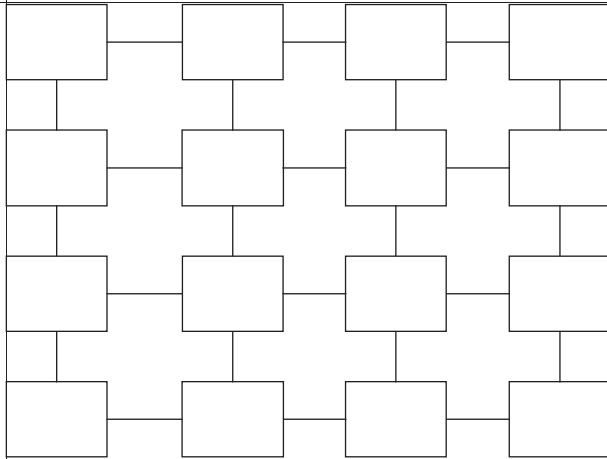


To go from processor  $i$  ( $xyz$  in binary) to processor  $j$  ( $uvw$ ), start at  $i$  and at each stage  $k$  follow either the high link if the  $k^{\text{th}}$  bit of the destination address is 0 or the low link if it is 1. For example the path to go from processor 4 (100) to processor 6 (110) is marked in bold lines.

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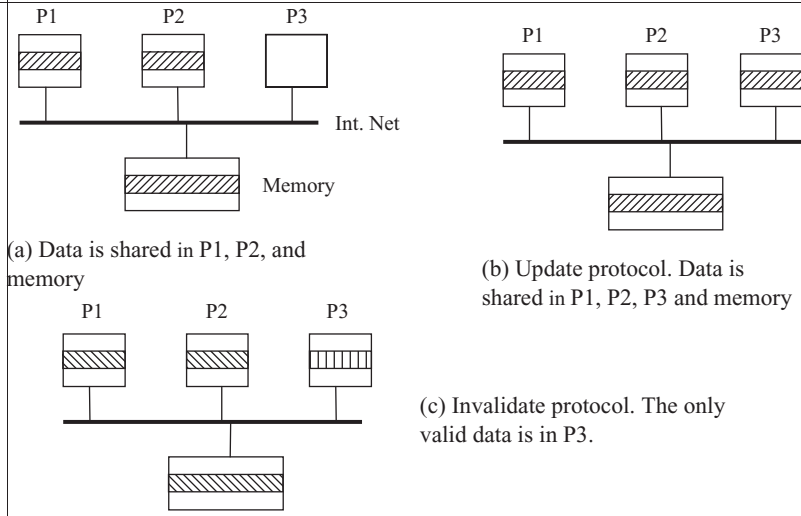
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Figure 07-06.



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Figure 07-07.



(a) Data is shared in P1, P2, and memory

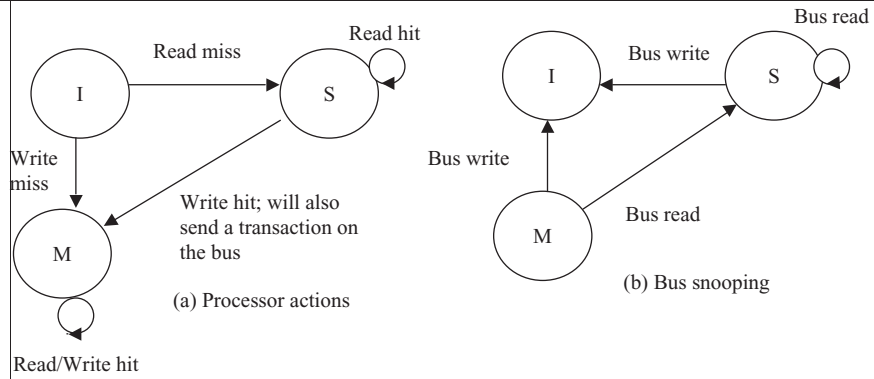
(b) Update protocol. Data is shared in P1, P2, P3 and memory

(c) Invalidate protocol. The only valid data is in P3.

Figure 07-08.

Convert Art





(a) Processor actions

(b) Bus snooping

Figure 07-09.

Convert Art

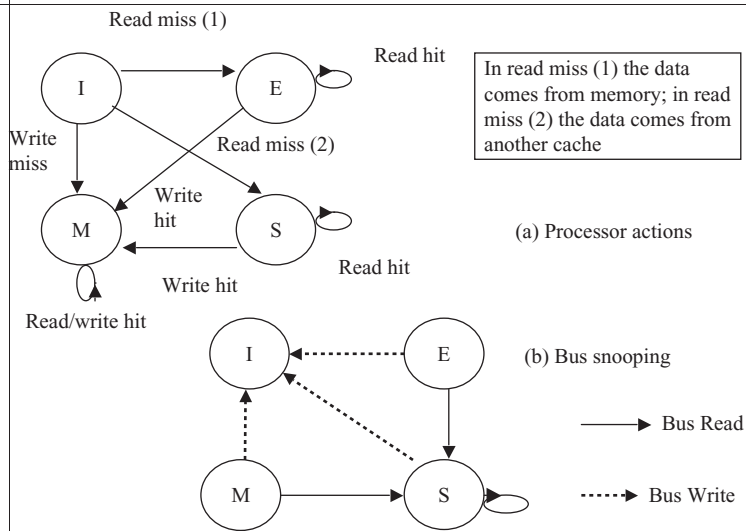


Figure 07-10.

Convert Art