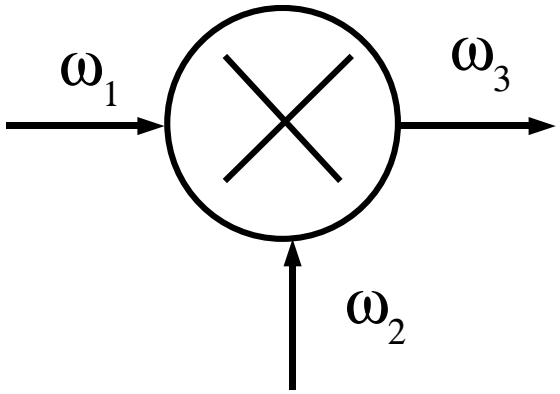
HF mixer, switch & modulator design

Outline

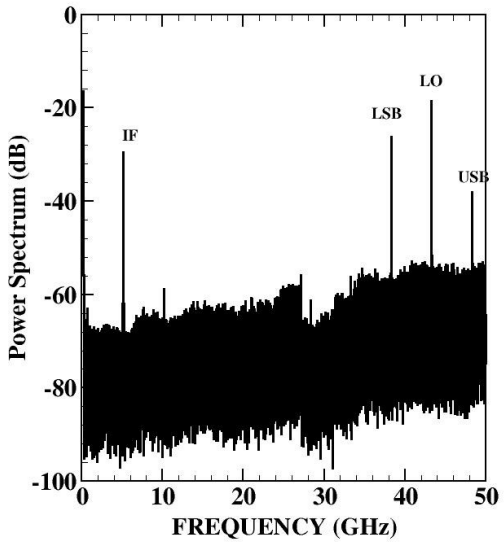
- Mixer fundamentals & topologies
- Mixer design methodology
- Example of up- and down-convert mixers
- Switches
- Phase shifters
- Modulators

Mixer fundamentals (i)



$$A\cos(\omega_1 t)\times\ B\cos(\omega_2 t)=\frac{AB}{2}[\cos(\omega_1-\omega_2)t+\cos(\omega_1+\omega_2)t]$$

- The mixer is a multiplier used as a frequency translation device:
  - up-converter from IF to RF
  - down-converter from RF to IF
- Two input signals and one output signal
- Image frequency (undesired)



Mixer fundamentals (ii)

- Requires non-linear device:
  - diode,
  - HBT,
  - MOSFET

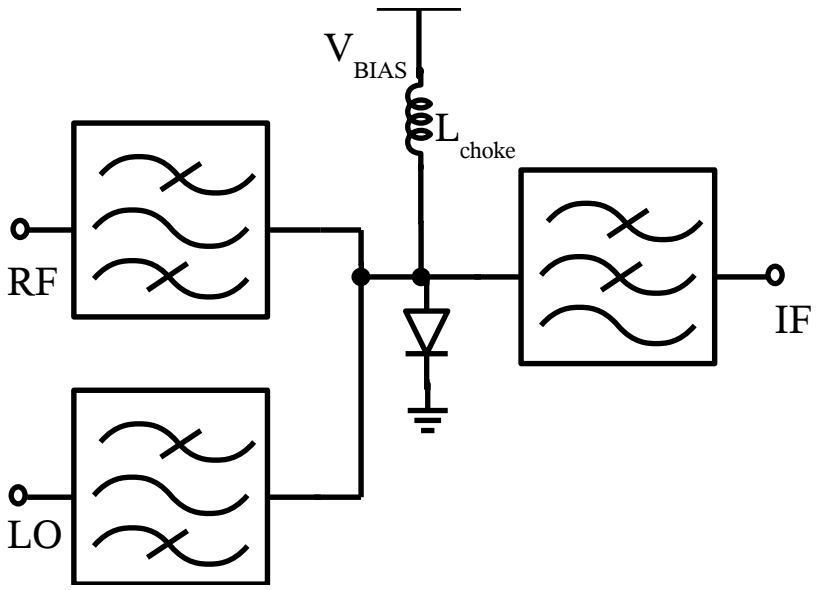
  or time varying device (switch)

$$I(V)=I_S\left[\exp\left(\frac{qV}{nKT}\right)-1\right]$$

$$i_{DS}=\frac{\beta}{2}\left[v_{GS}(t)-V_T\right]^2$$

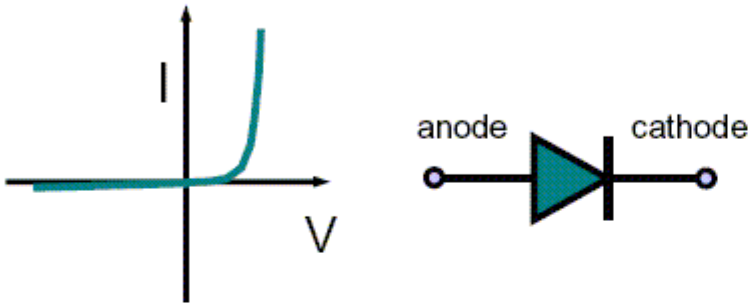
to generate "mixing" terms at sum and difference frequencies

- Requires filtering at RF, LO and IF to select desired signal frequency

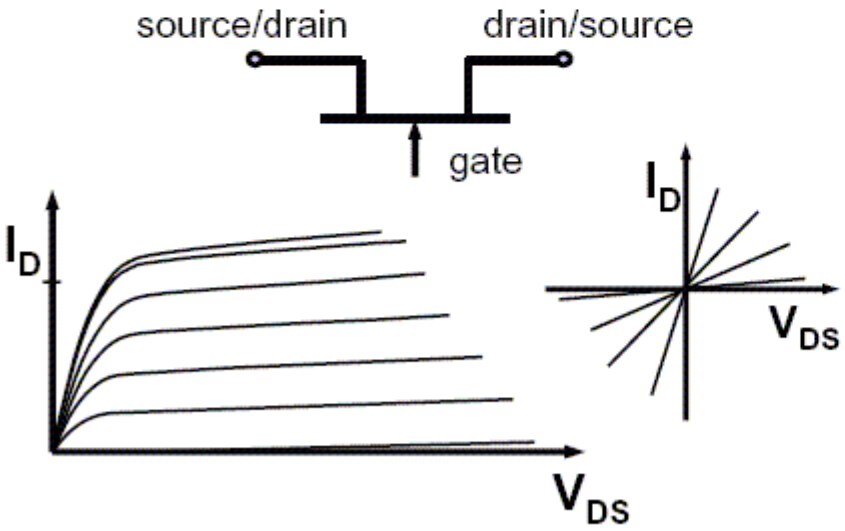


How do you make a multiplier?

1 Nonlinear Device

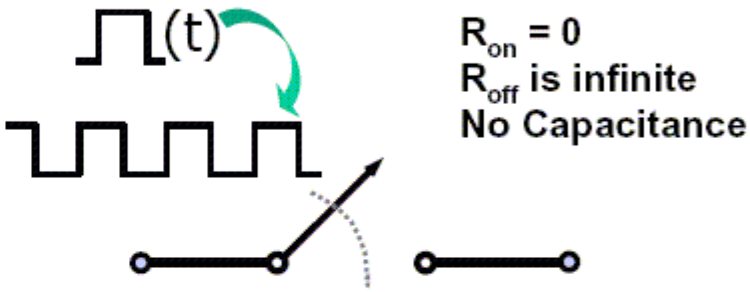


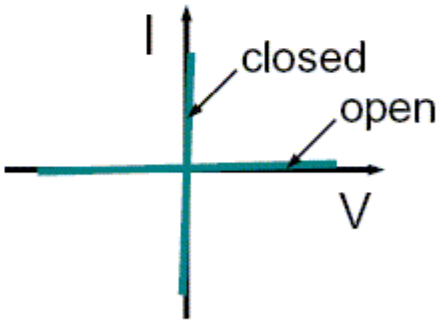
or



"Any device exhibiting nonlinear behavior is a multiplier."

2 Time-varying Device





$$W = \sqcap(t) \times f(t)$$

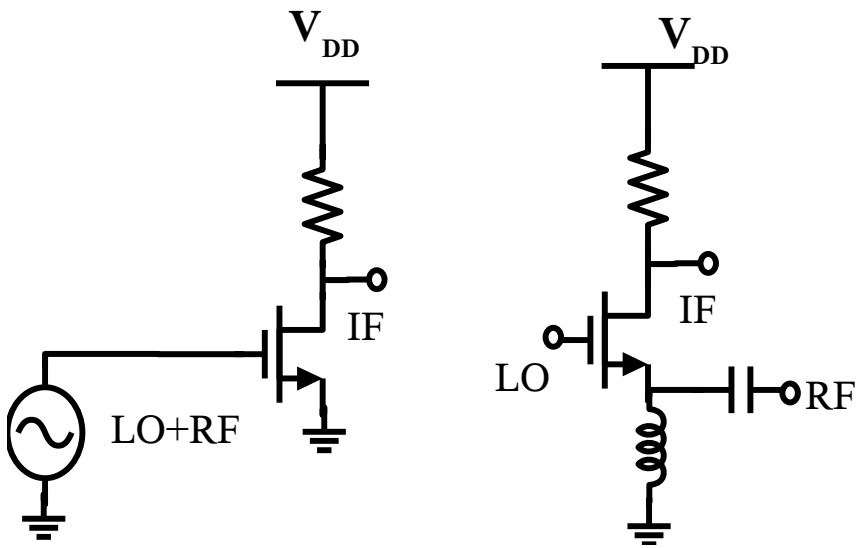
[CSICS-2005 Primer Course]

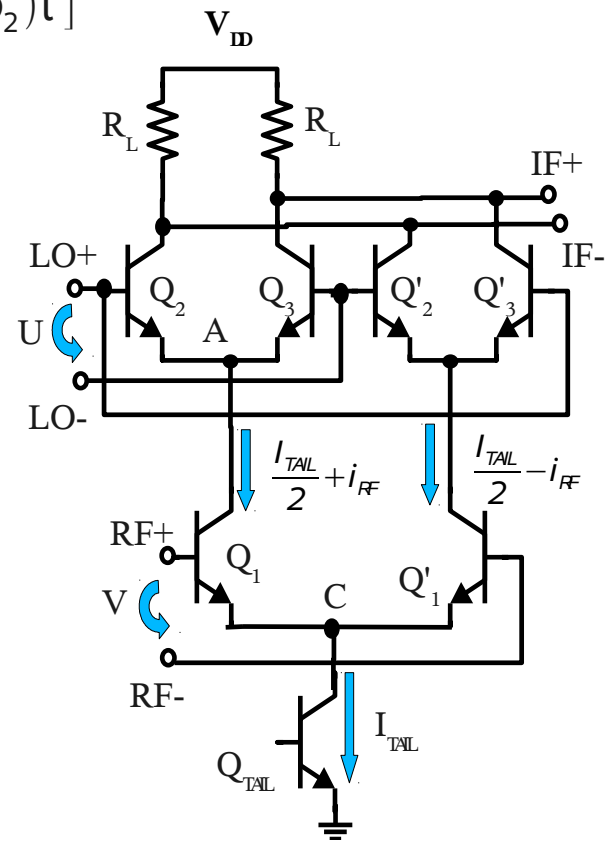
Mixer fundamentals (iii)

- Single-, two-port or three-port implementation
- Present IC mixers use Gilbert-cell multiplication

$$(A\cos\omega_1 t)(B\cos\omega_2 t)=\frac{AB}{2}[\cos(\omega_1-\omega_2)t+\cos(\omega_1+\omega_2)t]$$

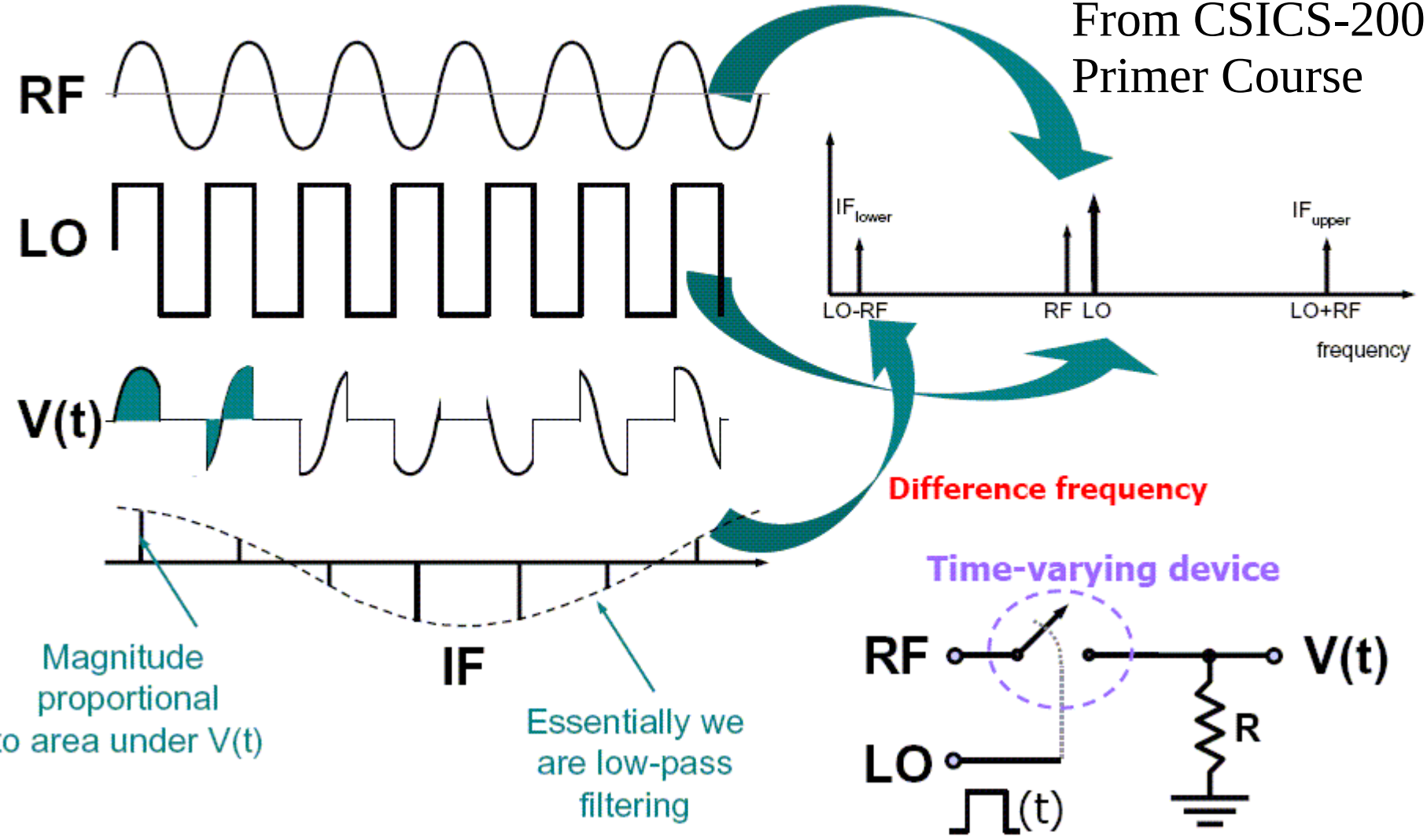
  - $\omega_1 = \omega_{RF}$, $\omega_2 = \omega_{LO}$ and $\omega_1-\omega_2 = \omega_{IF}$
  - $\omega_1 = \omega_{IF}$, $\omega_2 = \omega_{LO}$ and $\omega_1+\omega_2 = \omega_{RF}$



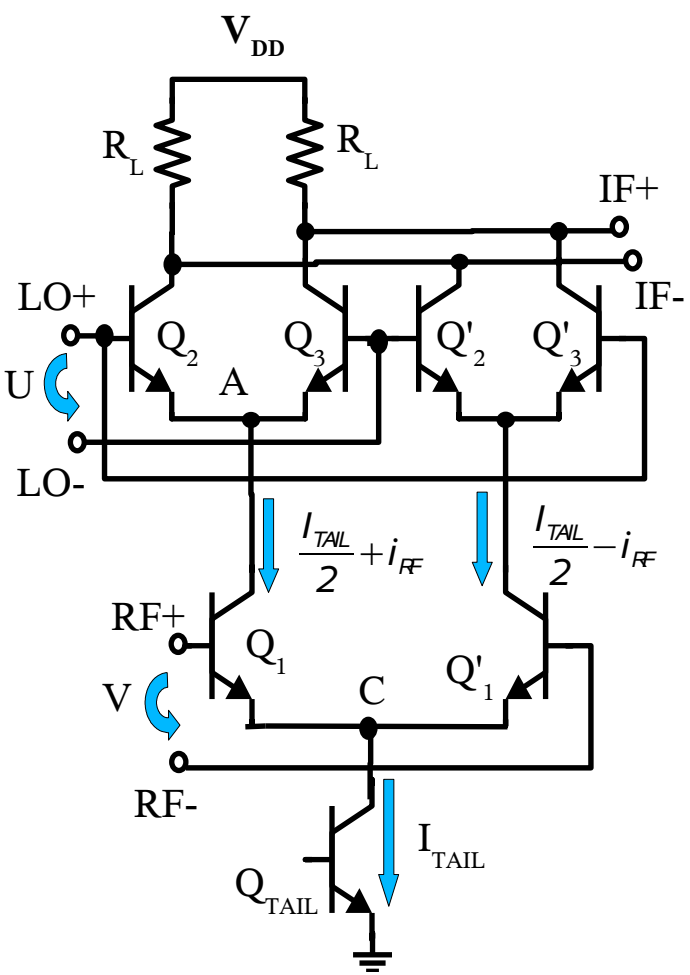


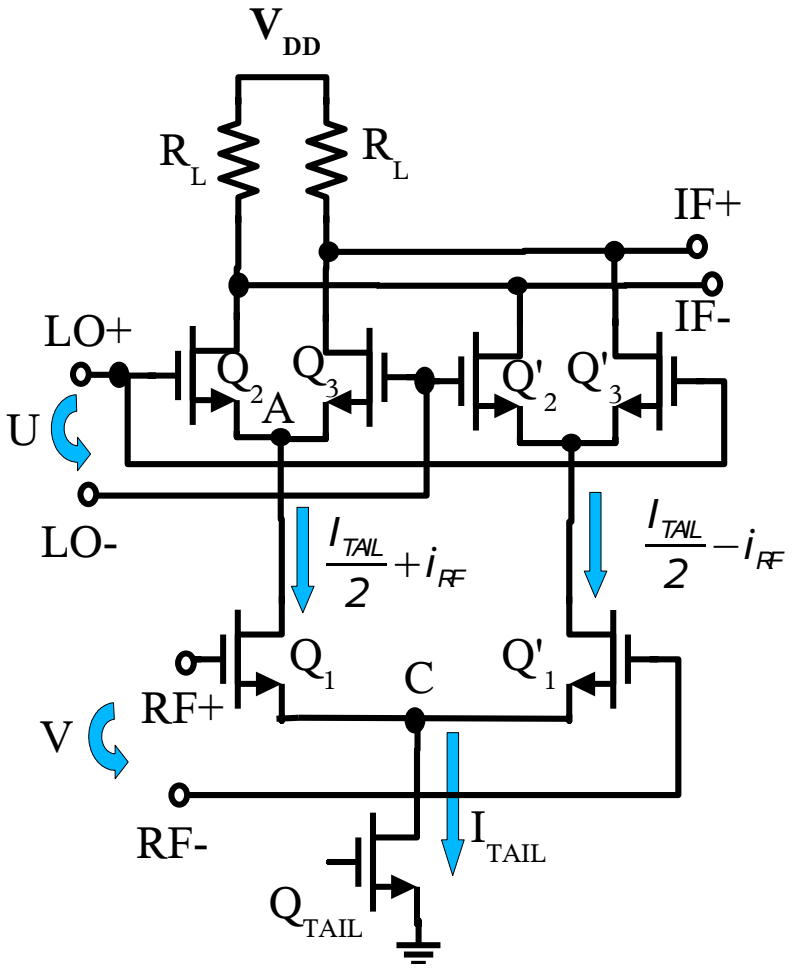
Visualizing Mixer Operation – (LO – RF) "IF" Signal

From CSICS-2005 Primer Course



Mixer topology: Gilbert (multiplier) cell





$$\Delta I = I_{Q2} - I_{Q3} = I_{Q1} \times \tanh(U/2V_T)$$

Mixer specification

- RF, LO, IF frequencies
- Conversion (power) gain
- Linearity
- Noise Figure (receive mixers only)
- Isolation

Conversion gain

- Conversion (power) gain (depends on LO power and mixing quad device type):
  - RF to IF in down-converters
  - IF to RF in up-converters

Gilbert-cell mixer conversion gain

- Output (IF) voltage in BJT mixer

$$v_{IF} = -2 R_L I_{bias} \tanh\left(\frac{v_{RF}}{2 V_T}\right) \tanh\left(\frac{v_{LO}}{2 V_T}\right)$$

- Voltage conversion gain for large square wave LO signal is (valid for HBT & MOSFET):

$$\tanh\left(V_{LO}\cos(\omega_{LO} t)\right) = \frac{4}{\pi}\cos(\omega_{LO} t) + \frac{4}{3\pi}\cos(3\omega_{LO} t) + \frac{4}{5\pi}\cos(5\omega_{LO} t) + ..$$

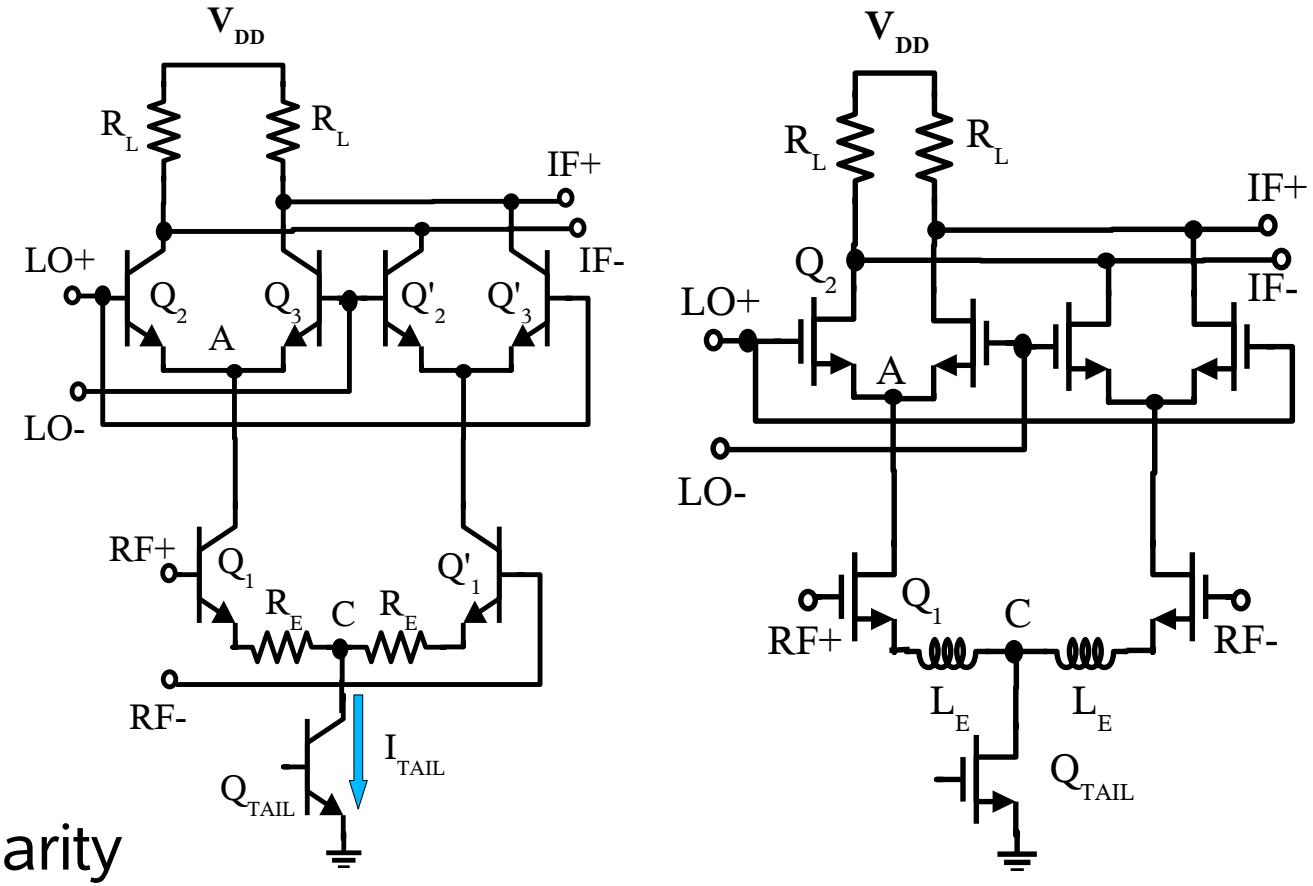
$$\frac{v_{IF}}{v_{RF}} = \frac{-2}{\pi} g_m R_L$$

Linearity

- Linearity: – depends on transconductor (input amplifier) linearity and V_{DS}/V_{CE} of mixing quad transistors.
  - The 1 dB compression point: P_{1dB}
  - Third-order intercept point: IIP3, OIP3
  - Second-order intercept point: IIP2, OIP2
- Linearity in a cascade of stages:

$$\frac{1}{IIP3} = \frac{1}{IIP3_1} + \frac{G_1}{IIP3_2} + \frac{G_1 \times G_2}{IIP3_3} + \ldots + \frac{G_1 \times G_2 \times \ldots G_{n-1}}{IIP3_n}$$

Gilbert cell with degeneration



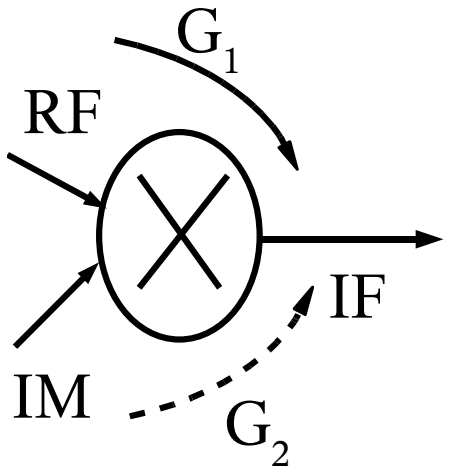
- Improves linearity
- Inductive degeneration does not degrade noise figure

Noise Figure

- Double-sideband noise figure

$$NF_{DSB} = NF_{SSB} - 3dB \text{ (if no image rejection)}$$

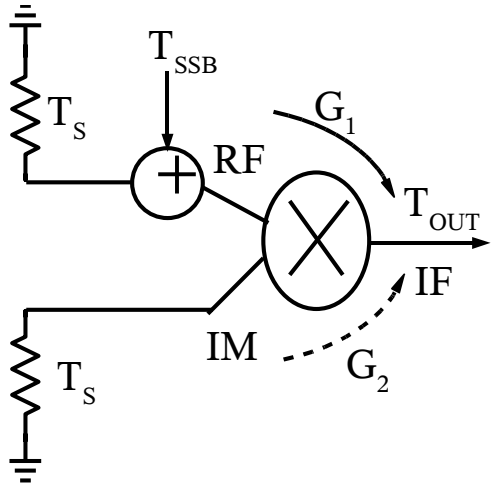
$$F_{DSB} = 1 + \frac{\langle v_{nout}^2 \rangle}{kT(G_1 + G_2)}$$

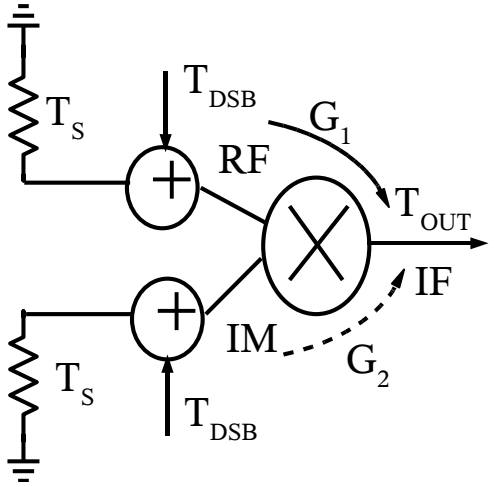


- Single-sideband noise figure (temperature)

$$NF_{DSB} = NF_{SSB} \text{ (if image rejection)}$$

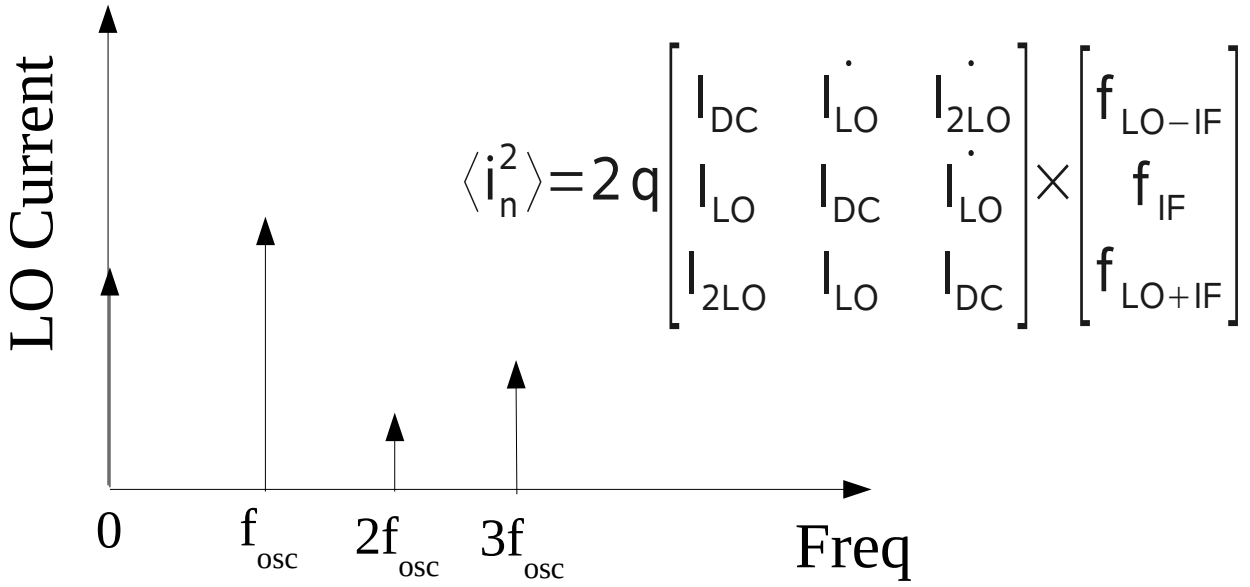
$$F_{SSB} = 1 + \frac{\langle v_{nout}^2 \rangle}{kTG_1}$$





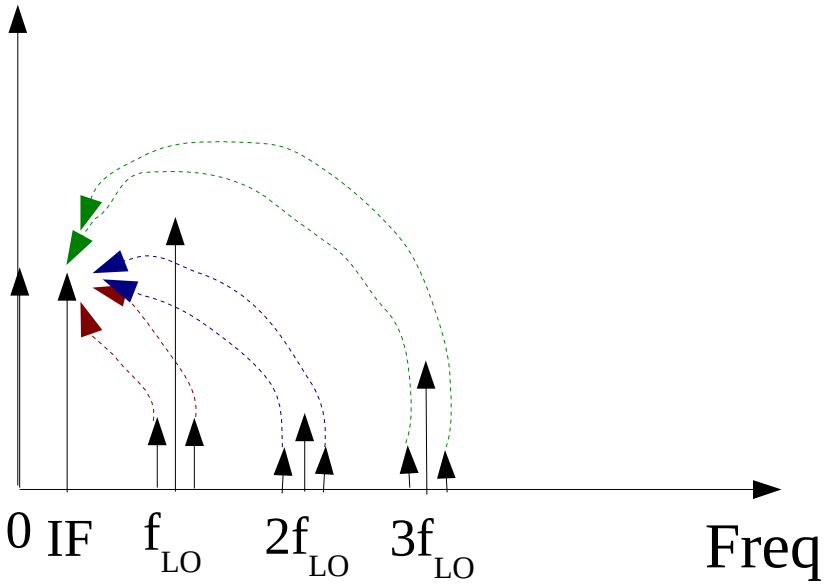
Noise Figure (cont)

- Mixer shot noise sources
  - @ DC
  - @ harmonics of LO (currents at LO harmonics comparable to DC currents).



Noise Figure (cont.)

- Frequency translation of noise sources
  - Large signals at harmonics of LO,
  - Small signals on either side of LO harmonics,
  - Hence noise from nf_{LO} +/- f_{IF} translates to IF and to the output



Isolation

- Want it as high as possible
- Implemented through choice of topology and/or filtering:
  - LO to IF
  - LO to RF
  - IF to LO
- In Gilbert-cell mixer isolation is built-in

$$g_{mLO-IF} = \frac{(I_{Q1} - I_{Q'1})}{2V_T} \times sech^2\left(\frac{U}{2V_T}\right) \approx 0$$

Transmit (up-converter) mixer topology

- Doubly balanced
- MOS, BJT and BiCMOS
- IF linear input amplifier + mixing quad
- IF signal applied to bottom pair
- LO signal applied to mixing quad
- RF BPF (tuned) output at top
- Image rejection must be placed after mixing quad or built into the topology

Receive (down-converter) mixer topology

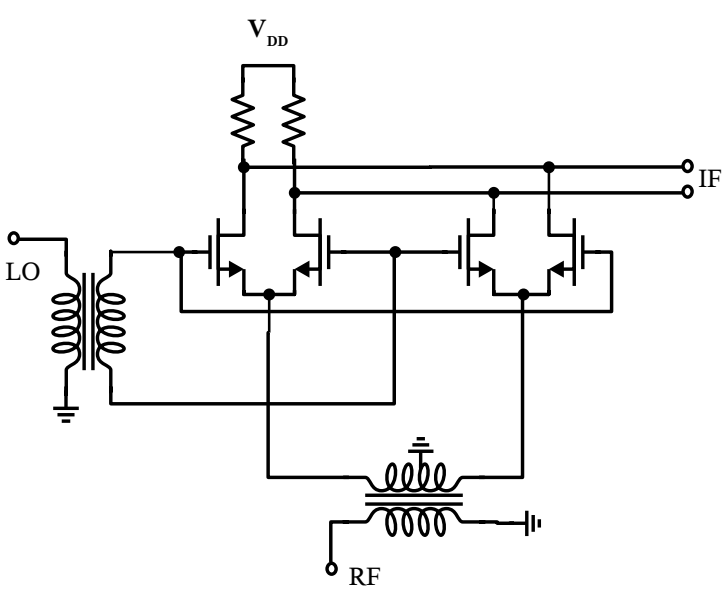
- Doubly balanced
- Good for MOS, BJT and BiCMOS
- RF (low-noise) linear input amplifier + mixing quad
- RF signal applied to bottom pair
- LO signal applied to mixing quad
- IF LPF output
- LO and or RF trap at IF output

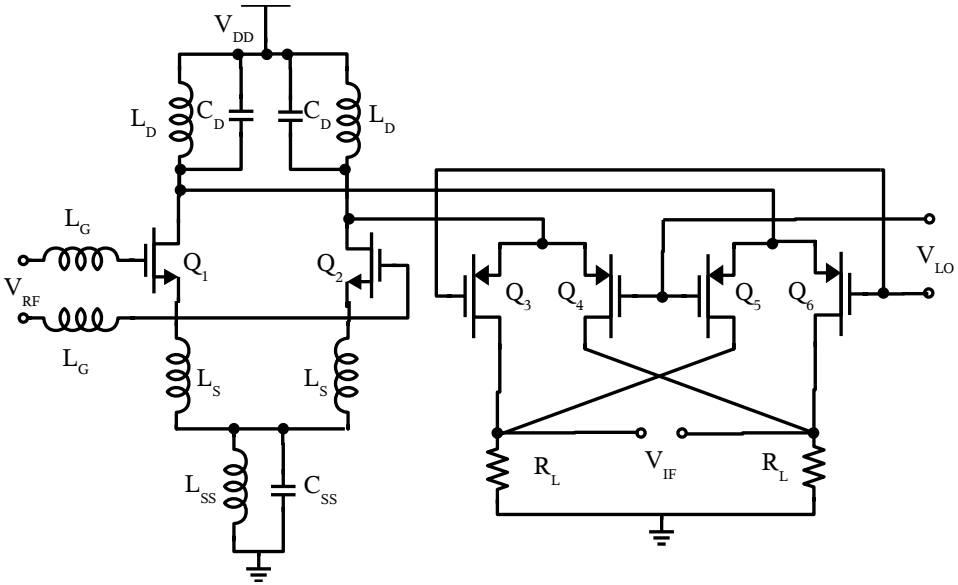
Receive (down-converter) mixer topology

- Image rejection must be placed before mixing quad or built into the topology.

Improved-mixer topologies

- Gilbert cell with transformer coupling of RF and IF signals: lower supply voltage but higher noise and conversion loss
- Folded cascode Gilbert cell (lower supply voltage)
- BiCMOS Gilbert cell with MOS input and HBT quad (better linearity, lower LO swing)

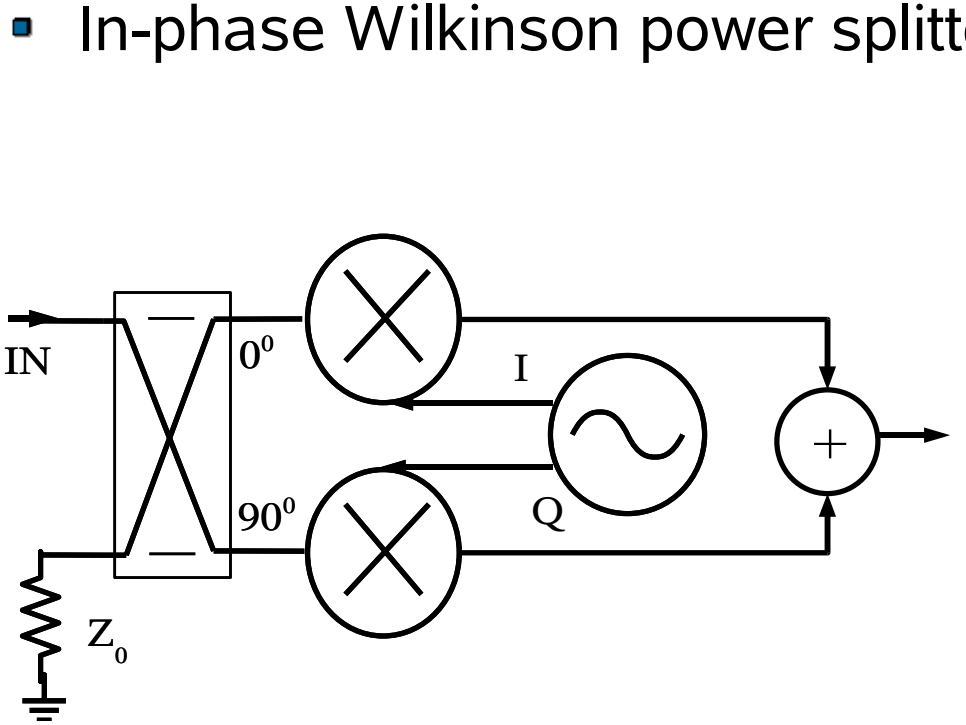


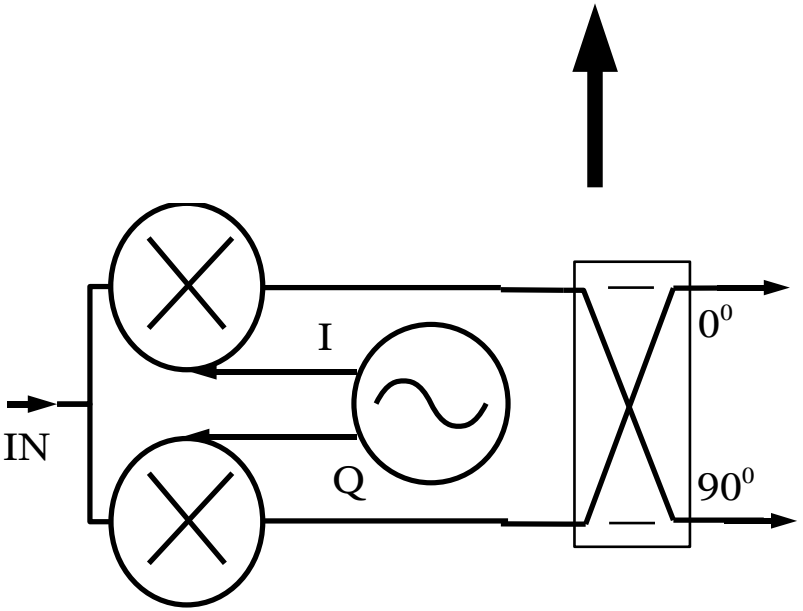


mm-Wave image reject mixer topologies

- Use 90° and 180° hybrid couplers.
  - 90° coupler: Lange or branchline
- 180° coupler: ratrace (Marchand) balun
- In-phase Wilkinson power splitter

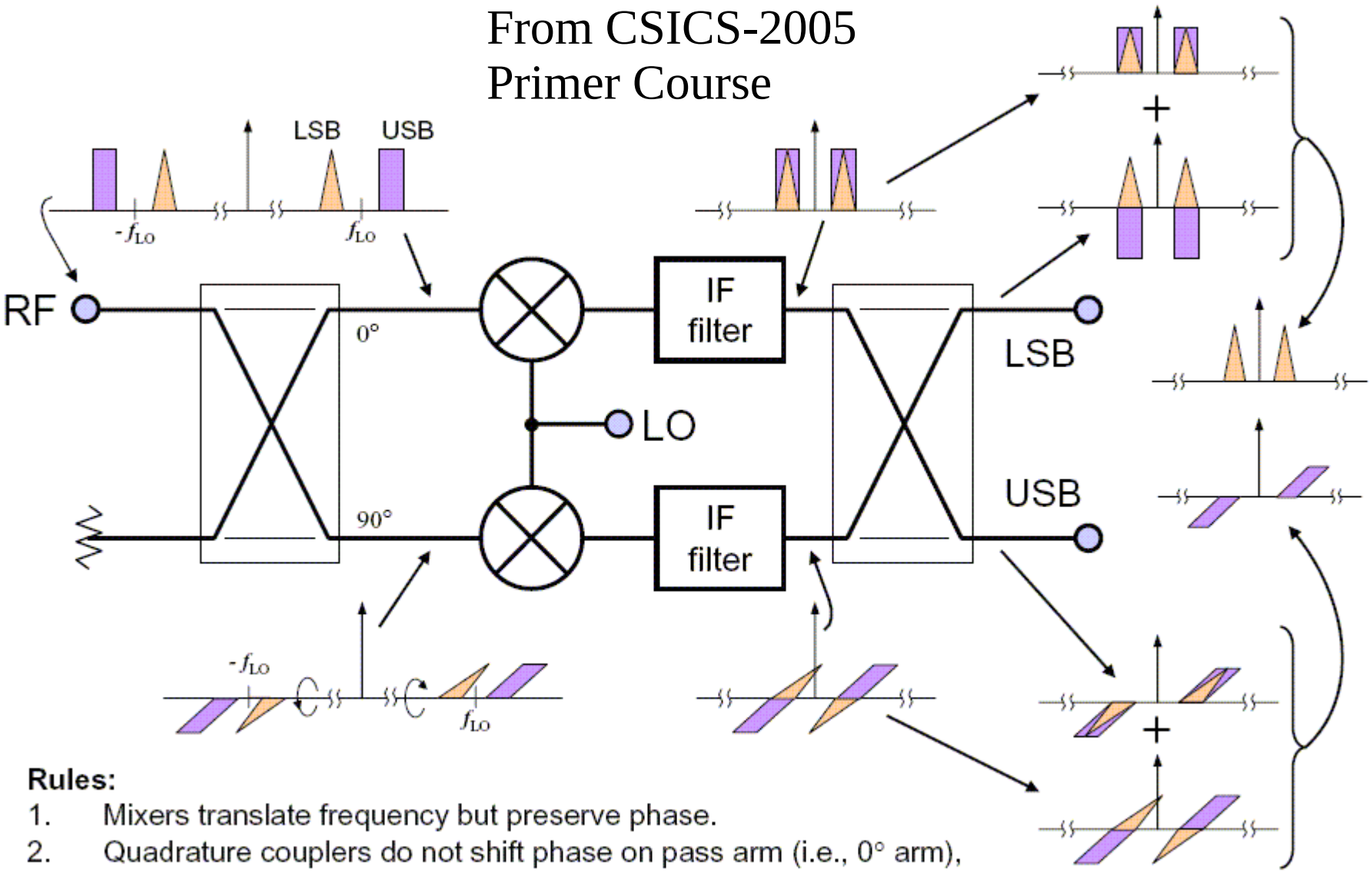
$$[S]=\frac{-1}{\sqrt{2}}\begin{bmatrix} 0 & j & 1 & 0 \\ j & 0 & 0 & 1 \\ 1 & 0 & 0 & j \\ 0 & 1 & j & 0 \end{bmatrix}$$





Pictorial Operation of Quadrature (Image-Rejection) Mixer

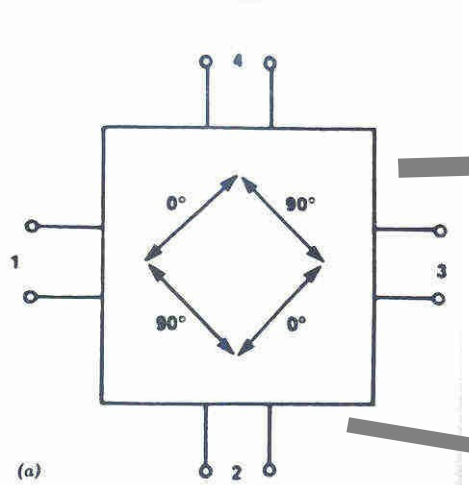
From CSICS-2005
Primer Course

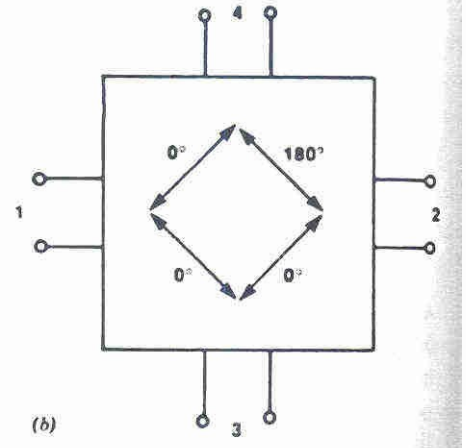


Rules:

1. Mixers translate frequency but preserve phase.
2. Quadrature couplers do not shift phase on pass arm (i.e., 0° arm), but give 90° phase shift through cross arm (i.e., 90° arm).

90^0 and 180^0 hybrid couplers (broadband)





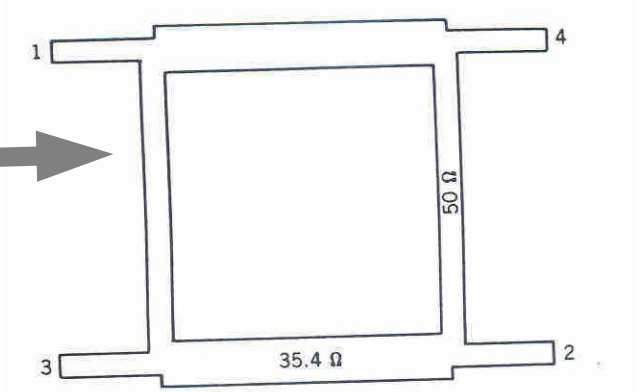
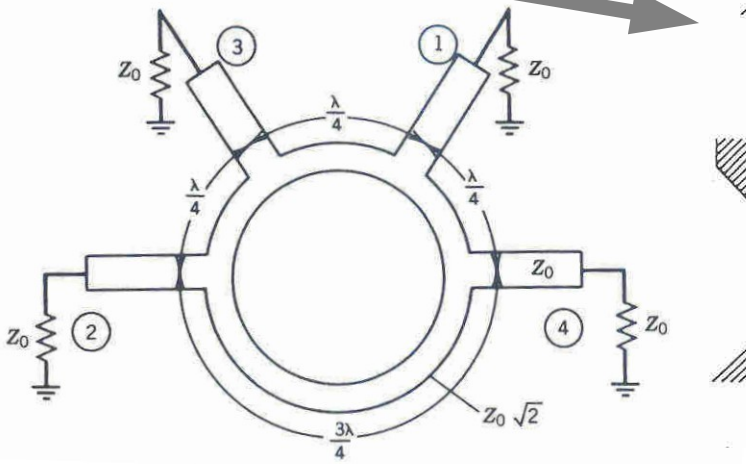
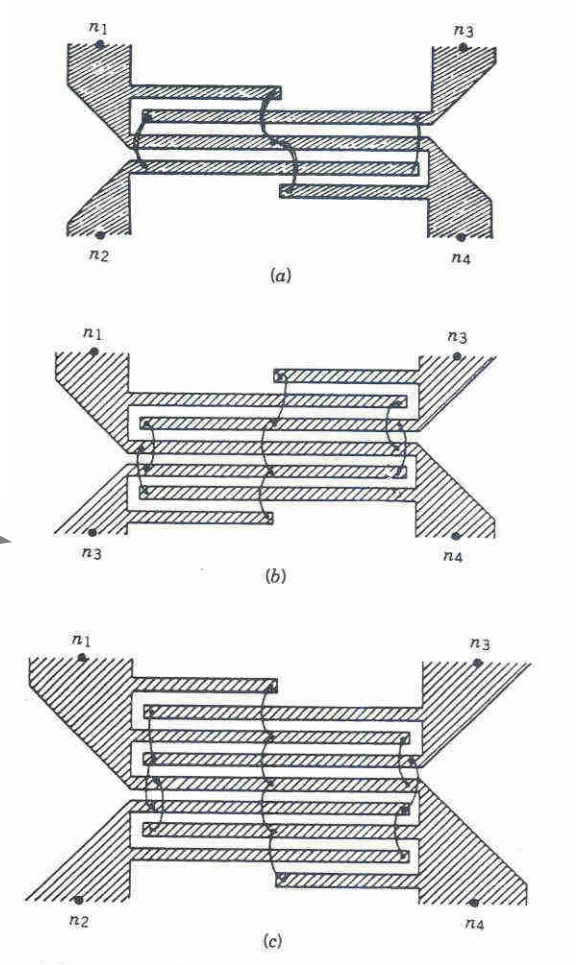


Figure 7.31 Branchline hybrid for 50-Ω system.

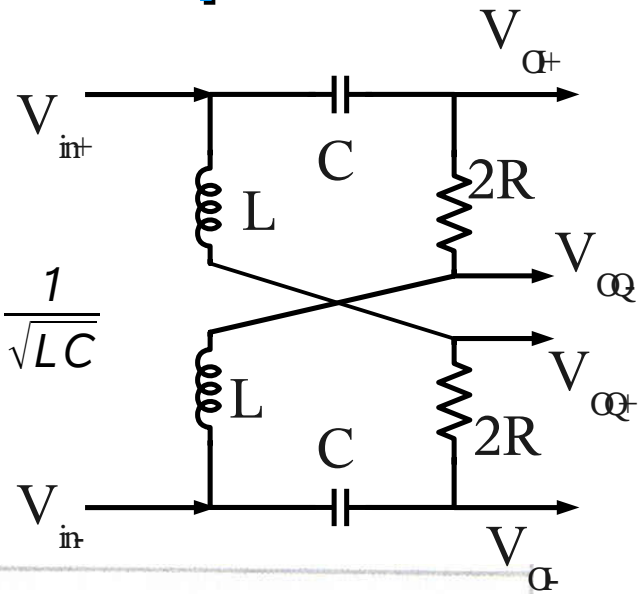


180° Ratrace Coupler

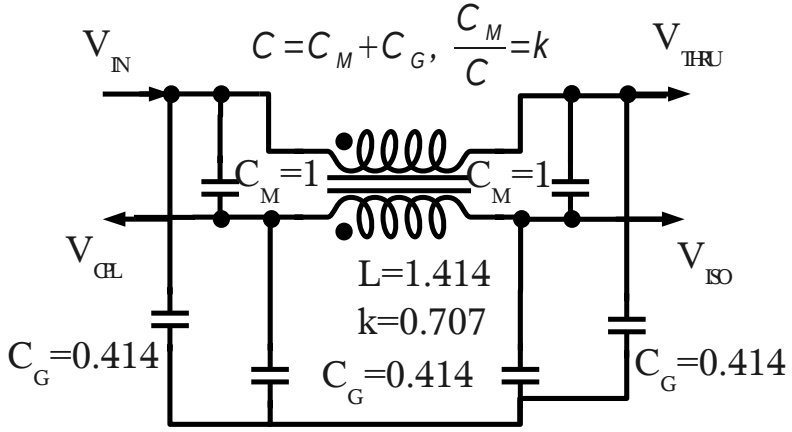


Lange Coupler

90^0 phase shifter (lumped)



$$Q=\frac{\sqrt{\frac{L}{C}}}{R} \text{ and } \omega_0=\frac{1}{\sqrt{LC}}$$



$$\omega_0=\frac{1}{\sqrt{LC\,(1-k^2)}} \qquad Z_0=\sqrt{\frac{L}{C}}$$

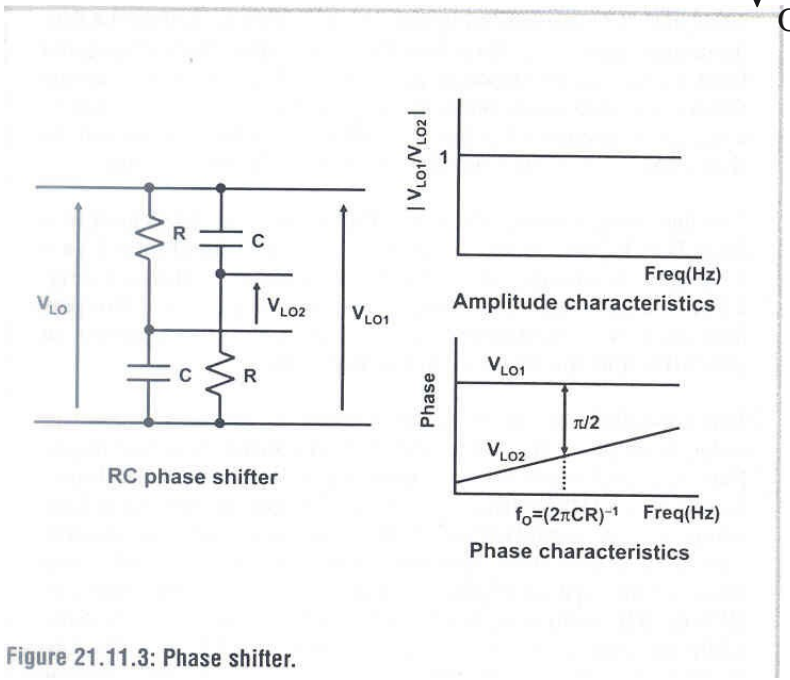


Figure 21.11.3: Phase shifter.

$$\begin{bmatrix} V_{OI+,-} \\ V_{OQ+,-} \end{bmatrix} = V_{in} \times \begin{bmatrix} \dfrac{\pm s^2 + 2\frac{\omega_0}{Q}s - \omega_0^2}{s^2 + 2\frac{\omega_0}{Q}s + \omega_0^2} \\ \dfrac{\mp s^2 - 2\frac{\omega_0}{Q}s - \omega_0^2}{s^2 + 2\frac{\omega_0}{Q}s + \omega_0^2} \end{bmatrix}$$

Low noise mixer design methodology (as for LNA) (S. Voinigescu & M.Maliepaard, ISSCC-1997)

- Bias @ minimum NF current density (if power gain is still adequate at f_{osc}.
- Size transistor for optimal noise resistance - active matching
  - "Source" impedance is the LNA output impedance
- Add inductive emitter degeneration L_E to meet linearity target (more important than noise and conversion gain). MOSFET input is more linear.

Low noise mixer design methodology (II)

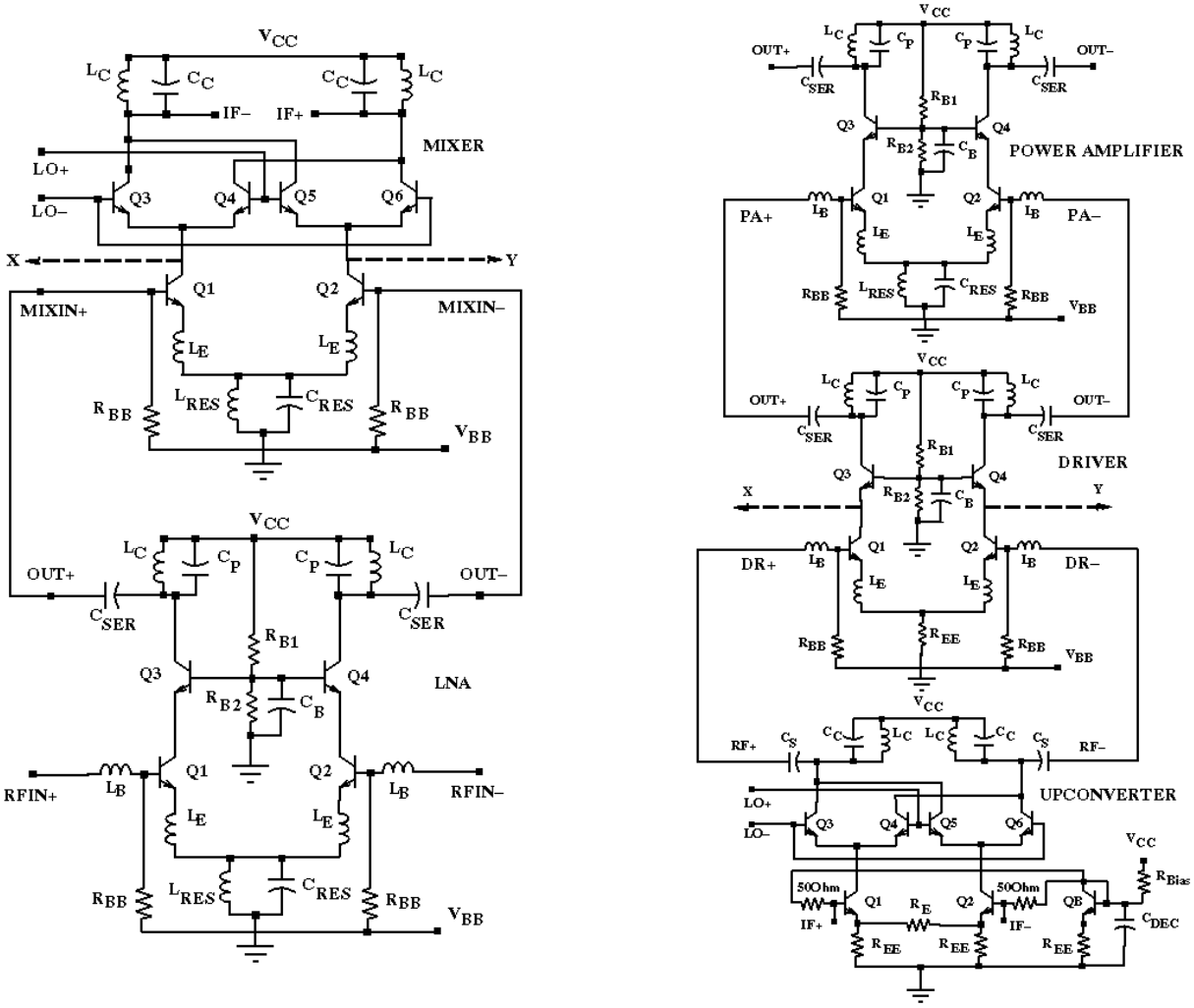
- If mixer is designed for noise matching to impedance Z_o then linearity is given by:

$$IIP_3 \propto \frac{\omega g_m Z_0}{2\pi f_T}; \quad \text{where} \quad L_E = \frac{Z_0}{2\pi f_T}$$

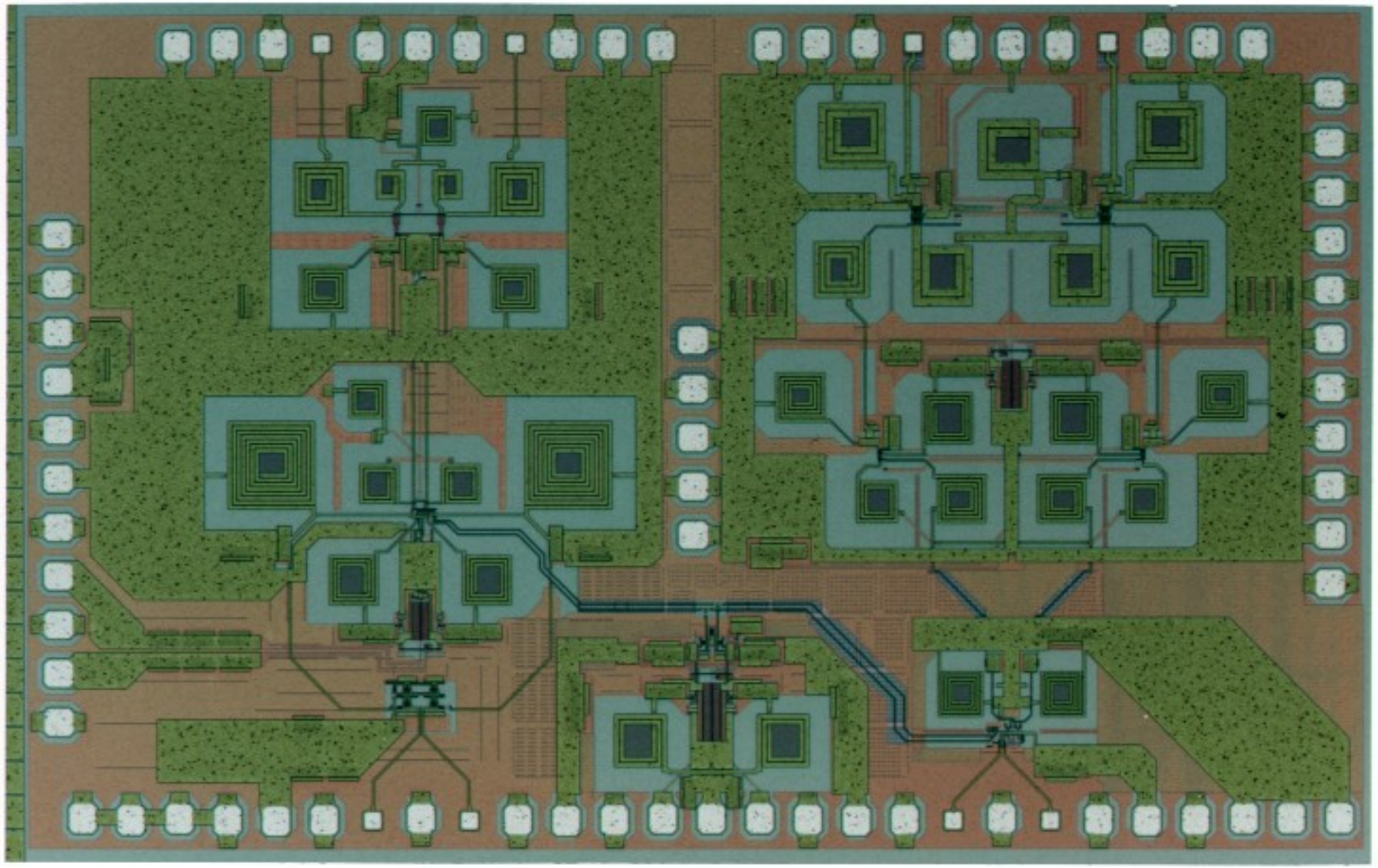
- LO swing must be large enough to fully switch the mixing quad, yet not too large to cause transistor saturation. MOSFET quad is inferior to HBT quad due to larger LO swing requirement.

5-GHz single-chip SiGe radio

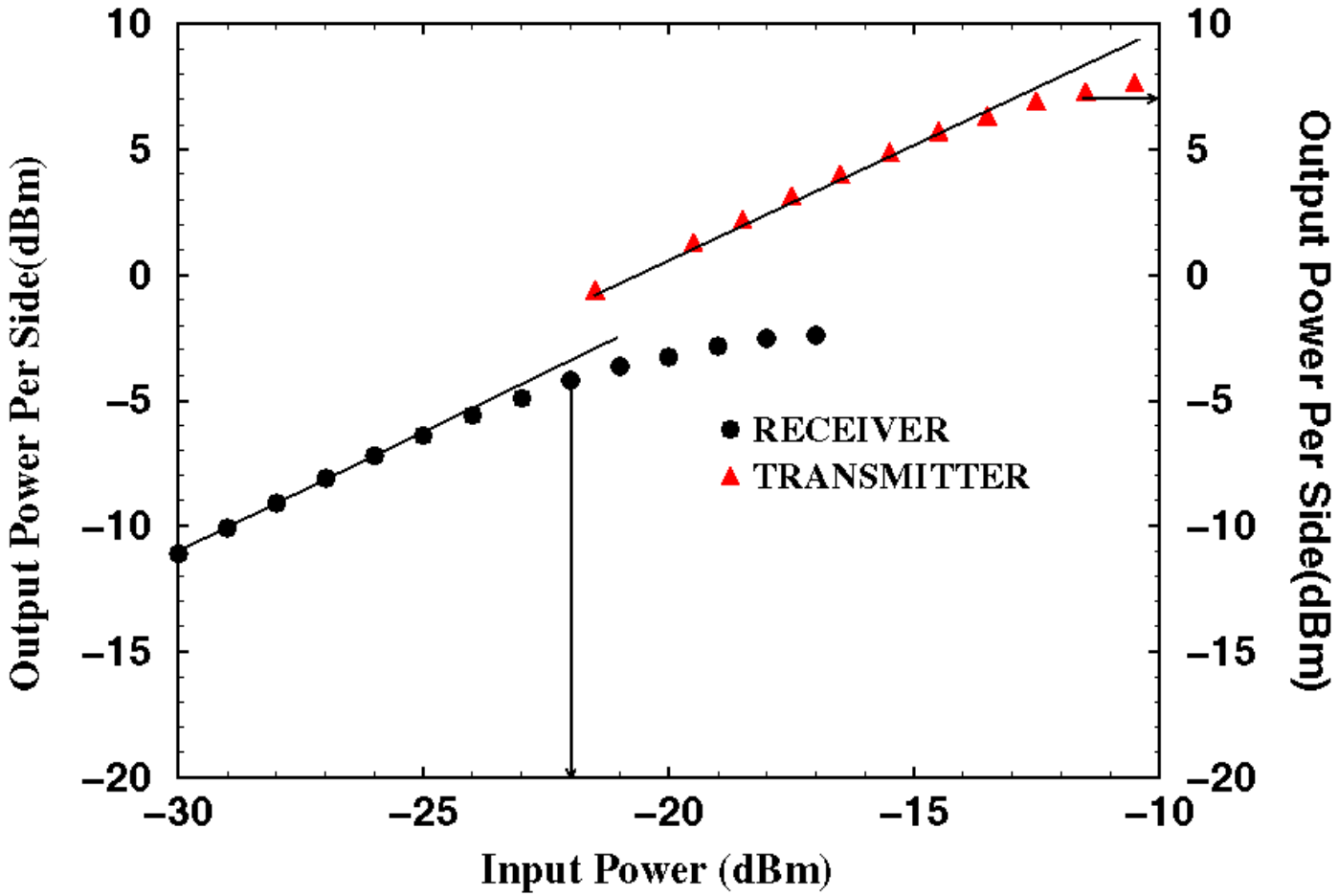
(S.Voinigescu et al. IEEE MTT-S 1999)



5-GHz single-chip SiGe radio

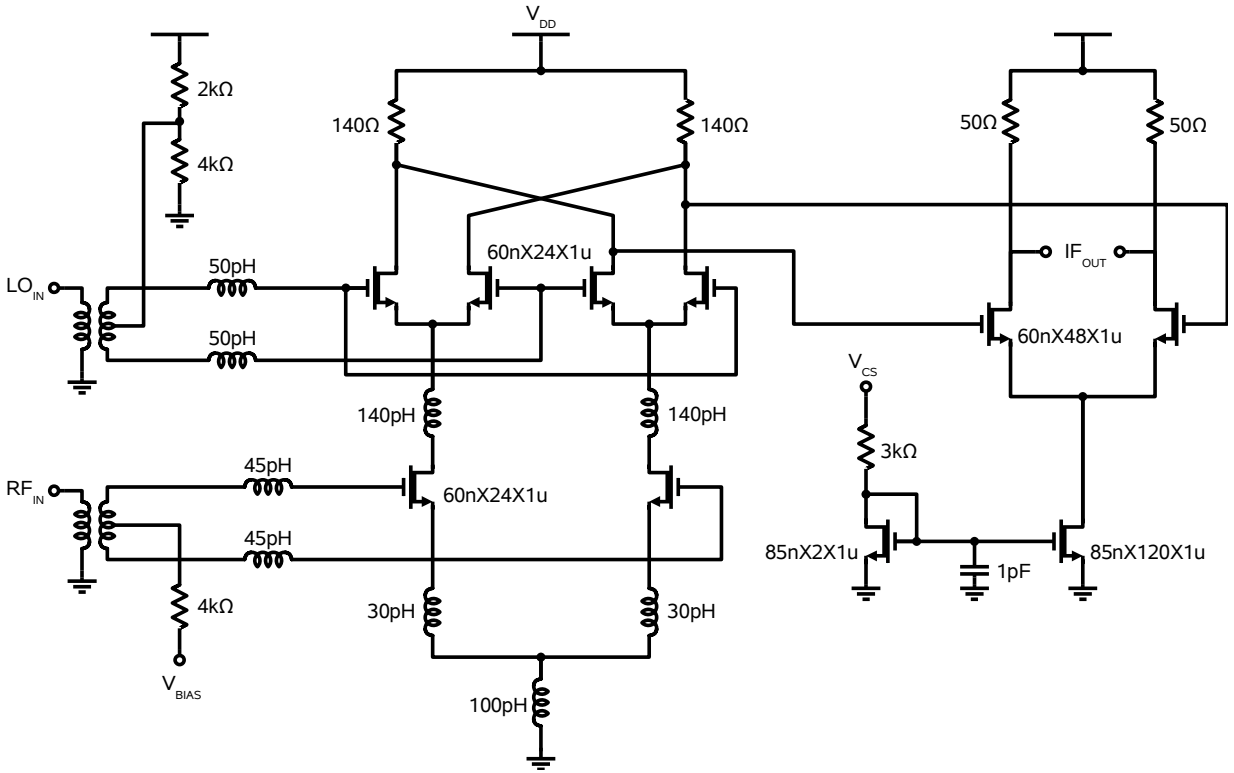


5-GHz SiGe Radio: Rx and TX linearity



mm-Wave Gilbert cell mixer examples

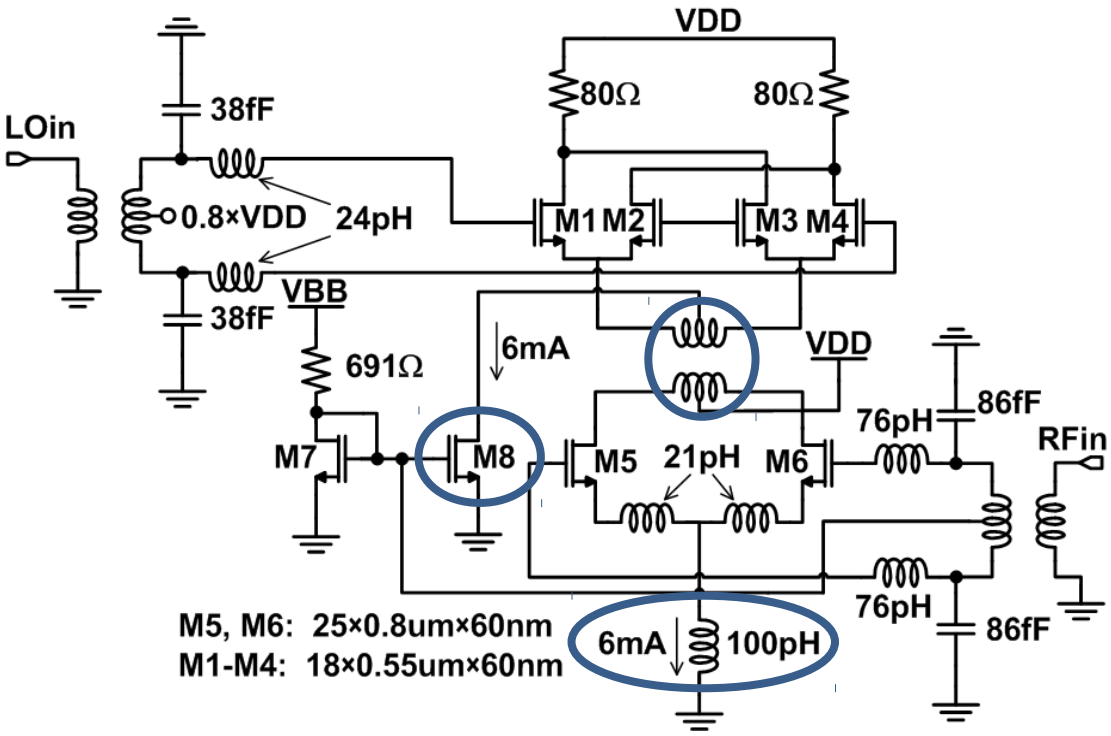
71-95 GHz

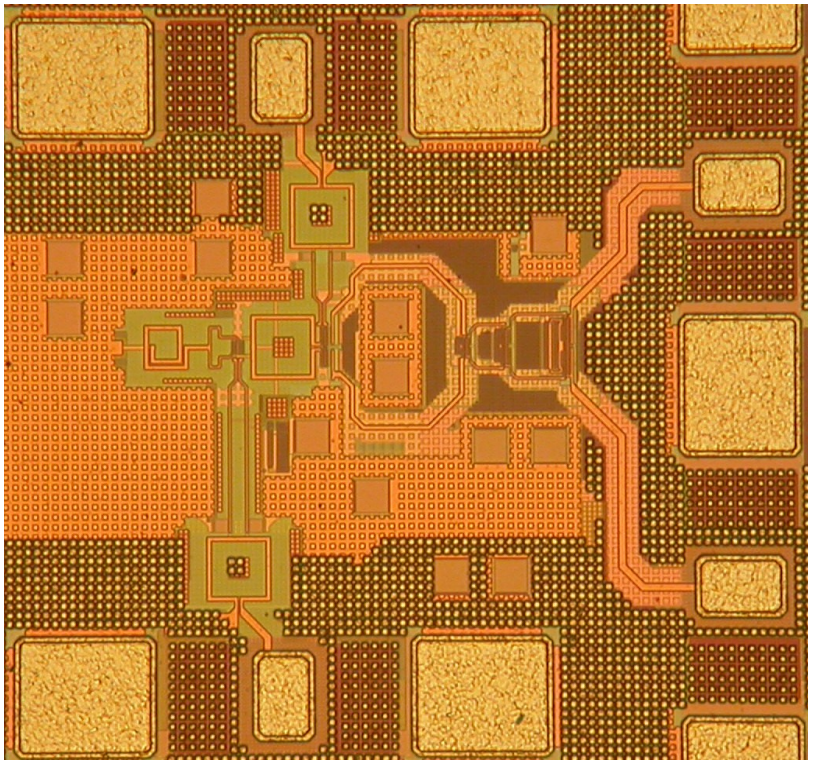


140-GHz Down-Conversion Mixer

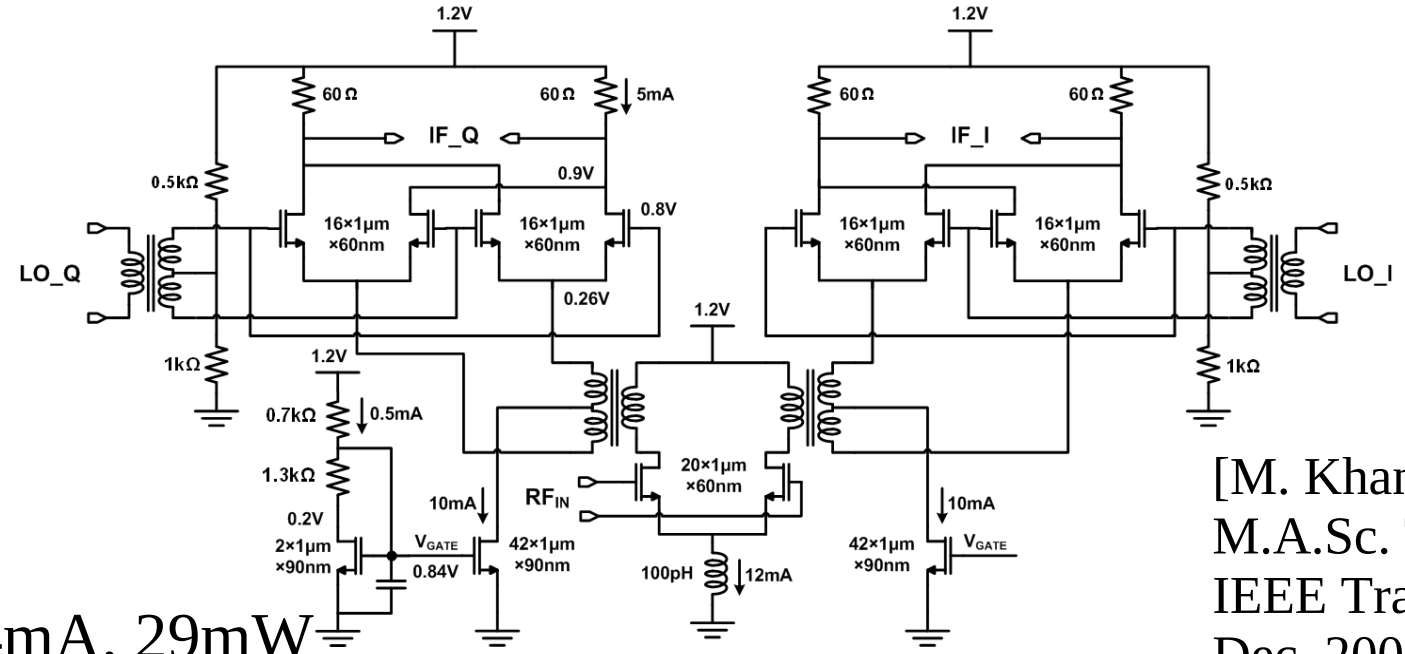
- **Consumes 12 mA from 1.2V (14.4 mW)**

[S. Nicolson RFIC-08]



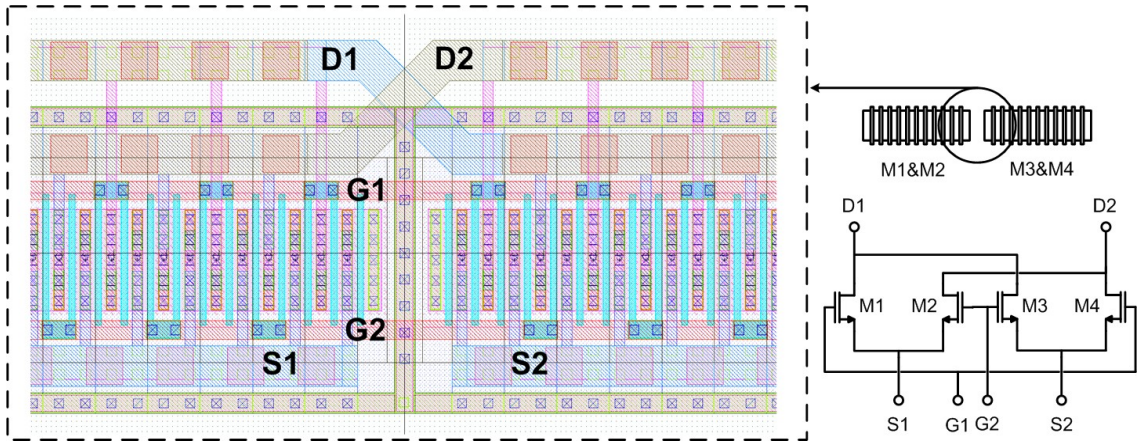


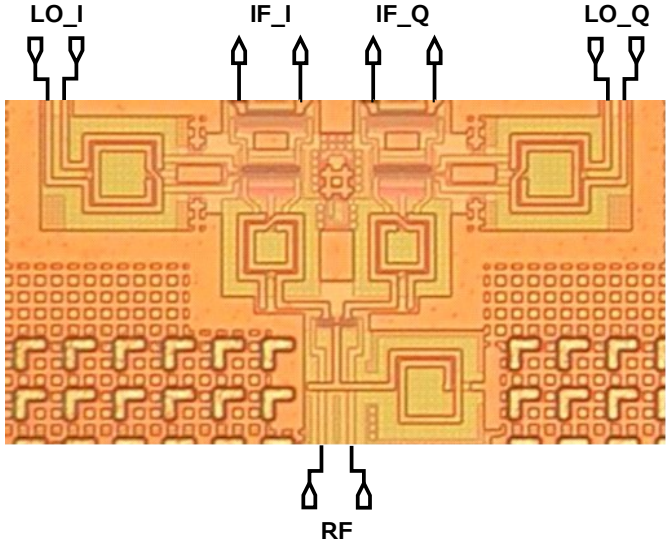
100-GHz IQ Down-Conversion Mixer



24mA, 29mW

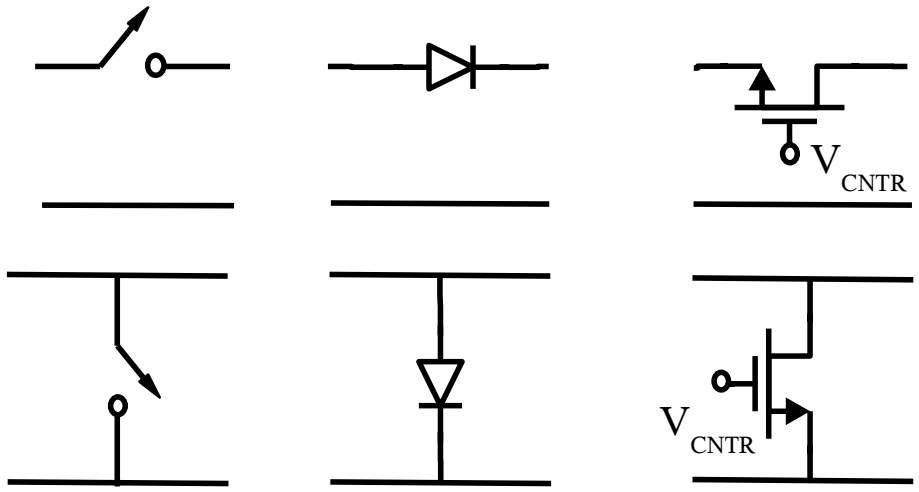
[M. Khanpour, M.A.Sc. Thesis 2008 IEEE Trans. MTT, Dec. 2009]





Switches

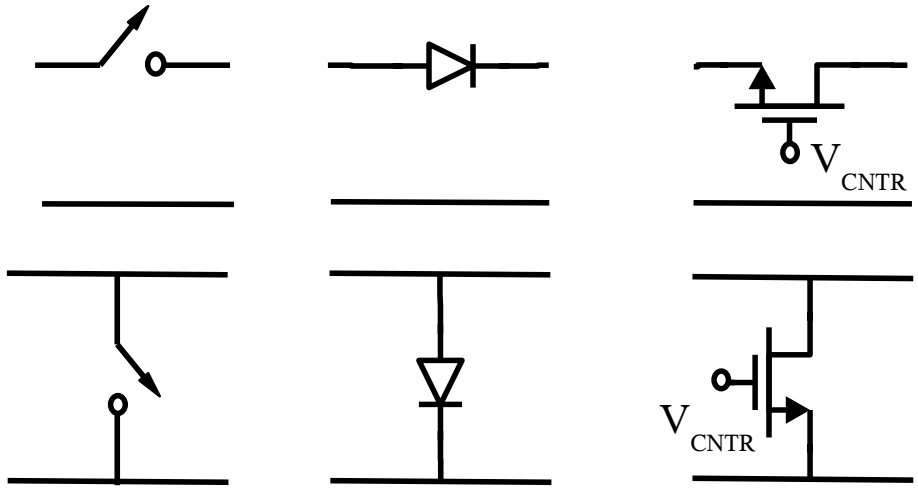
- PIN and Schottky diodes, FETs
- Ideally:
  - R_{on}=0, R_{off} = ∞, C=0
  - High isolation when off
  - low insertion loss when on
- Topologies:
  - Shunt, series, series-shunt
- Used as antenna switches



Switches

$$IL = -20 \cdot \log_{10}\left(1 + \frac{R_{SW}}{2Z_0}\right)$$

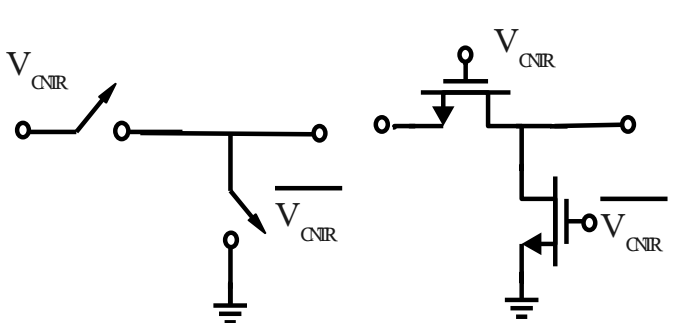
$$I = 10 \cdot \log_{10}\left[1 + (4\pi f C_{SW} Z_0)^{-2}\right]$$

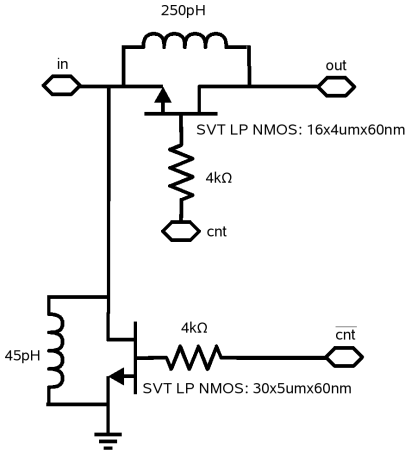


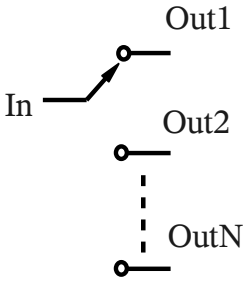
$$IL = 10 \cdot \log_{10}\left[1 + (\pi f C_{SW} Z_0)^{2}\right]$$

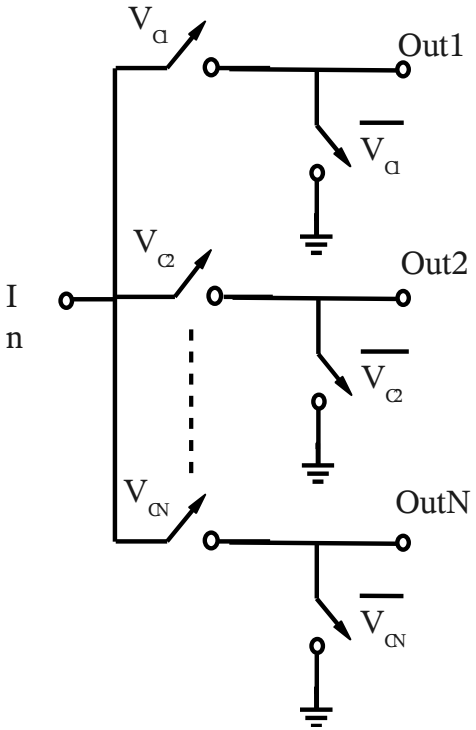
$$I = -20 \cdot \log_{10}\left(\frac{2R_{SW}}{2R_{SW} + Z_0}\right)$$

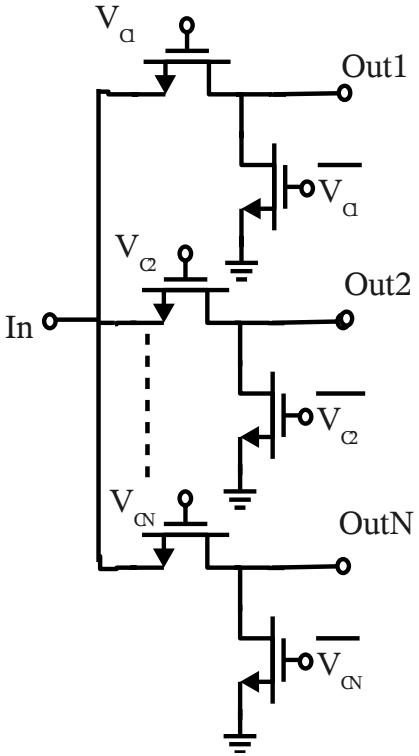
CMOS mm-wave switch examples







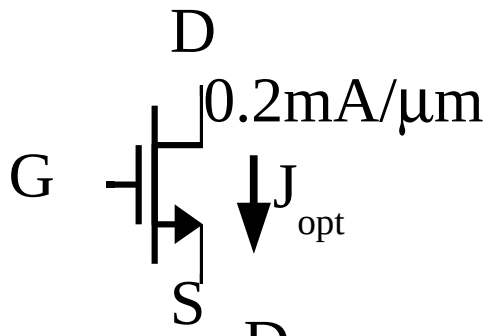


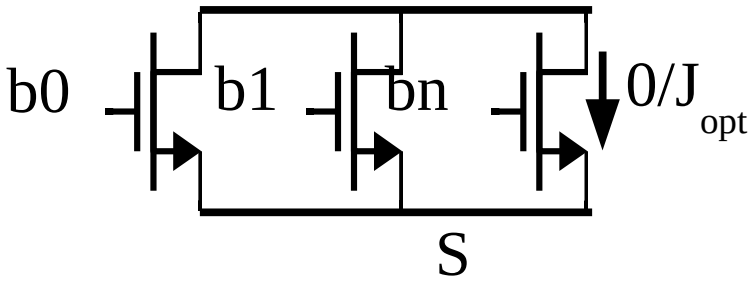


Binary-Weighted Geometry

Idea: Shared source and drain, segmented gates

- varactor, PA (R.B. Staszewski, 2006)
- transistor: digitally-controlled attenuator
- Gilbert-cell biased at constant J_{DS}
  - digitally-controlled gain cells
  - digitally-controlled phase shifters
  - mm-Wave IQ DACs

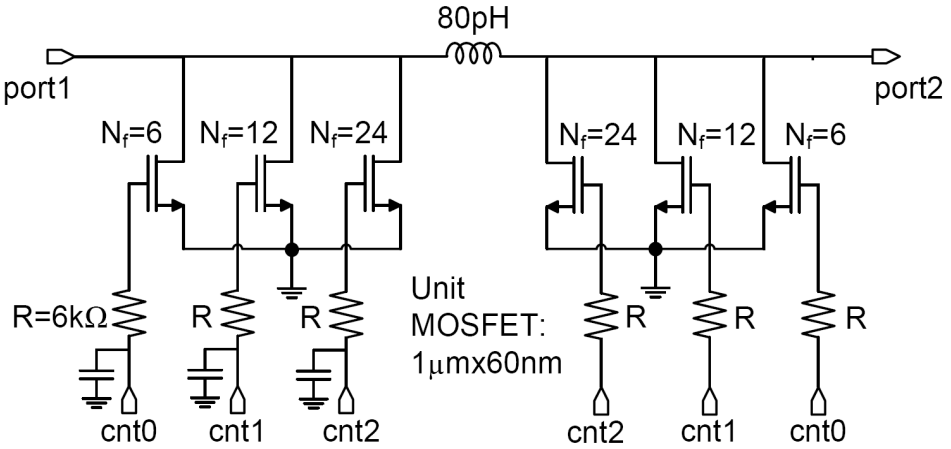




$0 < V_G < 1$

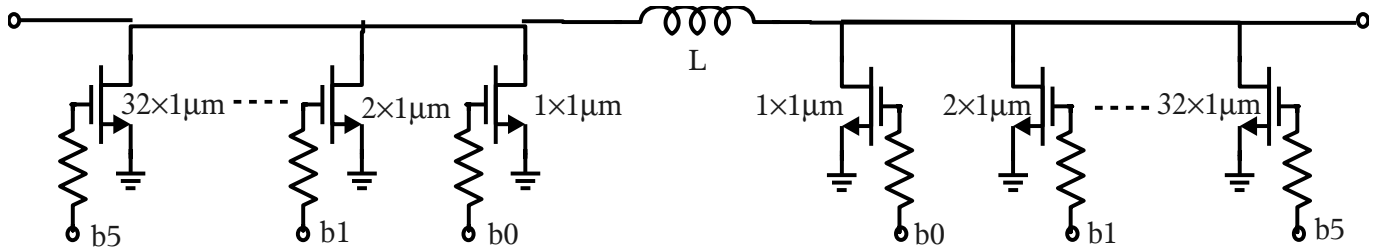
$b_0, b_1, .. b_n$ ="0" or "1"

Binary-Weighted Atten./Switch



[A. Tomkins et al. CSICS-08]

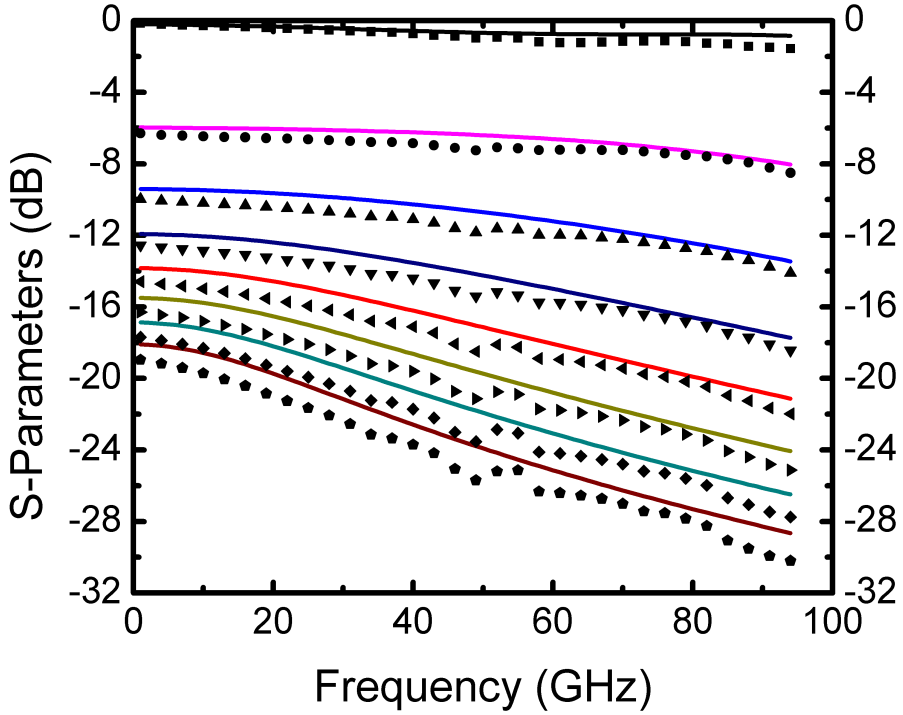
C_{OFF} = 1fF/μm, 42μm

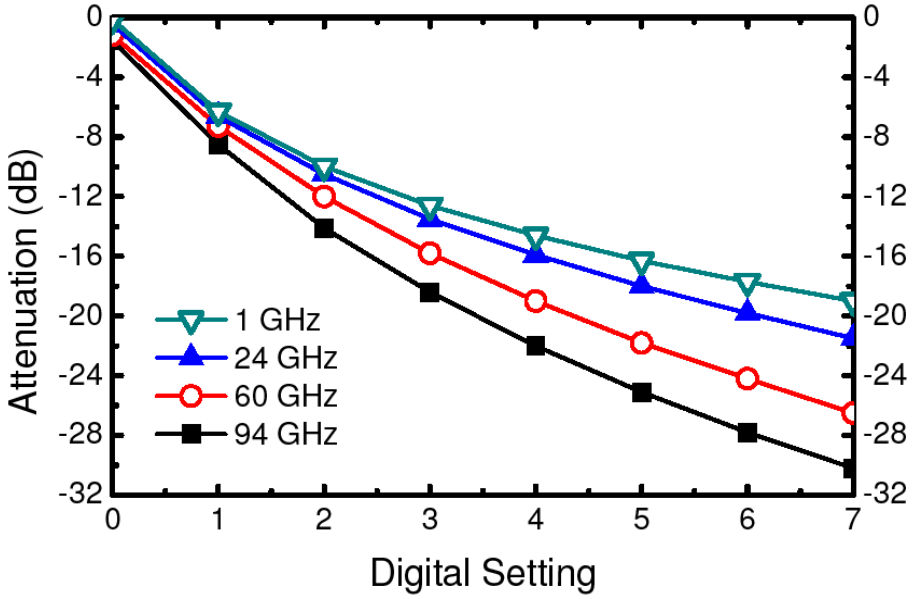


$$R_{SHUNT} = \frac{R_{unit}}{\left(b_0 + b_1 2 + b_2 2^2 + \ldots + b_{n-1} 2^{n-1}\right)}$$

$$IL = 20 \cdot \log\left(1 + \frac{Z_0}{2R_{SW}}\right) = 20\log\left[1 + \frac{25}{R_{unit}}\left(b_0 + b_1 2 + b_2 2^2 + .. + b_{n-1} 2^{n-1}\right)\right]$$

Measurement Results

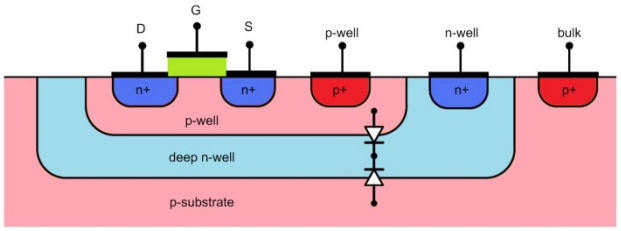


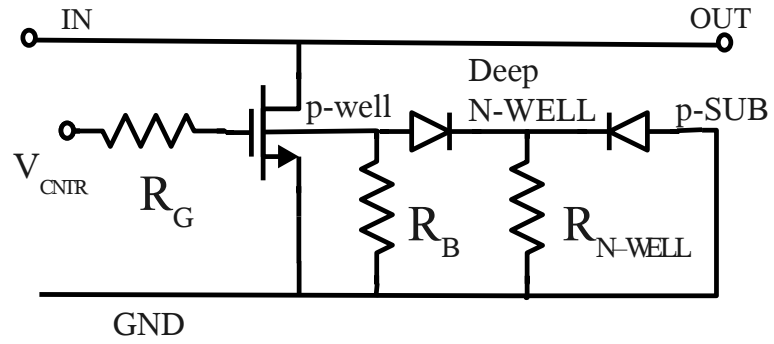


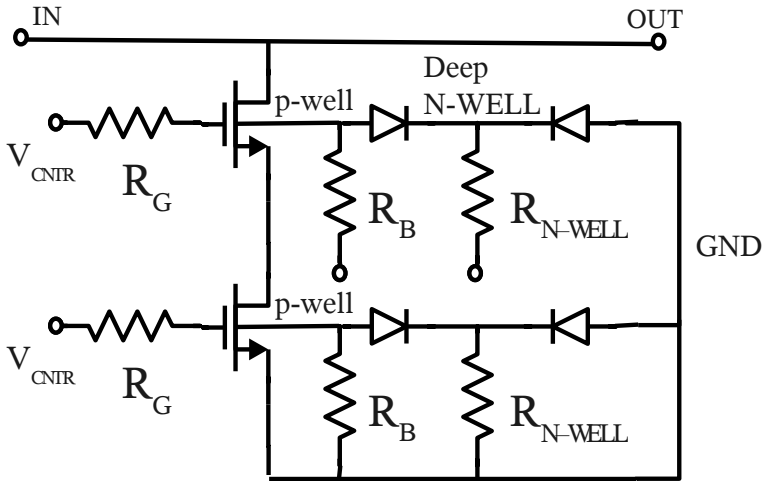
IL<2 dB, ISOL>20dB up to 94 GHz

P_{1dB}>+10dBm

Improving the CMOS switch



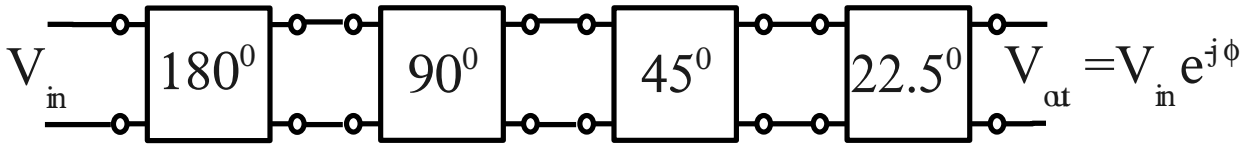




- Use deep N-well to reduce capacitance
- Use large resistor is series with gate, substrate and n-well to reduce loss and improve linearity
- Stack transistors for improved linearity

Phase shifters

$$\phi = b_0 22.5^0 + b_1 45^0 + b_2 90^0 + b_3 180^0$$



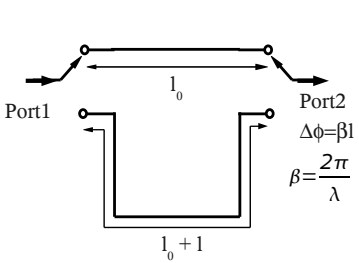
$b_3=(0,1)$ $b_2=(0,1)$ $b_1=(0,1)$ $b_o=(0,1)$

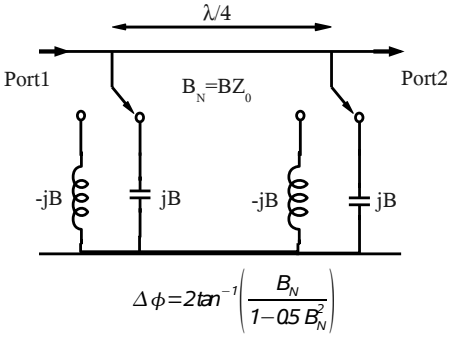
$$[S]_{PS} = \begin{bmatrix} 0 & e^{-j\phi} \\ e^{-j\phi} & 0 \end{bmatrix}$$

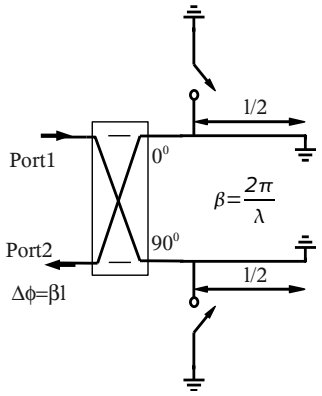
Each cell can be implemented as:

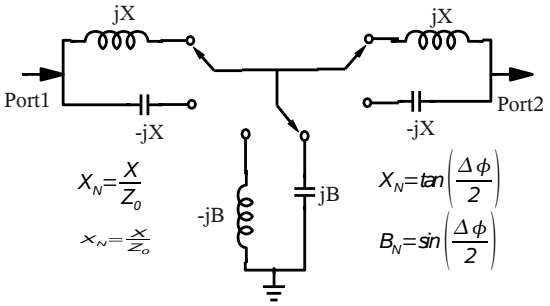
- Switched line
- Hybrid-coupled
- Loaded line
- High-pass low-pass

Can have analog or digital control

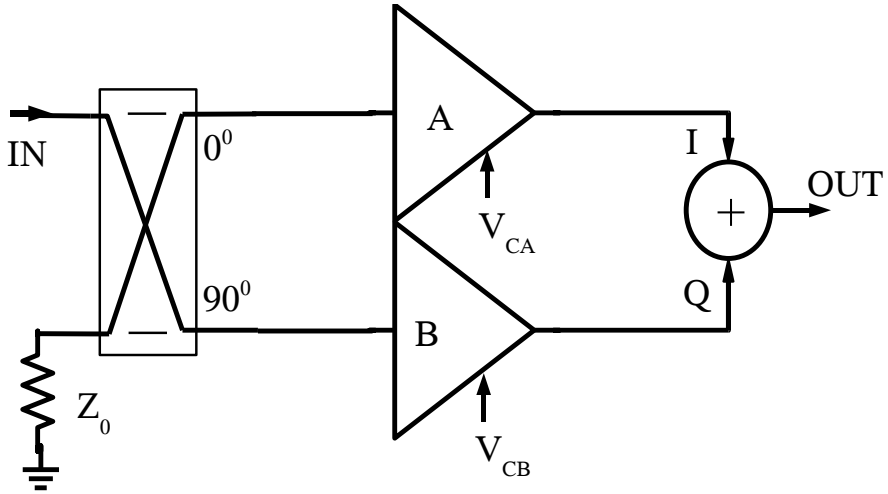


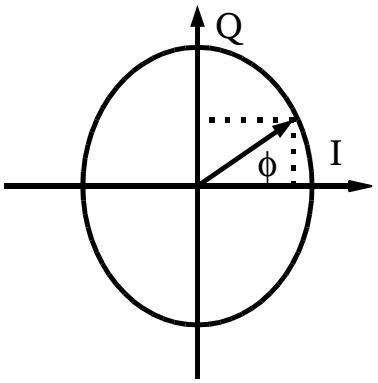


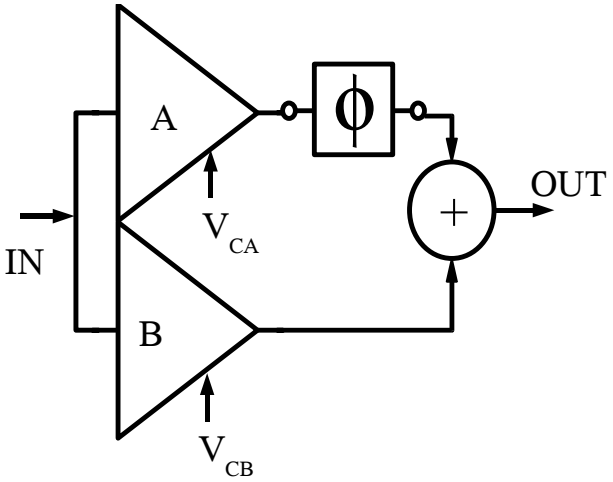


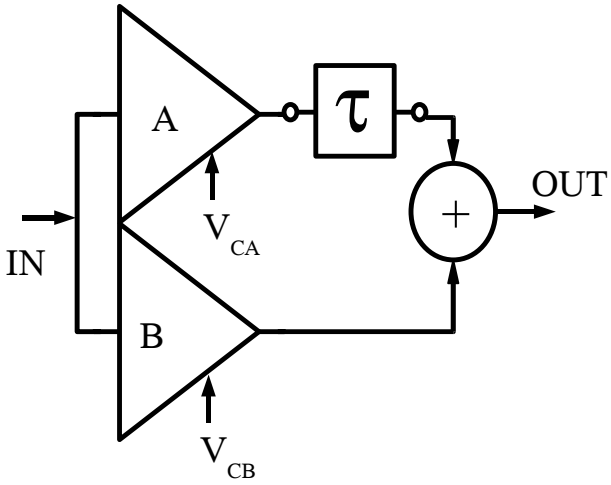


Cartesian and VGA-based phase shifters



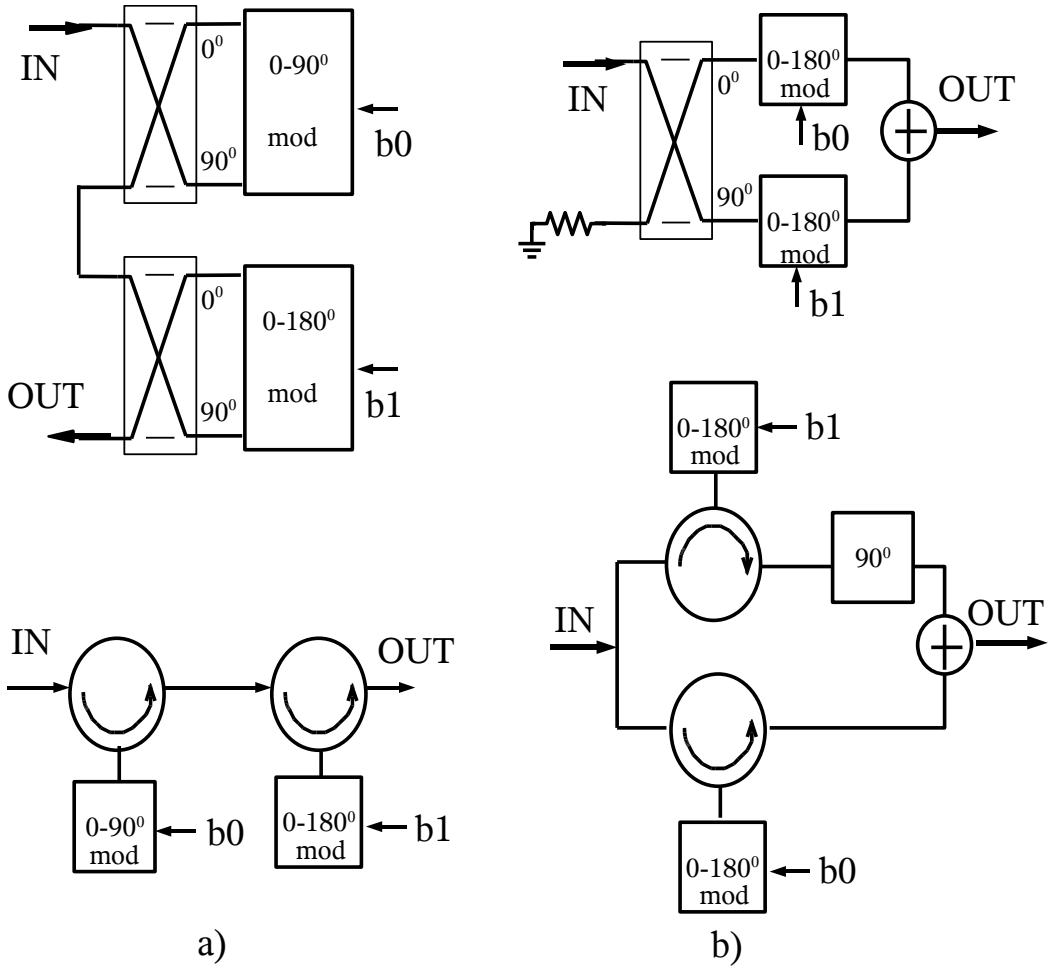






$$OUT = I + jQ = |OUT| e^{j\phi} \qquad |OUT| = \sqrt{I^2 + Q^2} \qquad \phi = \tan^{-1}\left(\frac{Q}{I}\right)$$

Modulators



Require: phase shifters, hybrid couplers or isolators or a Gilbert cell

Transformer-Coupled Gilbert Cell

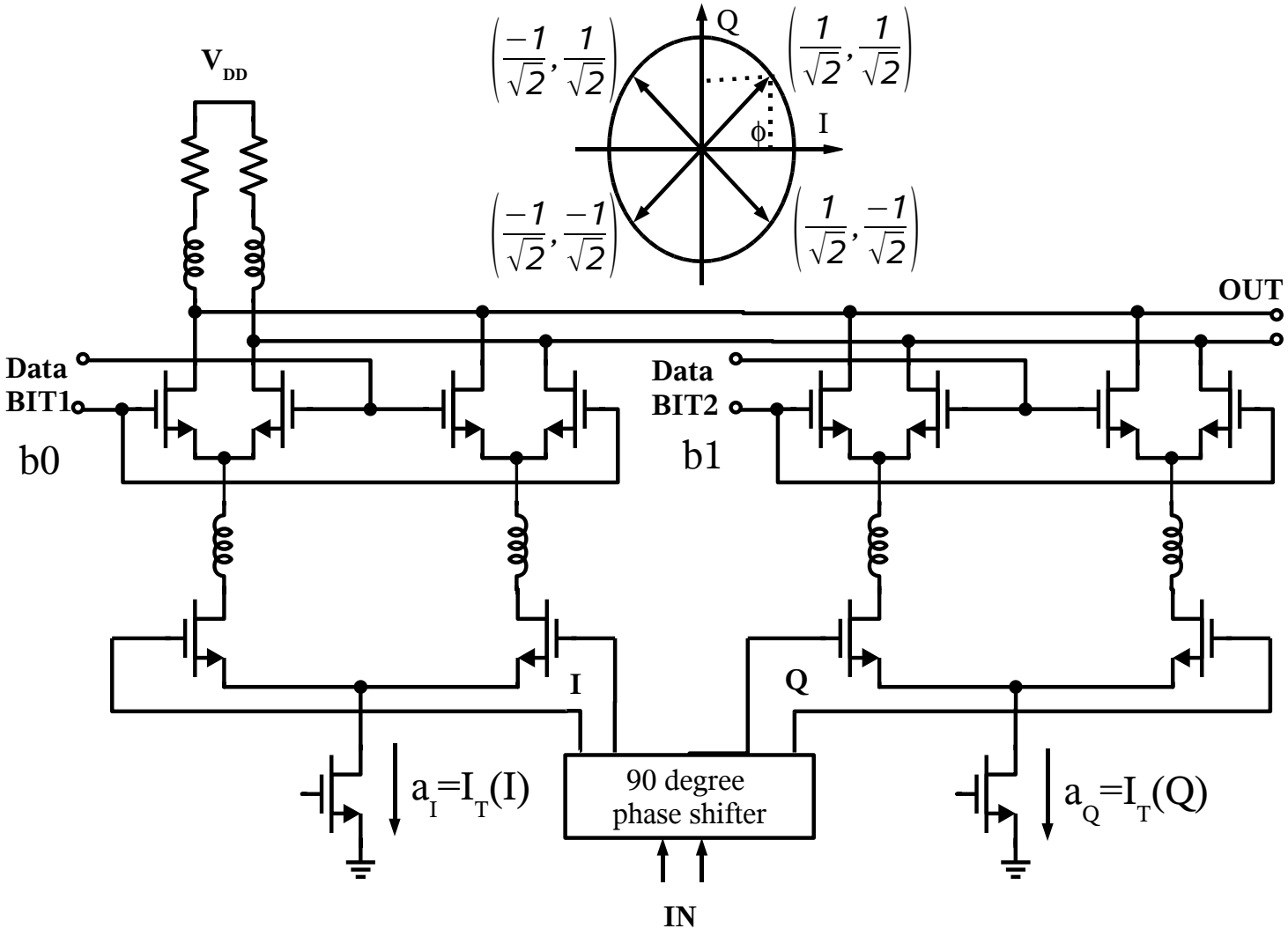
BPSK Modulator

[A.Tomkins CICC-08]

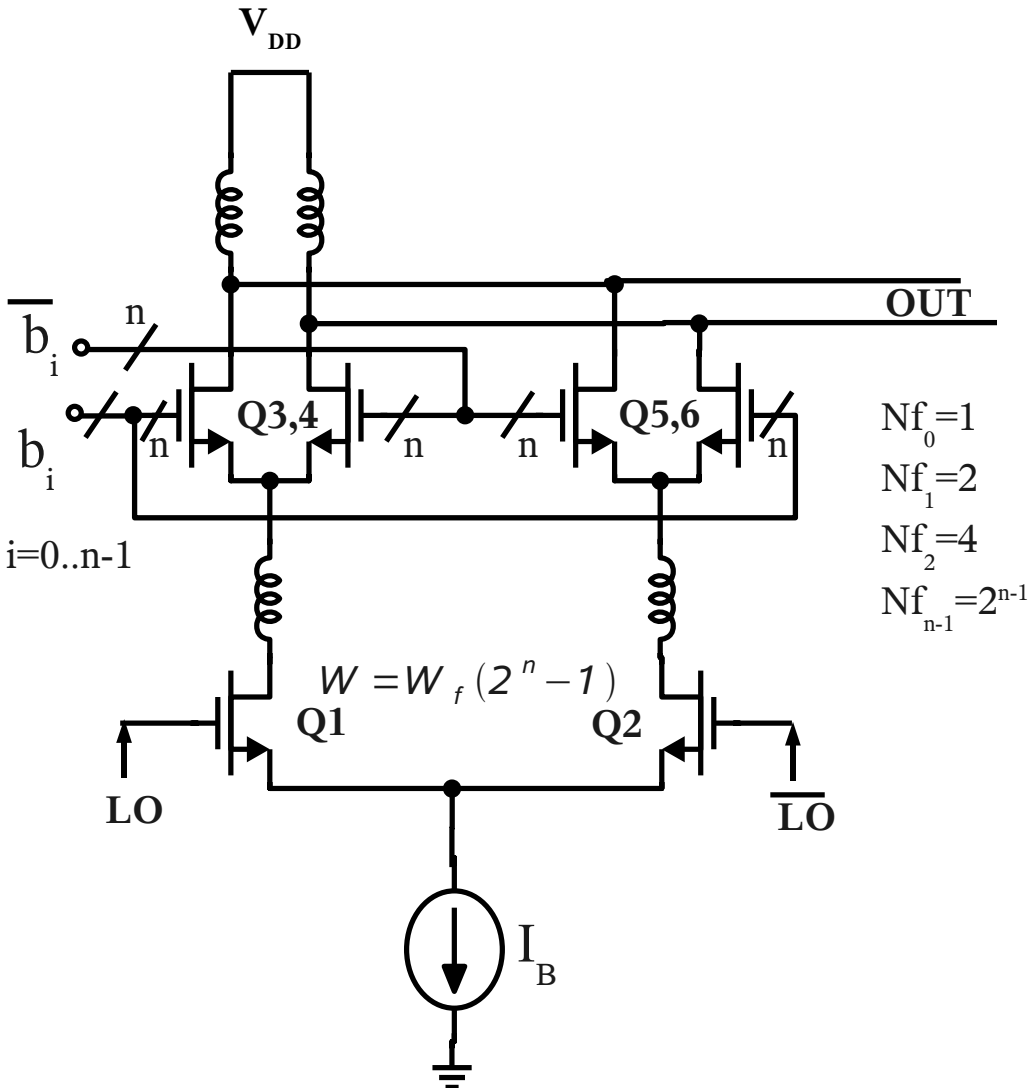
Mixer

Xfmr coupling favoured over capacitor coupling

QPSK, m-ary QAM modulators



Binary-weighted DAC/VGA



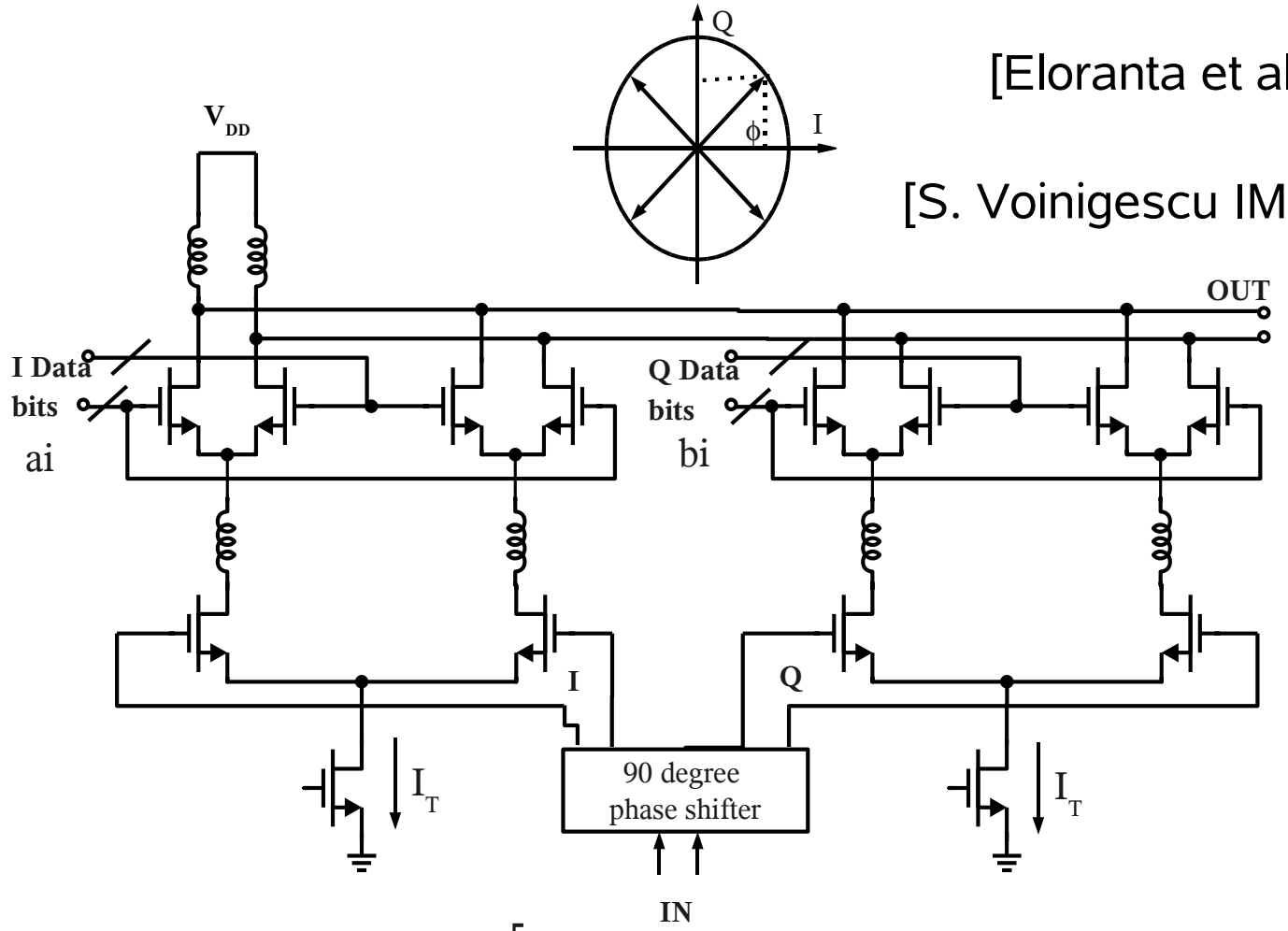
- Binary-weighted or segmented BPSK mods. in parallel
- $Q_{3\text{-}6}$ binary-weighted gate fingers
- $Q_{1,2}$ biased at 0.3 mA/μm
- $Q_{3\text{-}6}$ switch from 0 to 0.3mA/μm
- Load current, impedance remain constant

$$V_{OUT} = g'_m W_f Z_L V_{LO} \sum_{i=0}^{n-1} (-1)^{b_i} 2^i = f(V_{LO}) \times g_w$$

mm-Wave IQ DAC/Phase Rotator

[Eloranta et al, JSSC-07]

[S. Voinigescu IMS-08 Workshop]



$$V_{OUT} = g'_m W_f Z_L V_{IN} \left[\cos(\omega t) \sum_{i=0}^{n-1} (-1)^{a_i} 2^i + j \sin(\omega t) \sum_{i=0}^{n-1} (-1)^{b_i} 2^i \right]$$

Summary

- Mixer performs the fundamental frequency translation function
- Switches are critical building blocks for mixers, antenna switches, phase shifters and modulators
- Gilbert cell is the most common mixer topology today
- Gilbert cell employed to realize VGA, modulators and phase shifters
- Binary-weighted layout allows fine digital control/correction of all mm-wave blocks .