
Digital Design: A Systems Approach

Lecture 12: Timing

Readings

- L12: Chapter 15
- L13: Chapter 27 & 28

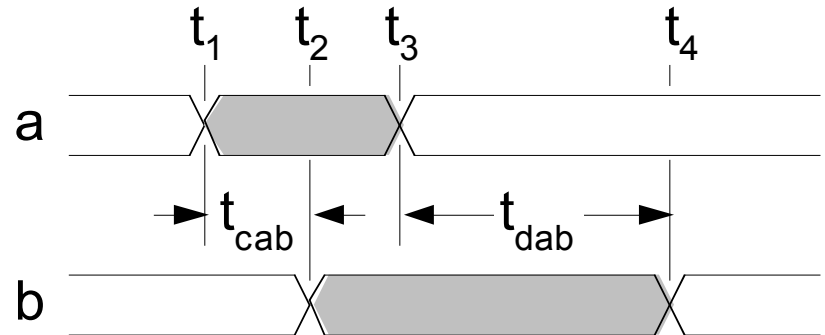
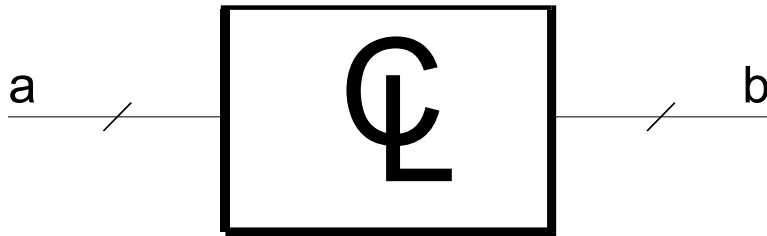
Timing

- How fast can a system run?
- Will it work at any speed?

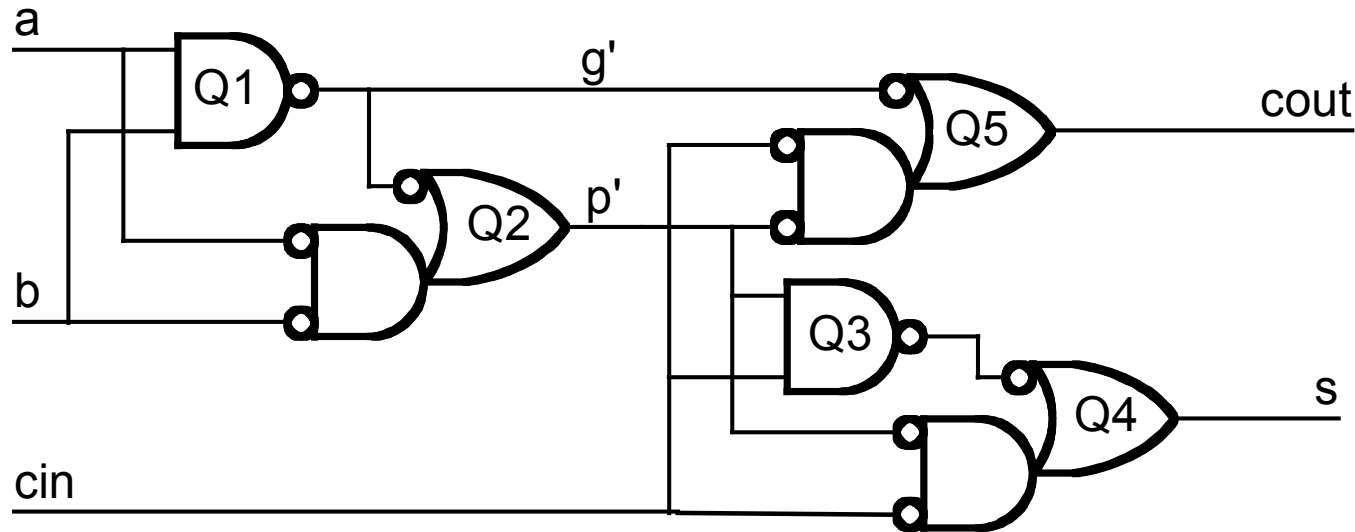
Propagation Delay and Contamination Delay

Propagation Delay – Time from last input change until last output change. (Input at steady state to output at steady state.)

Contamination Delay – Time from first input change until first output change. (Input contaminated to output contaminated)



Example, Contamination and Propagation Delay of Full Adder



Gate	Delay (ps)
Nand2	80
OAI21	120

min	a,b	cin
g'	80	-
p'	120	-
cout	200	120
U3	200	80
s	240	120

max	a,b	cin
g'	80	-
p'	200	-
cout	320	120
U3	280	80
s	400	200

What is

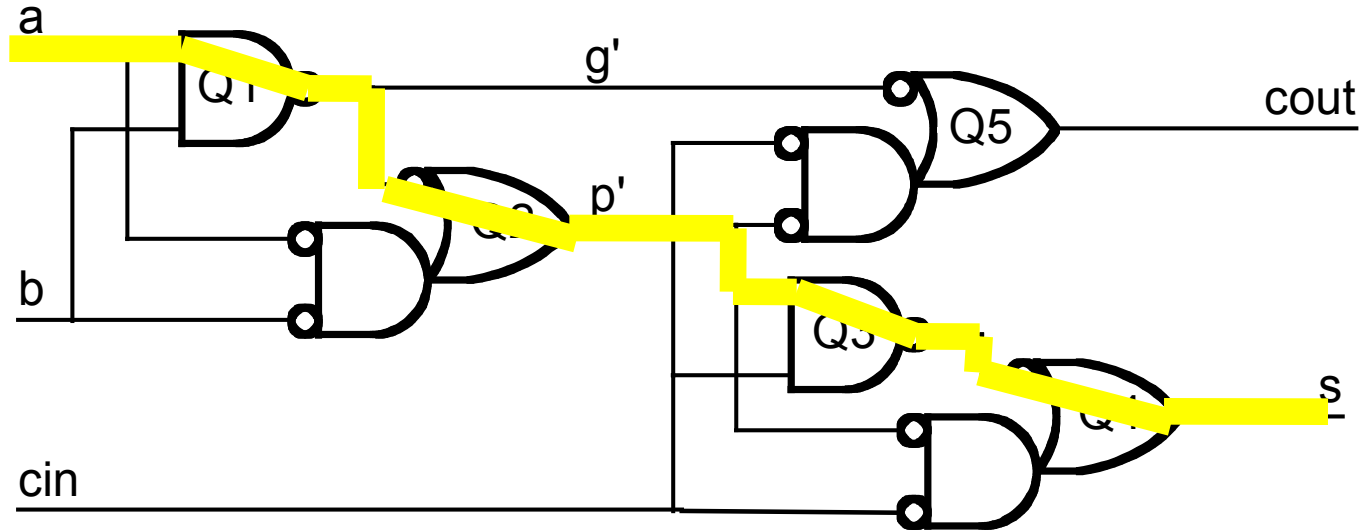
t_{das}

t_{cas}

t_{dcs}

t_{ccc}

Example, Contamination and Propagation Delay of Full Adder



Gate	Delay (ps)
Nand2	80
OAI21	120

min	a,b	cin
<i>g'</i>	80	-
<i>p'</i>	120	-
<i>cout</i>	200	120
U3	200	80
<i>s</i>	240	120

max	a,b	cin
<i>g'</i>	80	-
<i>p'</i>	200	-
<i>cout</i>	320	120
U3	280	80
<i>s</i>	400	200

What is

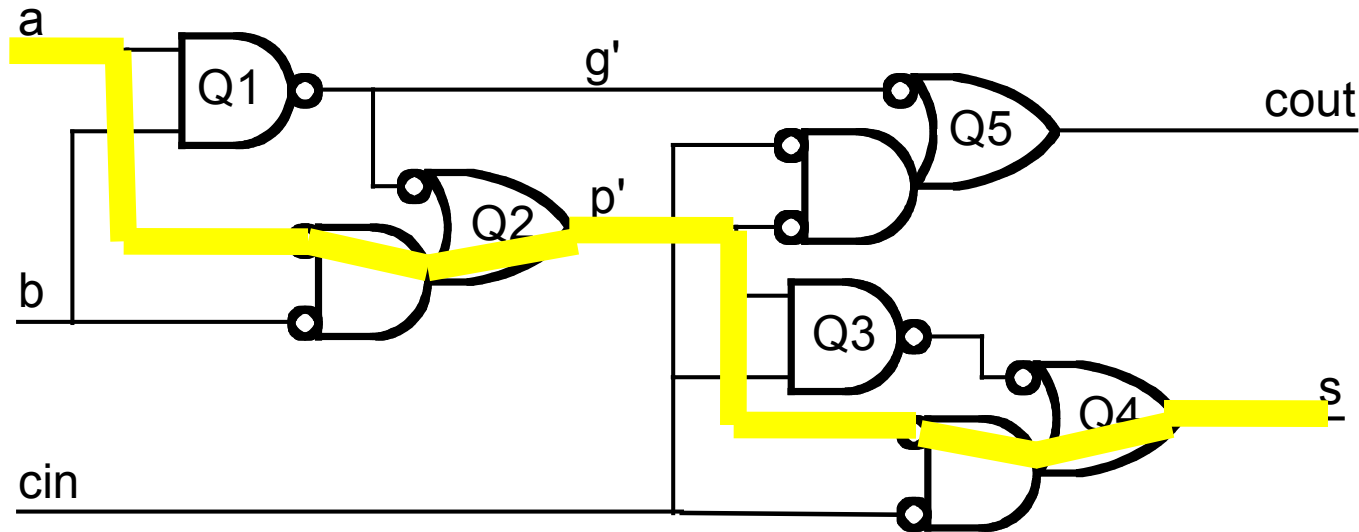
t_{das}

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Example, Contamination and Propagation Delay of Full Adder



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What is

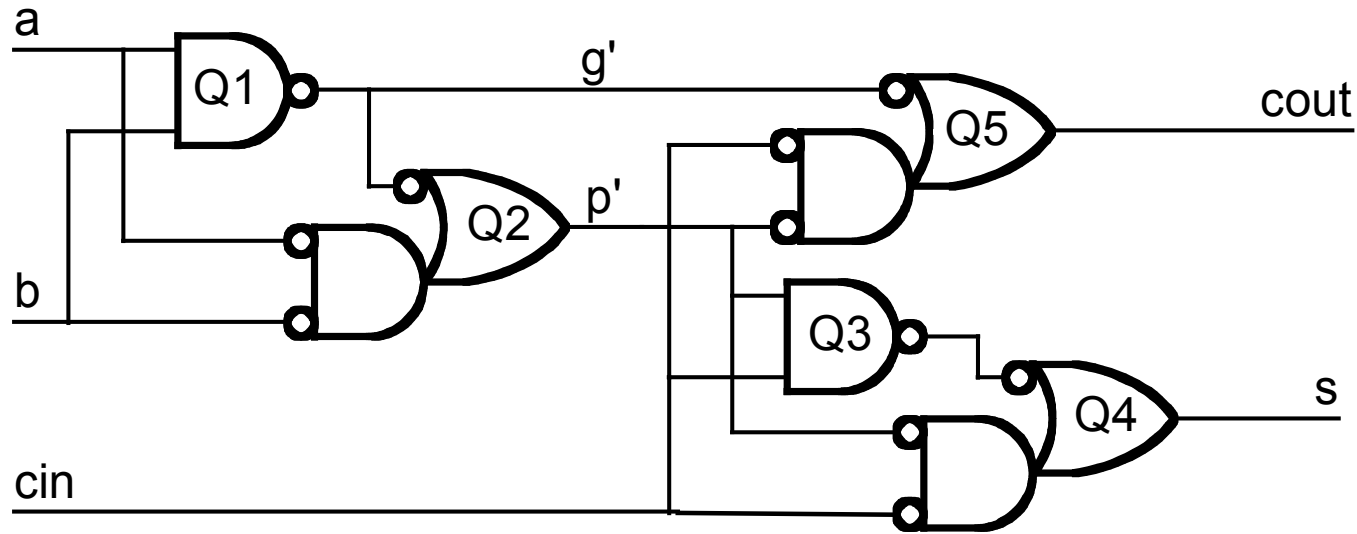
t_{das}

t_{cas}

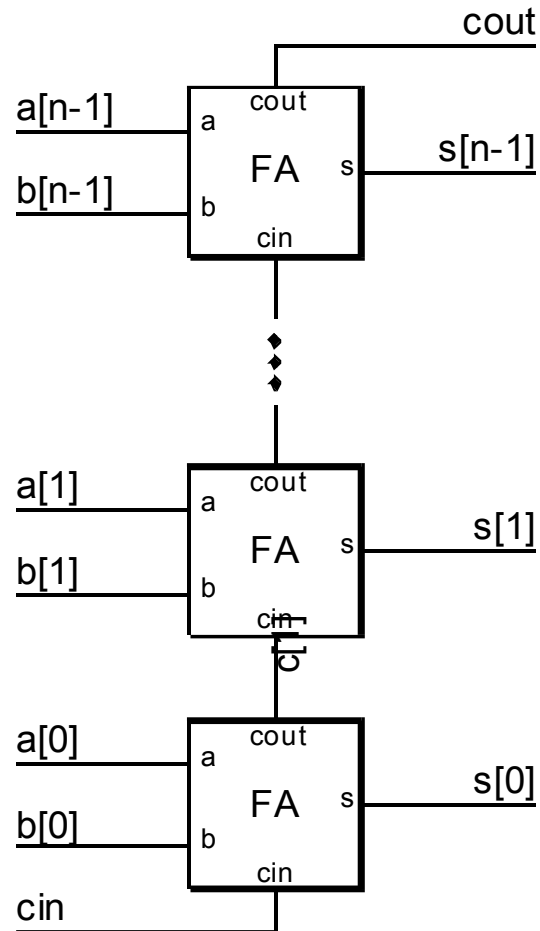
t_{dcs}

t_{ccc}

Note that if a, b goes from 0,0 to 1,1 contamination does occur



What about an n-bit adder?



Assume delay of FA is 1

What is

t_{das}

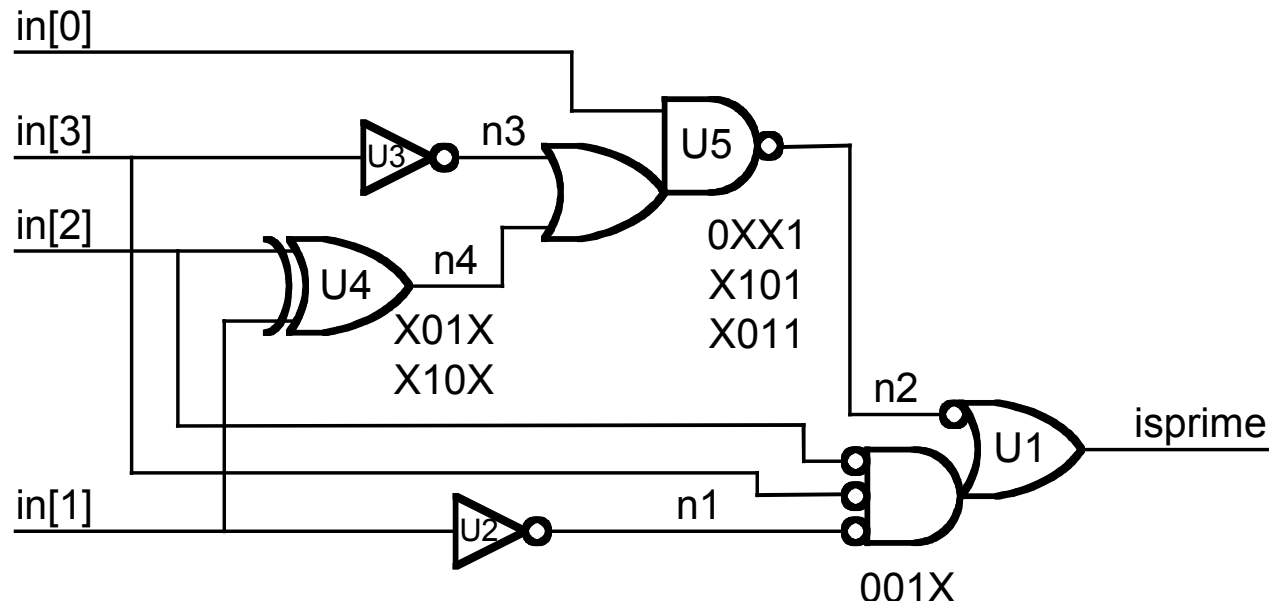
t_{cas}

t_{dcs}

t_{ccs}

4-bit Prime or one Function in Verilog Code – Result of synthesizing description using case

```
module prime ( in, isprime );  
input  [3:0] in;  
output isprime;  
    wire n1, n2, n3, n4;  
    OAI13 U1 ( .A1(n2), .B1(n1), .B2(in[2]), .B3(in[3]), .Y(isprime) );  
    INV U2 ( .A(in[1]), .Y(n1) );  
    INV U3 ( .A(in[3]), .Y(n3) );  
    XOR2 U4 ( .A(in[2]), .B(in[1]), .Y(n4) );  
    OAI12 U5 ( .A1(in[0]), .B1(n3), .B2(n4), .Y(n2) );  
endmodule
```



Synthesis Reports

Report : area
Design : prime
Version: 2003.06
Date : Sat Oct 4 11:38:08 2003

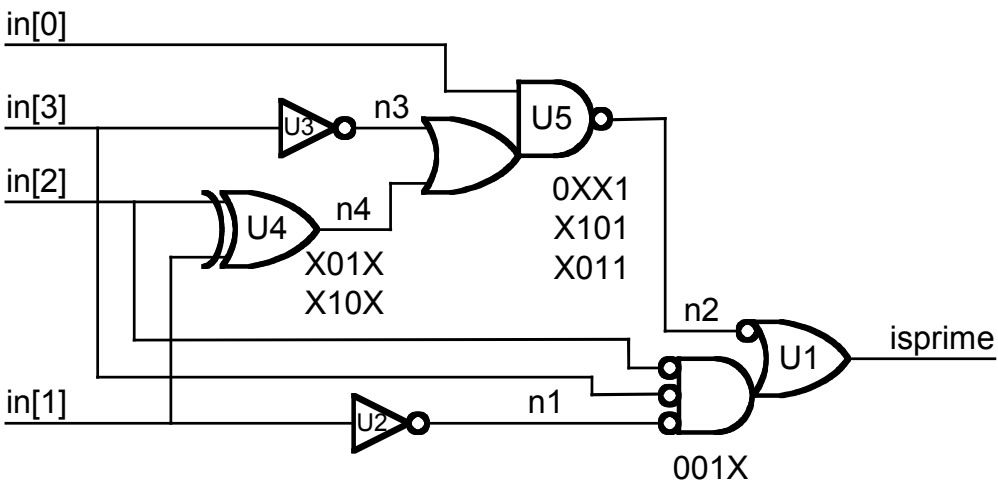
Library(s) Used:

GS30KA_W_125_1.35_CORE.db (File:
/home/imagine/from_ti/gs30ka_1.3/sun5/synop
sys/lib/GS30KA_W_125_1.35_CORE.db)

Number of ports: 5
Number of nets: 9
Number of cells: 5
Number of references: 4

Combinational area: 7.000000
Noncombinational area: 0.000000
Net Interconnect area: undefined (Wire load has zero net area)

Total cell area: 7.000000
Total area: undefined



Report : timing
-path full
-delay max
-max_paths 1
Design : prime
Version: 2003.06
Date : Sat Oct 4 11:38:08 2003

Operating Conditions:
Wire Load Model Mode: enclosed

Startpoint: in[2] (input port)
Endpoint: isprime (output port)
Path Group: (none)
Path Type: max

Des/Clust/Port	Wire Load Model	Library
prime	2K_5LM	
GS30KA_W_125_1.35_CORE.db		

Point	Incr	Path
-		
input external delay	0.000	0.000 r
in[2] (in)	0.000	0.000 r
U4/Y (EX210)	0.191	0.191 f
U5/Y (BF051)	0.116	0.307 r
U1/Y (BF052)	0.168	0.475 f
isprime (out)	0.000	0.475 f
data arrival time		0.475
-		
(Path is unconstrained)		

Timing report from Xilinx tools

Delay: 7.668ns (Levels of Logic = 20)
Source: wave_buffer_inst/Mram_RAM_inst_ramb_0 (RAM)
Destination: vga_blue_reg/q_1 (FF)
Source Clock: clk rising
Destination Clock: clk rising

Data Path: wave_buffer_inst/Mram_RAM_inst_ramb_0 to vga_blue_reg/q_1

Cell:in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)
RAMB16_S36_S36:CLKB->DOB0		4	1.500	0.629 wave_buffer_inst/Mram_RAM_inst_ramb_0 (data_read<0>)
LUT2_L:I0->LO	1	0.313	0.000	vga_driver_inst/XNor_stagelut (vga_driver_inst/N2)
MUXCY:S->O	1	0.377	0.000	vga_driver_inst/XNor_stagecy (vga_driver_inst/XNor_stage_cyo1)
MUXCY:CI->O	1	0.042	0.000	vga_driver_inst/XNor_stagecy_rn_0 (vga_driver_inst/XNor_stage_cyo1)
MUXCY:CI->O	1	0.042	0.000	vga_driver_inst/XNor_stagecy_rn_1 (vga_driver_inst/XNor_stage_cyo2)
MUXCY:CI->O	1	0.042	0.000	vga_driver_inst/XNor_stagecy_rn_2 (vga_driver_inst/XNor_stage_cyo3)
MUXCY:CI->O	1	0.042	0.000	vga_driver_inst/XNor_stagecy_rn_3 (vga_driver_inst/XNor_stage_cyo4)
MUXCY:CI->O	1	0.042	0.000	vga_driver_inst/XNor_stagecy_rn_4 (vga_driver_inst/XNor_stage_cyo5)
MUXCY:CI->O	1	0.042	0.000	vga_driver_inst/XNor_stagecy_rn_5 (vga_driver_inst/XNor_stage_cyo6)
MUXCY:CI->O	23	0.524	0.779	vga_driver_inst/XNor_stagecy_rn_6 (vga_driver_inst/XNor_stage_cyo7)
LUT3:I2->O	1	0.313	0.533	vga_driver_inst/_AUX_5<0>1 (vga_driver_inst/max_data<0>)
LUT2_L:I0->LO	1	0.313	0.000	vga_driver_inst/XNor_stagelut8 (vga_driver_inst/N11)
MUXCY:S->O	1	0.377	0.000	vga_driver_inst/XNor_stagecy_rn_7 (vga_driver_inst/XNor_stage_cyo8)
MUXCY:CI->O	1	0.041	0.000	vga_driver_inst/XNor_stagecy_rn_8 (vga_driver_inst/XNor_stage_cyo9)
MUXCY:CI->O	1	0.041	0.000	vga_driver_inst/XNor_stagecy_rn_9 (vga_driver_inst/XNor_stage_cyo10)
MUXCY:CI->O	1	0.041	0.000	vga_driver_inst/XNor_stagecy_rn_10 (vga_driver_inst/XNor_stage_cyo11)
MUXCY:CI->O	1	0.041	0.000	vga_driver_inst/XNor_stagecy_rn_11 (vga_driver_inst/XNor_stage_cyo12)
MUXCY:CI->O	1	0.041	0.000	vga_driver_inst/XNor_stagecy_rn_12 (vga_driver_inst/XNor_stage_cyo13)
MUXCY:CI->O	1	0.041	0.000	vga_driver_inst/XNor_stagecy_rn_13 (vga_driver_inst/XNor_stage_cyo14)
MUXCY:CI->O	1	0.525	0.440	vga_driver_inst/XNor_stagecy_rn_14 (vga_driver_inst/_n0002)
LUT4_D:I3->LO	1	0.313	0.000	vga_driver_inst/rgb_mux_select2 (N531)
FD:D		0.234		vga_blue_reg/q_1

Total 7.668ns (5.287ns logic, 2.381ns route)
(68.9% logic, 31.1% route)

And, from the .twr file

```
=====
Timing constraint: TS_J_TO_J = MAXDELAY FROM TIMEGRP "J_CLK" TO TIMEGRP "J_CLK" 30 ns;

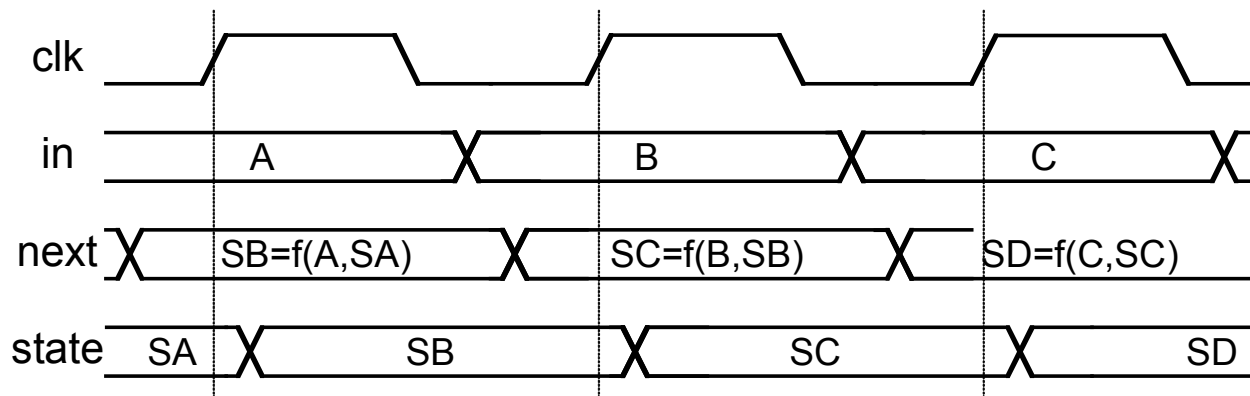
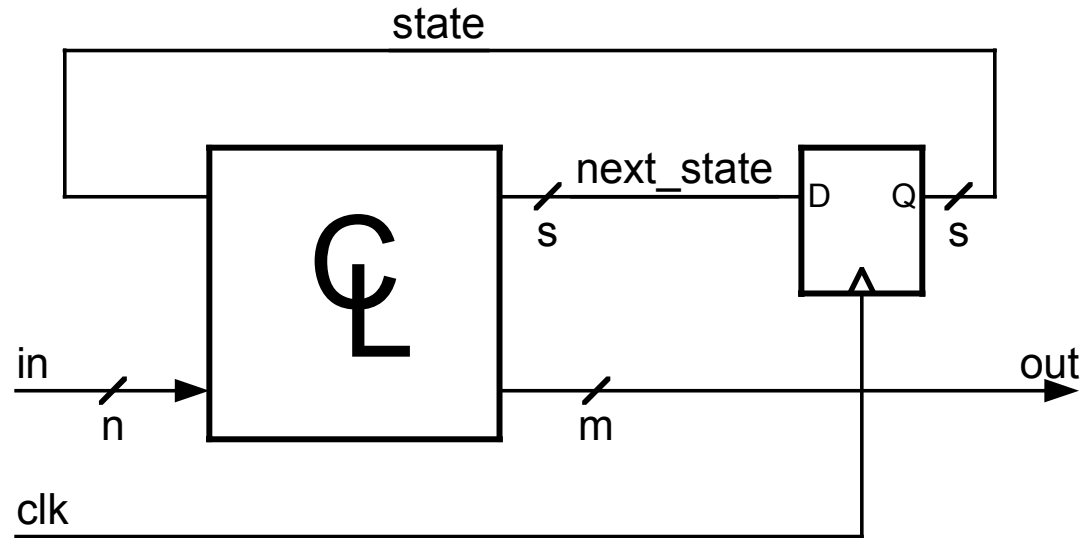
2782 items analyzed, 0 timing errors detected. (0 setup errors, 0 hold errors)
Maximum delay is 7.915ns.
-----
```

Contamination delay is not the same thing as *minimum delay*

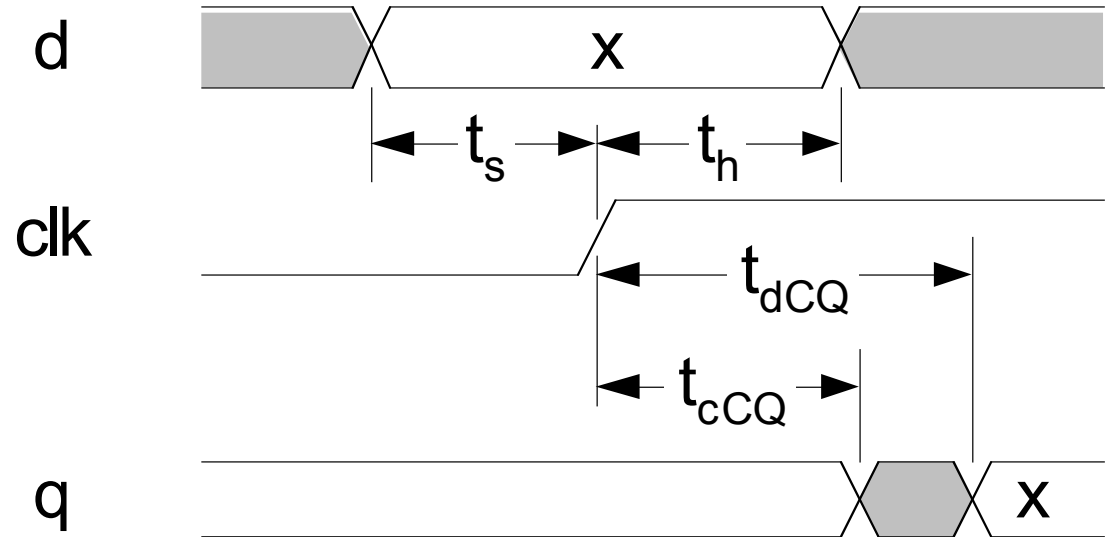
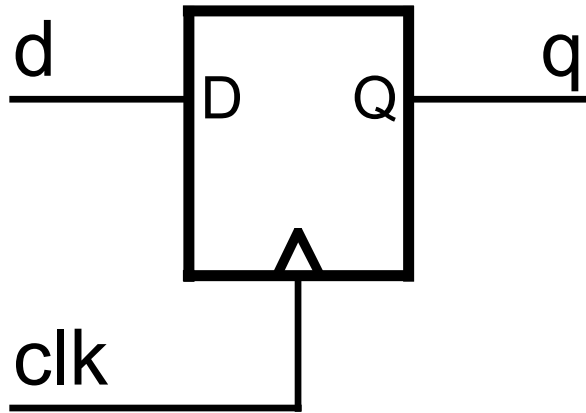
Contamination delay - is the minimum amount of time from an input signal change to an output signal **change**

Minimum delay - is the minimum amount of time from an input signal change (to its correct value) to an output signal taking on its **correct value**

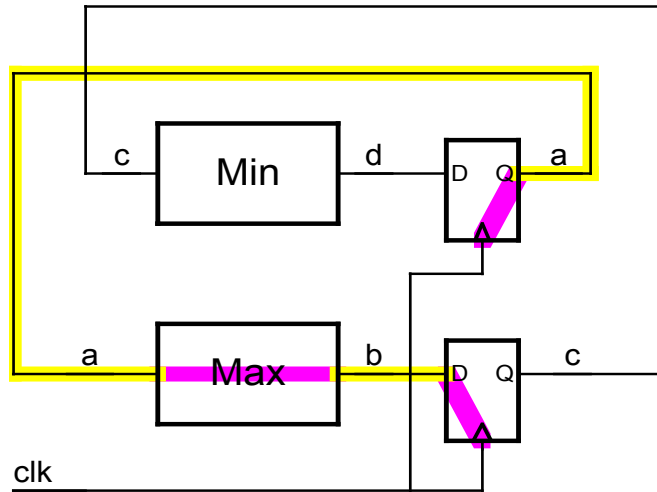
Synchronous Sequential Logic



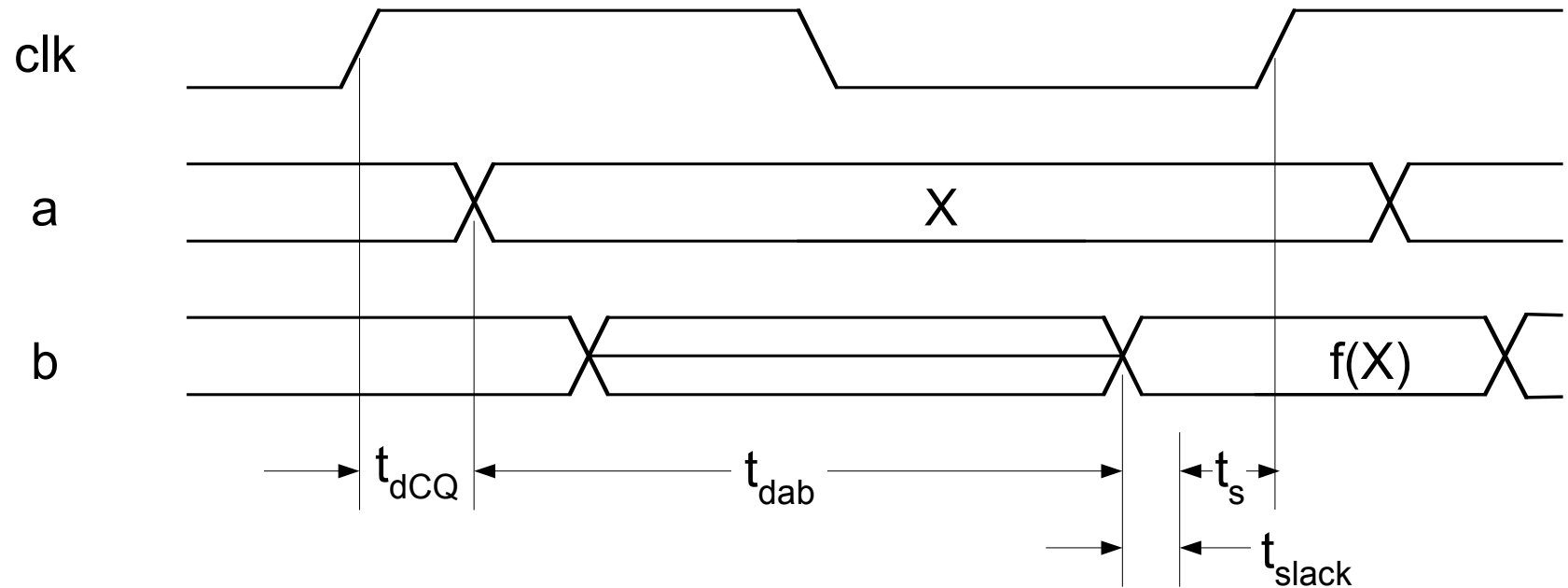
Edge-Triggered D Flip-Flop



Setup Time Constraint



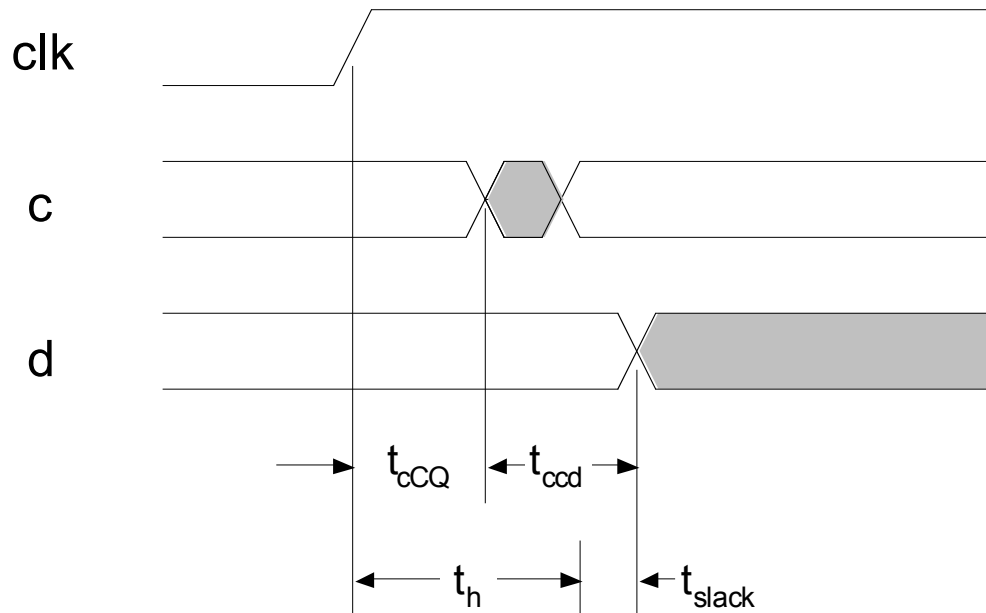
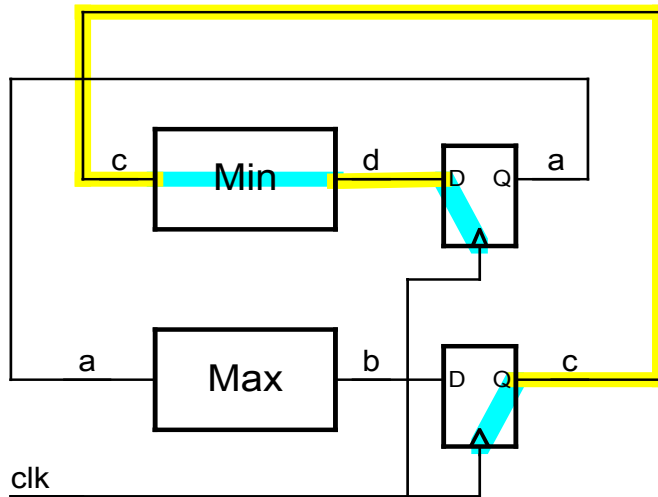
$$t_{cy} > t_{dCQ} + t_{dMax} + t_s$$



Hold Time Constraint

$$t_h < t_{cCQ} + t_{cMin}$$

Unsafe at any speed



t_{cXY} – contamination delay
 t_{dXY} – propagation delay

Example

$$t_{dcQ} = t_{ccQ} = t_s = 150\text{ps}$$

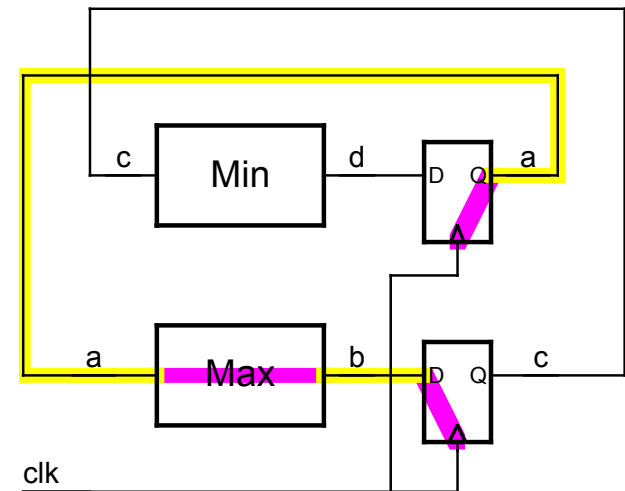
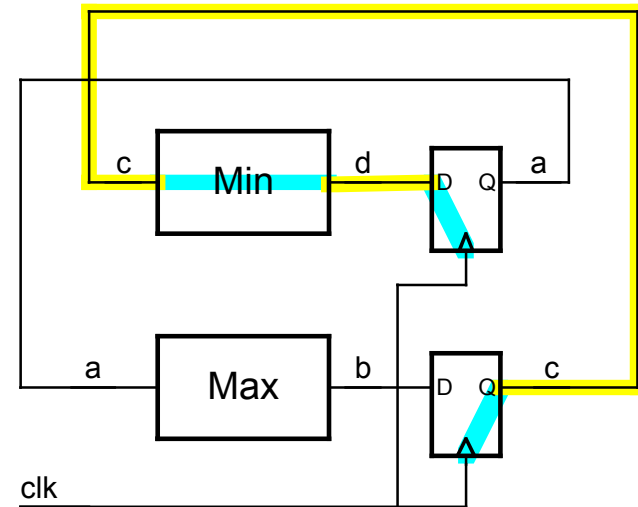
$$t_h = 250\text{ps}$$

$$t_{dMax} = 850\text{ps}$$

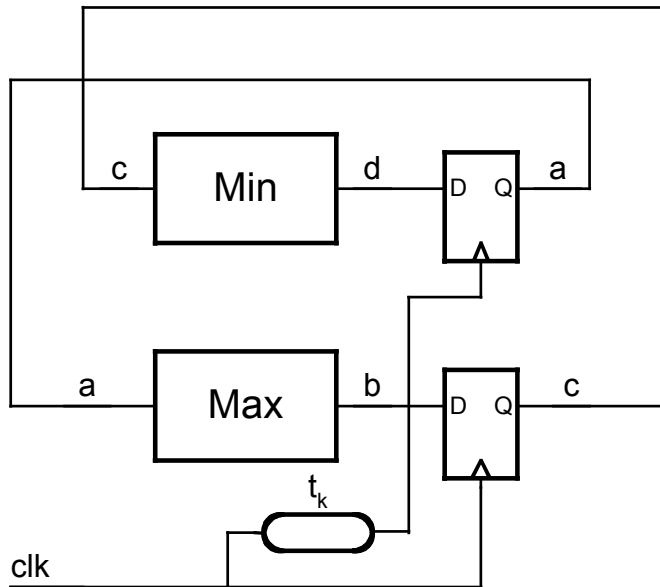
$$t_{cMin} = 100\text{ps}$$

Is hold time constraint met?

What is the minimum cycle time?

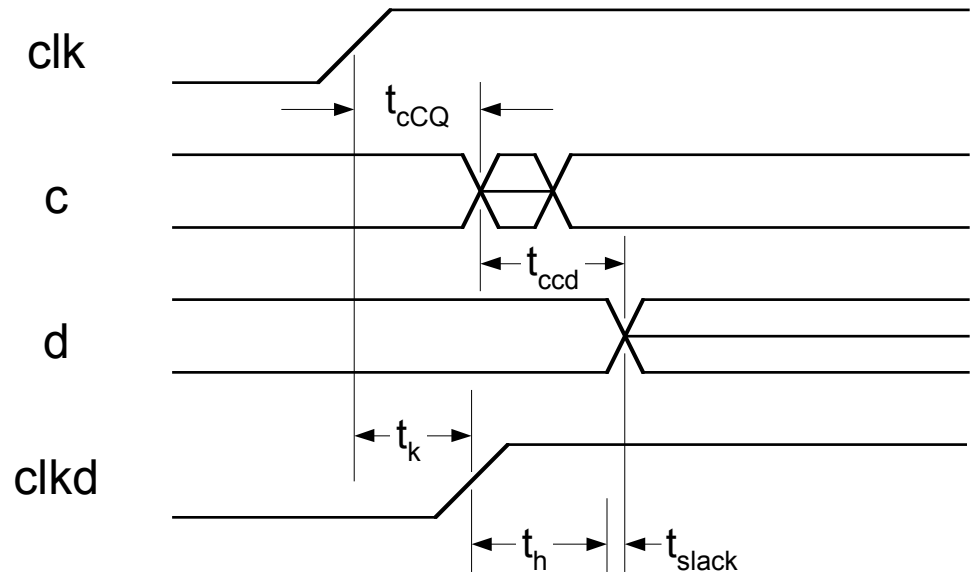


Clock Skew



$$t_{cy} > t_{dCQ} + t_{dMax} + t_s + t_k$$

$$t_h < t_{cCQ} + t_{cMin} - t_k$$



Example

$$t_{dCQ} = t_{cCQ} = t_s = 150\text{ps}$$

$$t_h = 250\text{ps}$$

$$t_{dMax} = 850\text{ps}$$

$$t_{cMin} = 100\text{ps}$$

$$t_k = 100\text{ps}$$

Is hold time constraint met?

What is the minimum cycle time?

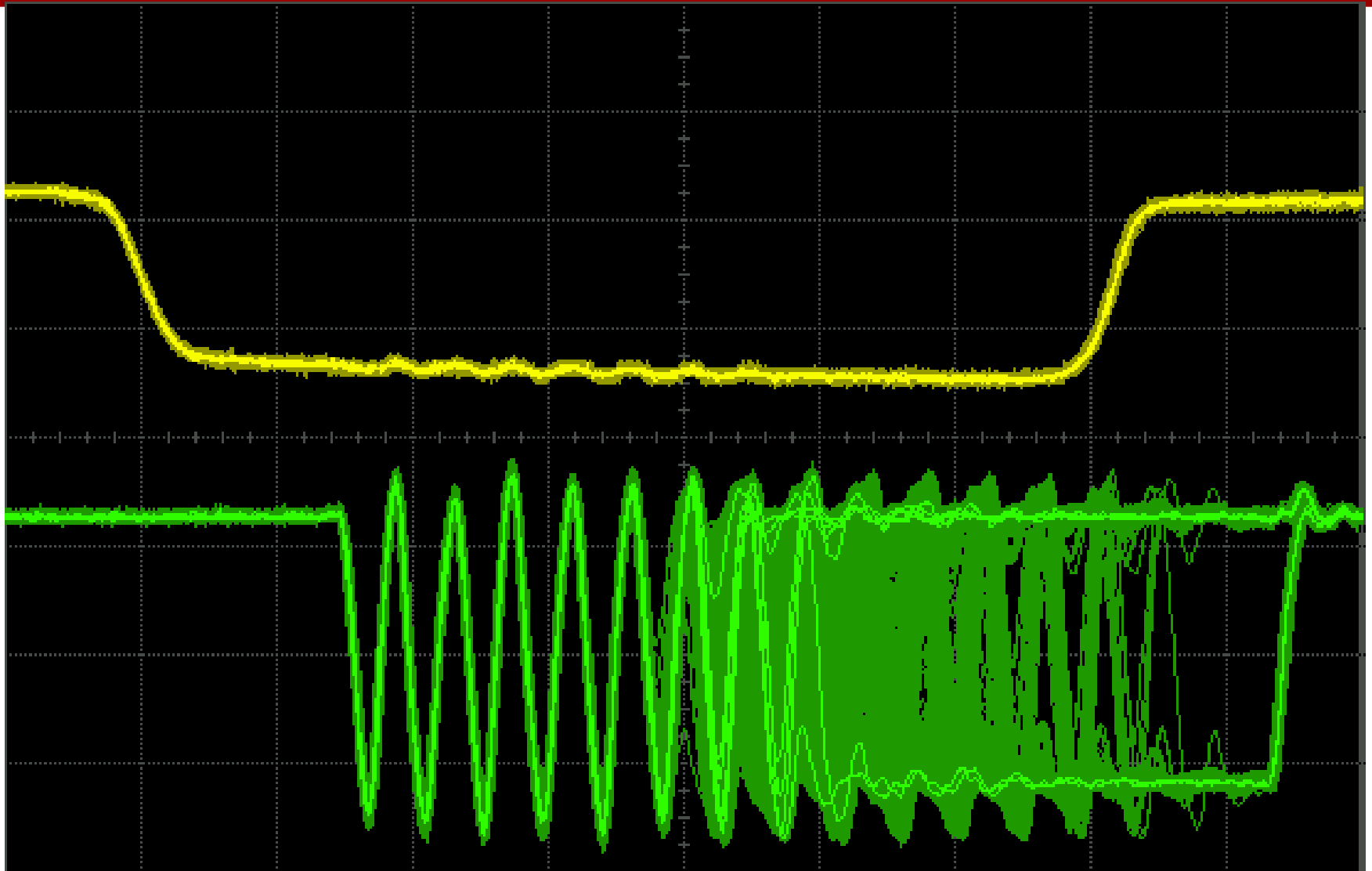
Another example

- You have three flip-flops connected as a shift register
- You need to connect the clock to these three flip flops
- Your connection must be from flip-flop to flip-flop (no intermediate points)
- Each segment of your connection takes $t_{dck}=200\text{ps}$
- Assume $t_s = t_h = t_{dcq} = t_{ccq} = 100\text{ps}$
- How should you connect the clock to these flip-flops (what order?)

Summary

- Delays in digital systems
 - Propagation delay
 - Contamination delay
- Flip-flop timing constraints
 - Setup time (t_s)
 - Hold time (t_h)
- Cycle time determined by maximum delay
$$t_{cy} > t_{dCQ} + t_{dMax} + t_s$$
- Correct operation depends on minimum delay
$$t_h < t_{cCQ} + t_{cMin}$$
- Clock skew affects both
$$t_{cy} > t_{dCQ} + t_{dMax} + t_s + t_k$$
$$t_h < t_{cCQ} + t_{cMin} - t_k$$

A Preview of coming attractions



Coming Next Lecture

- Metastability and synchronization failure
- or – When good flip-flops go bad