3.8.4 A Technique for Band Widening: Inductive Peaking

All resistance-loaded amplifiers can be considered as "wide-band amplifiers" by their nature. The low end of the band is determined by the coupling capacitors (if there are any), and the high end by the capacitance parallel to the load resistor. A wide-band amplifier is characterized with its gain that must be flat and equal to the low frequency gain with an acceptable tolerance up to the high end of the band, and the upper cut-off frequency where the gain drops to 3dB below the low frequency gain.

For a resistance-loaded common source amplifier[1], the 3 dB frequency, the low frequency gain and the gain-bandwidth product (the figure of merit for wide band amplifiers) were given previously as

$$\omega_p = \frac{G_o}{C_L} \; ; \; \frac{1}{C_L R_L} \quad \text{for } r_{ds} \; ? \; R_L \tag{3.4b}$$

$$A_v(0) = -\frac{g_m}{G_o} \; ; \; -g_m R_L \tag{3.5}$$

$$GBW = \frac{g_m}{2\pi C_L} \tag{3.6}$$

where R_L is the load resistance of the transistor and $C_L = C_o + C_L^{'}$ is the total capacitance of the output node, where C_o is the output capacitance of the transistor, mainly determined by the junction capacitance of the drain region, and $C_L^{'}$ the input capacitance of the succeeding stage (or the load). $C_L^{'}$ is usually given as one of the input parameters of the design problem. C_o can be initially neglected, or an estimated value depending on the technology can be given. (after the calculation of the dimensions of the transistor the correct value of C_o must be found and the design must be updated, if necessary).

To reach the targeted 3dB frequency that is equal to the pole frequency for a resistance loaded common source amplifier, the appropriate R_L value can be calculated from (3.4b) as

$$R_L = \frac{1}{2\pi f_p C_L} \tag{3.91}$$

To obtain the targeted gain, according to (3.5) the transconductance must be

$$g_m = \frac{|A_v(0)|}{R_L} \tag{3.92}$$

The transconductance of a transistor operating in the saturation region is determined by the DC drain current and the aspect ratio of the transistor.

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[1] The following investigations can be applied to other amplifier configurations with minor modifications (whenever necessary).

$$g_m = \sqrt{2\mu C_{ox} \frac{W}{L} I_D} \tag{1.33}$$

According to (1.33), any combination of *(W/L)* and I_D can be used to obtain the desired g_m value. Choosing lower drain current values will correspond to wider transistors, and therefore, to higher parasitic capacitance values, for the same g_m value. For higher drain current values, the parasitic capacitance can be decreased but the power consumption increases. Another concern related to the drain DC current (the quiescent current) is its position on the output characteristic curves. To obtain maximum dynamic range for the output voltage and minimum nonlinear (harmonic and intermodulation) distortion for a certain amplitude, the operating point must be placed at the center of the saturated operating region (as shown in Fig. 2.1), corresponding to

$$I_D = \frac{(V_{DD} - V_{DS(sat)})}{2R_L} \tag{3.93}$$

which can be considered as the optimum current for the majority of applications. Using this I_D, the aspect ratio of the transistor can be calculated from (1.33):

$$\frac{W}{L} = \frac{g_m^2}{2\mu C_{ox} I_D} \tag{3.94}$$

From (3.6) it is obvious that the factor limiting the bandwidth of an amplifier is C_L, i.e., the sum of the input capacitance of the load and the output parasitic capacitance of the transistor. The only chance to reduce the value of C_L and to increase the gain-bandwidth product is to reduce the width of the transistor that helps to reduce the parasitic junction capacitance of the drain region, at the expense of increasing the drain current and reducing the output signal dynamic range.

Another possibility to decrease the effect of the output capacitance is to compensate it with an inductance in the frequency region around the pole frequency. This technique, called as "inductive peaking", has been investigated and used from the early days of the electronic engineering[2] to present day[3]. The two basic approaches to compensate the load capacitance with an inductor are shown in Fig. 3.47.

The circuit shown in Fig. 3.47(a) is called "parallel (or shunt) compensation" and its small signal equivalent circuit is given in Fig. 3.47(b). In this approach, the output capacitance is resonated with an inductance (that increases the load impedance and hence the gain) in the vicinity of the 3 dB frequency of the basic amplifier, where the gain starts to decrease.

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[2] See: A. V. Bedford, G. L. Fredendall, "Transient Response of Multistage Video-frequency Amplifiers, Proc. IRE, Vol. 27, 1939, pp. 277-284, and Samuel Seely, "Electronic Engineering", McGraw-Hill, 1956, pp.101-110.

[3] See: Peter Staric, Eric Margan, "Wideband Amplifiers", Springer, 2007, and S. S. Mohan, M. del Mar Hershenson, S.P. Boyd, T.H. Lee, "Bandwidth Extension in CMOS with Optimized On-Chip Inductors", JSSC, Vol. 35, 2000, pp.346-355.

The circuit shown in Fig. 3.47(c) is called “series compensation” and its small signal equivalent circuit is given in Fig. 3.47(d). In this approach, the increase of the capacitance voltage at resonance with respect to the input voltage of the series resonance circuit is used to compensate the decrease of the output voltage (See Chapter 4, Section 4.1.2 for the details of main concepts).

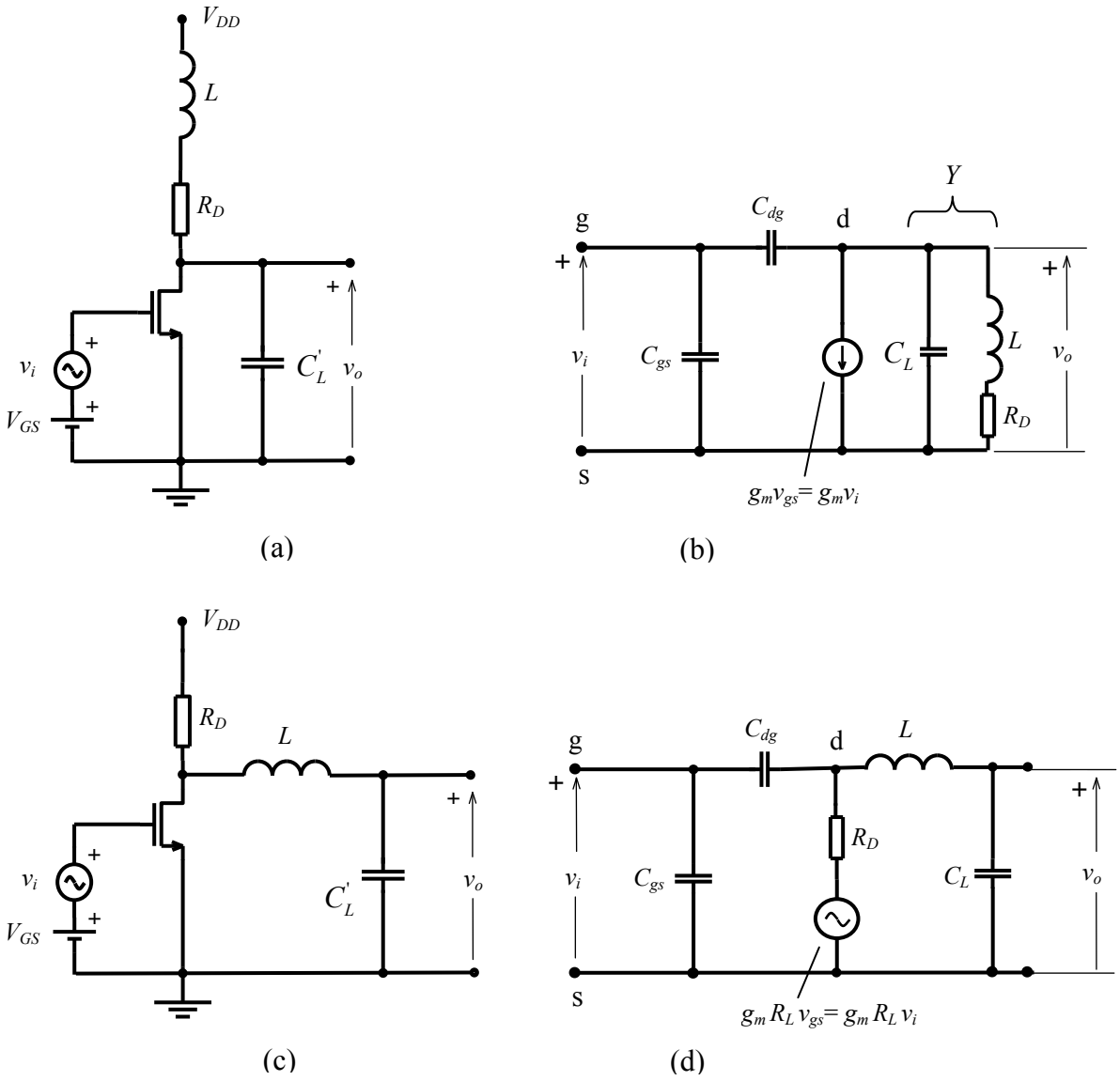


Figure 3.47 (a) Simplified circuit diagram of a inductively peaked resistive loaded common source amplifier. (b) The small signal equivalent circuit.

Let us first investigate the parallel compensated amplifier. From the equivalent circuit shown in Fig. 3.47(b), the voltage gain can be found as

$$A_v = \frac{v_o}{v_i} = -g_m \frac{R_D + sL}{s^2 LC_L + sC_L R_D + 1} \tag{3.95}$$

The gain in frequency domain, normalized with respect to the low frequency gain:

$$\overline{A} = \frac{|A_v(\omega)|}{|A_v(0)|} = \frac{1 + j\omega \dfrac{L}{R_D}}{(1 - \omega^2 LC_L) + j\omega C_L R_D} \tag{3.96}$$

Using the pole frequency of the basic (non-compensated) amplifier ($\omega_p = 1/R_D C_L$), the resonance frequency of the *LC* circuit ($\omega_o = 1/\sqrt{LC_L}$) and a parameter α that is defined as $\alpha = \omega_p / \omega_0$, (3.92) can be arranged in normalized form as

$$\overline{A} = \frac{1 + j(\omega/\omega_P)\alpha^2}{\left[1 - (\omega/\omega_P)^2 \alpha^2\right] + j(\omega/\omega_P)} \tag{3.97}$$

It must be noted that α can be written in terms of the circuit parameters and helps to calculate of the value of *L*, which is the most important design parameter:

$$\alpha = \frac{1}{R_D C_L}\sqrt{LC_L} \quad \rightarrow \quad L = \alpha^2 R_D^2 C_L \tag{3.98}$$

The variation of the normalized gain as a function of the normalized frequency for different values of α is given in Fig. 3.48. It can be seen from this graph that;

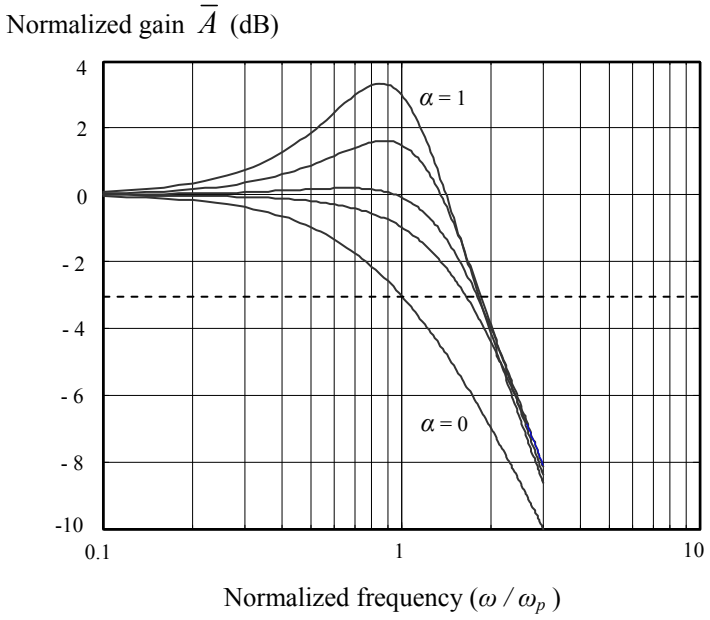


Figure 3.48 Variation of the normalized gain as a function of the normalized frequency for α = 0, 0.6, 0.7, 0.85 and 1.

- Increasing α (increasing L) effectively helps to increase of the bandwidth (and the gain-bandwidth product) of the amplifier. For α = 0.6 the bandwidth is 62% higher than that of a non-compensated amplifier. For higher values of α, the increase of the bandwidth approaches 87%.

- For α = 0.7, the frequency characteristic remains almost flat with a peaking of only 0.2 dB.

- For higher values of α, the bandwidth does not exhibit any further increase but the peaking becomes unacceptably high for many applications.

- Therefore, it can be concluded that the optimum value of α is 0.7.

But this conclusion has to be checked from the point of view of the delay characteristic of the amplifier.

Amplifiers are typically used to amplify complex waveforms, in most cases pulses and square waves. The flatness of the gain-versus-frequency characteristic guarantees the uniform amplification of all Fourier components associated with the waveform, up to the 3dB frequency. It must not be overlooked that to preserve the correct shape of the output waveform, the delay of all Fourier components must be same, in other words, the delay characteristic (not the phase characteristic) must also be flat.

The relation of the phase shift and the delay for a certain frequency is illustrated in Fig. 3.49. From this figure it can be seen that the delay (τ) corresponding to a certain phase shift φ is

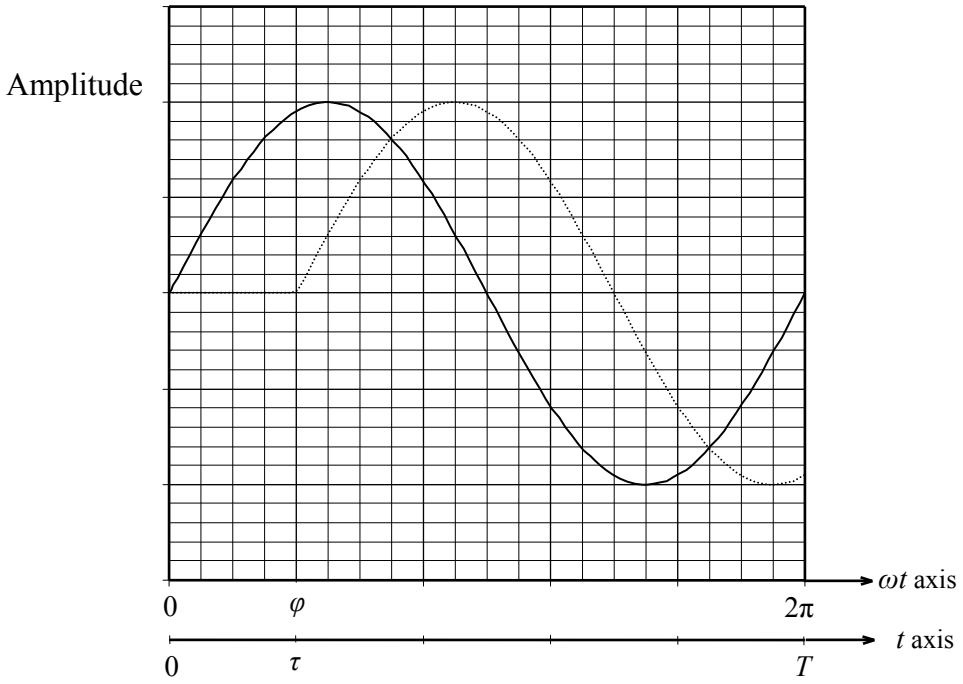


Figure 3.49 Relation of phase shift and time delay.

$$\tau = \varphi \frac{T}{2\pi} = \frac{\varphi}{2\pi f} = \frac{\varphi}{\omega} \tag{3.99}$$

The normalized delay characteristic obtained from the normalized phase characteristic is given in Fig. 3.50. From these curves it can be seen that:

- The delay characteristic corresponding to the flat magnitude characteristic (i.e. for $\alpha = 0.7$) is not flat.
- The flat delay characteristic corresponds to $\alpha = 0.6$.
- Therefore, for amplification of complex waveforms, despite 13% smaller bandwidth the appropriate value is $\alpha = 0.6$.

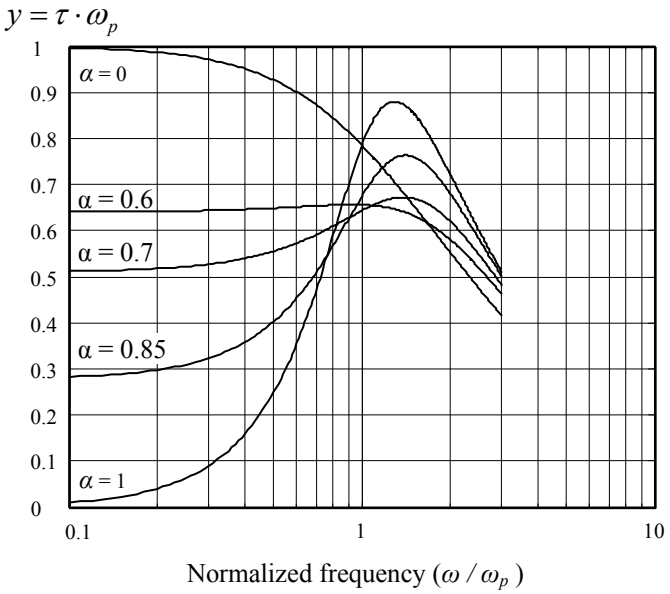


Figure 3.50 Variation of the normalized delay as a function of the normalized frequency for $\alpha = 0$, 0.6, 0.7, 0.85 and 1.

To illustrate the effect of the phase delay, the PSpice step response simulation results for an amplifier for various values of α (corresponding to various values of L) are given in Fig. 3.51, underlining the importance of the delay characteristic for a wide band amplifier.

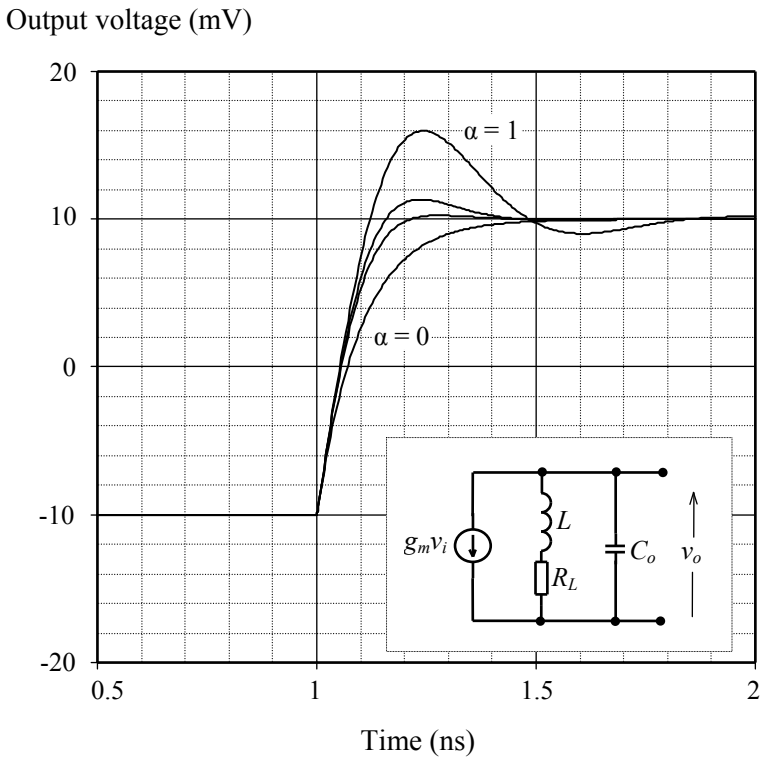


Figure 3.51 The step response of **a** wide-band amplifier model for +1 mV to -1 mV input step voltage. The parameters of the amplifier model are g_m = 10 mS, R_L = 1k ohm and C_o = 100 fF. The responses correspond to α = 0 (L = 0), α = 0.6 (L = 36 nH), α = 0.7 (L = 49 nH) and α = 1 (L = 100 nH).

Example 3.4 Design of a 3GHz bandwidth and 14 dB voltage gain, parallel inductive peaked wide band amplifier.

Technology: AMS035
Supply voltage: V_{DD} = + 3V
Load capacitance: $C_L^{'}$ = 75 fF
Frequency response: Minimum delay distortion
Signal source internal resistance: R_s = 50 ohm

Since the 3 dB frequency of an amplifier having minimum delay distortion (flat delay characteristic) is 62 % wider than that of a non peaked amplifier, the starting point must be a resistance loaded amplifier having 14 dB (A_v = 5) voltage gain and f_p = 3 GHz/1.62 = 1.85 GHz bandwidth.

The load capacitance is given as 75 fF. The other component of the total parallel output capacitance, the output capacitance of the transistor that depends on the dimensions has to be guessed in the beginning and must be checked later on, and updated if necessary. Let us assume the output capacitance of the transistor is also 75 fF, then the total parallel capacitance is C_L = 150 fF.

(3.91) gives the value of the collector load resistance:

$$R_L = \frac{1}{2\pi f_p C_L} = \frac{1}{2\pi \times (1.85\times 10^9) \times (150\times 10^{-12})} = 573.5 \text{ ohm}$$

The value of the transconductance to obtain the targeted gain with this load resistance can be calculated from (3.92):

$$g_m = \frac{5}{573.5} = 8.7 \text{ mS}$$

To obtain maximum output voltage dynamic range, the drain quiescent current, according to (3.93), must be

$$I_D \cong \frac{(3-0.5)}{2\times 573.5} = 2.18 \text{ mA}$$

The aspect ratio of the transistor can be calculated from (3.94):

$$\frac{W}{L} = \frac{(8.7\times 10^{-3})^2}{2\times 300\times (4.54\times 10^{-7})\times (2.18\times 10^{-3})} = 127.46 \quad \rightarrow \quad W \cong 45 \ \mu\text{m}$$

Finally, the value of the peaking inductance for a flat phase delay characteristic from (3.98):

$$L = (0.6)^2 \times (573.5)^2 \times (150\times 10^{-15}) = 17.76 \text{ nH}$$

and for comparison purpose, the value of the peaking inductance for a flat gain characteristic;

$$L = (0.7)^2 \times (573.5)^2 \times (150\times 10^{-15}) = 24.17 \text{ nH}$$

The PSpice simulations:

With the calculated values the circuit diagram of the amplifier is given in Fig. 3.52. To obtain the calculated I_D value, a DC sweep must be applied to V_G, the gate bias voltage. The AC simulation with the calculated circuit parameters and the found gate bias voltage shows that the voltage gain is $|A_v(0)| \cong 3$, considerably smaller than the targeted value. This is due to the smaller value of the simulated transconductance as explained in Chapter 1 and in principle can be compensated by increasing the aspect ratio and/or the DC drain current. But the maximum output voltage dynamic range forces us to keep the calculated I_D value. Therefore, to fine tune the gain to 5, the aspect ratio and the bias voltage must be adjusted. The obtained results are W = 84 μm and V_G = 0.95V (which is in agreement with the pre-estimated $V_{DS(sat)}$ = 0.5 V).

The PSpice netlist is given below, covering the DC sweep, AC gain and delay characteristics, the transient response for a pulse input voltage to check and compare the delay distortion, and the transient response for a 1 GHz sinusoidal input voltage to check the output dynamic range (the L values correspond to the fine-tuned amplitude and delay characteristics):

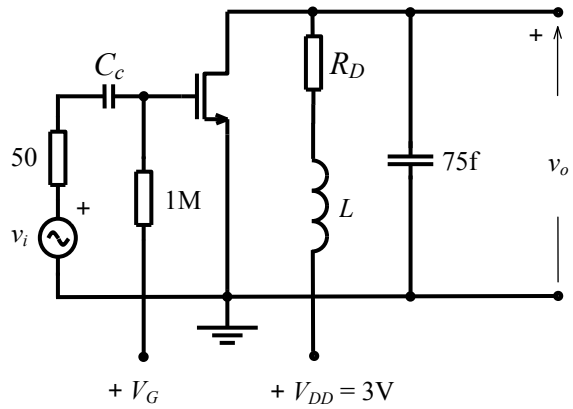


Figure 3.52 Schematic diagram of the amplifier.

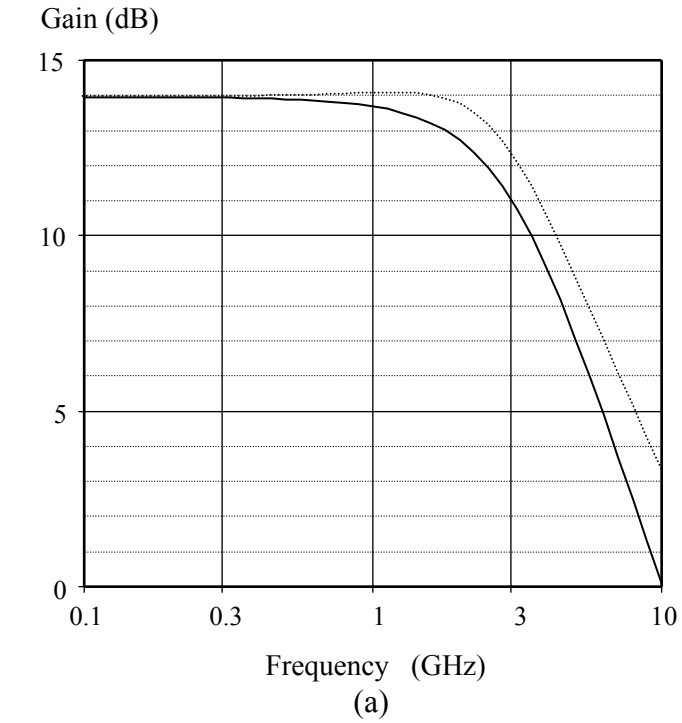
```
      *CS INDUCTIVE SHUNT PEAKED AMPLIFIER*

.LIB "ams035.lib"
VDD  100  0  3
M1  1 2 0 0 modn L=.35U  W=84U ad=70e-12 as=70e-12 Pd=84u Ps=84u
CL' 1 0 75f
RL 11 1 573.5
L 100 11 16.6n
*L 100 11 24n
RG 2 200  100k
VG 200 0 .95

vin  23 0 ac 10m
*vin 23 0 pulse 10m -10m .5n 1p 1p 1n 2n
*vin 23 0 sin (0 200mV 1G)
Rs 23 22 50
cc 22 2 100p

.DC VGG .5  2  10M
.AC DEC 20 .1G 10G
*.TRAN .1n 2.5n 0 5p
.PROBE
.END
```

Simulation results for frequency characteristics of the gain and the signal delay are shown in Fig.3.53 (a) and (b). The pulse response corresponding to the flat gain characteristic and the flat delay characteristic are shown in Fig.3.54. The simulation performed to check the position of the operating point, is shown in Fig.3.55.



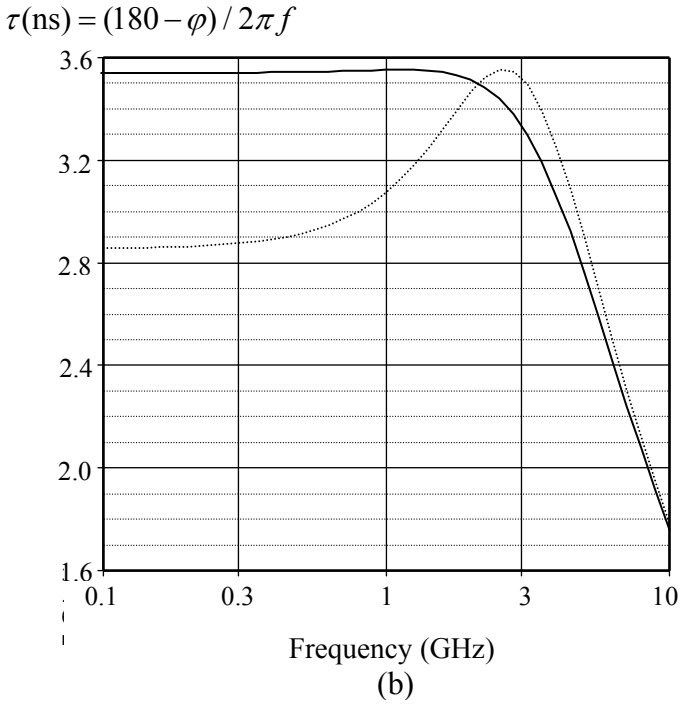


Figure 3.53 PSpice simulation results for (a) the gain characteristics, (b) the delay characteristics. The solid lines correspond to flat delay characteristic (L = 16.6 nH) and the dotted lines to the flat gain characteristic (L = 24 nH).

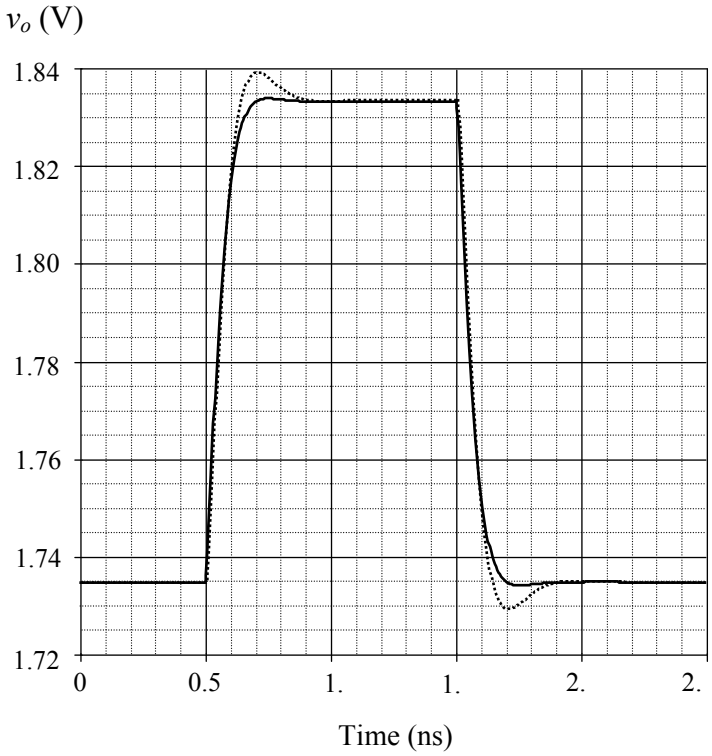


Figure 3.54 The pulse response of the amplifier. The solid line corresponds to the flat delay characteristic (L = 16.6 nH) and the dotted line to L = 24 nH.

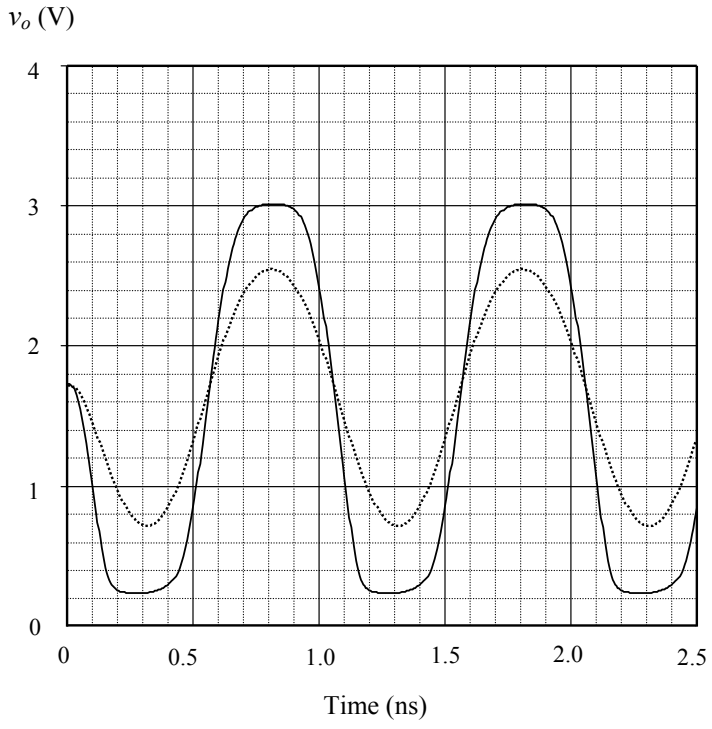


Figure 3.55 The output voltage of the amplifier at 1 GHz input frequency. The solid line corresponds to 500 mV input voltage amplitude and the dotted line to 200 mV amplitude.

These simulation results can be interpreted as follows:

- The delay characteristic corresponding to L = 16.6 nH shown in Fig.3.53(b) (the solid line) is flat up to 2GHz within 1.4% and up to 3 GHz within 5.8% [4]. The fine tuning of the inductance value (from the calculated 17.76 nH to 16.6 nH) indicates that the assumed value of the output parasitic capacitance of the transistor was somewhat higher than the assumed value. But the difference is small and therefore, iterative re-design is not considered to be necessary.

- The 3 dB frequency of the gain characteristic corresponding to minimum delay distortion (Fig.3.53(a), the solid line) fulfills the 3GHz bandwidth requirement.

- The 3 dB frequency corresponding to the flat gain characteristic is even higher than expected (3.38 GHz), at the expense of excessive signal delay at high frequencies, affecting the transient response.

- The transient responses corresponding to the flat delay characteristic and to the flat gain characteristic are given in Fig.3.54. The response corresponding to the flat delay characteristic settles to the final value without overshoot, with a rise time of 110.2 ps. The response corresponding to the flat gain characteristic has 5% overshoot, which can be tolerated for many applications. The rise time for this case is 94.8 ps, which may make it preferable.

- Since the inductance values are high, the quality factors for on-chip realization will be considerably low and series resistances high. For example, the series resistance of a L =16.6 nH, Q = 5 inductance at 1.85 GHz is 38.6 ohm (See Chapter 4, Section 4.1.1.1). Therefore, the value of R_L must be reduced to 535 ohm.

- In Fig. 3.55 the responses to 1 GHz, 500 mV amplitude and 200 mV amplitude sinusoidal input signals are shown. The symmetrical clipping of the output waveform corresponding to 500 mV input signal indicates that the position of the operating point on the output characteristic curves (the value of the drain quiescent current) is appropriate for small nonlinear distortion.

- If the power consumption has prime importance, a drain quiescent current smaller than the value given with (3.93) can be used, at the expense of reducing the output voltage dynamic range and increasing the output capacitance due to the increase of W.

- For higher signal source resistance values, it may be necessary to take into account the effect of the R_sC_{gs} low-pass section.

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[4] Note that to eliminate the 180º basic phase shift of the amplifier, the signal delay is calculated as $(180 - \varphi) / (2\pi f)$.

- The lower 3 dB frequency of the amplifier with C_c = 10 pF and R_G = 100 kohm is 160 kHz, which may be unnecessarily low for many applications. To increase the value of the lower 3 dB frequency a solution is reduce the value of C_c. But it must not be overlooked that C_c and C_{gs} form a capacitive, frequency independent voltage divider and reduce the signal reaching the gate of the transistor, and consequently, the voltage gain decreases in the whole band.

A final remark: After the layout and the post lay-out simulations, it may be necessary to perform a second fine-tuning, due to the layout related parasitics.

Problem 3.4

Derive the expressions for the series-peaked wide band amplifier shown in Fig. 3.47(c)

Problem 3.5

(a) Design a series-peaked amplifier fulfilling the requirements given in Example 3.4.

(b) Compare the results corresponding to the parallel and the series compensated amplifiers, and discuss.
