Problems for Chapter 21 of 'Ultra Low Power Bioelectronics'

Problem 21.1

Derive Equation (21.2). Also show that if the transistors are sized according to Equation (21.2), their off currents will be equalized if $\kappa_n = \kappa_p = \kappa$.

Problem 21.2

Use the circuit model for car power consumption shown in Figure 26.5 to map braking energy losses to switching energy losses in electrical circuits, and rolling-friction and drag-energy losses to static energy losses in electrical circuits.

a) From this mapping show why metrics for transportation energy efficiency are similar to those for circuit design, i.e., prove Equations (26.17) and (26.18).
b) How does the curve of car power consumption versus car speed in Figure 26.6 differ from one of a digital circuits' curve of power consumption versus clock frequency?

Problem 21.3

Using MATLAB or another computational program, show that optimal energy consumption in Equation (21.30) occurs for the expressions described in Equation (21.31).

Problem 21.4

Consider a CMOS inverter designed in a 0.1 μm process with V_{DD} smaller than the threshold voltages of both the NMOS and the PMOS transistors. Assume that $\kappa_n = \kappa_p = \kappa = 0.6$ and that $V_{THN} = 0.35$ and $V_{THP} = -0.4$. The threshold-voltage variation is approximately 3.2 mV for a 1 μm geometric mean of width and length; for other lengths and widths, it scales as given by Equation (6.53).

a) Determine the relative sizing of the PMOS and the NMOS transistors, $\frac{W_p / L_p}{W_n / L_n}$, such that the trip point of the inverter is at $V_{DD} / 2$.
b) Based on the relative sizing in part a), estimate the actual size of each transistor that will achieve robust operation at $V_{DD} = 200$ mV. State any assumptions that you make.

Problem 21.5

Figure P21.5 shows a schematic of a CMOS logic gate.

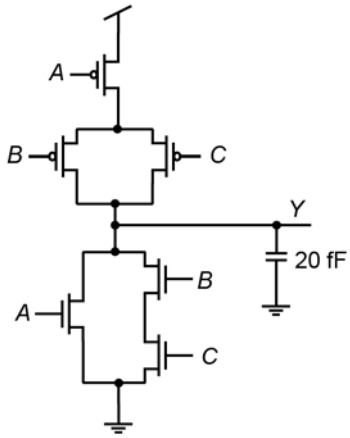

Figure P21.5: A static logic gate for Problem 21.5.

a) What is the logic function implemented by this circuit?
b) Suppose the statistics of A, B and C are uncorrelated with $P(A=1) = 0.2$, $P(B=1) = 0.3$ and $P(C=1) = 0.4$. Estimate the average dynamic power of this logic gate for $V_{DD} = 500$ mV and the input frequency of 500 kHz. Assume that all the intrinsic capacitances of the gate are negligible compared to the 20 fF output capacitance.
c) Draw a schematic for this logic gate if it is implemented in a dynamic-logic style.
d) Calculate the average dynamic power of the dynamic-logic version given the same conditions as in part b). Discuss why the gate of Figure P21.5 or your dynamic-logic version of the same gate consumes less/more power.

Problem 21.6

This problem requires the use of a circuit simulator such as SPICE. Simulate and plot the static power dissipation of the inverters in Figures P21.6 (a) and P21.6 (b) as a function of V_{DD}. Sweep V_{DD} from $V_{DD} = 0.2$ V to $V_{DD} = 1.8$ V. Use a 0.18 μm CMOS model for simulation. Comment on the discrepancies between the results of the two simulations. What causes the difference in static power consumption between the two inverters?

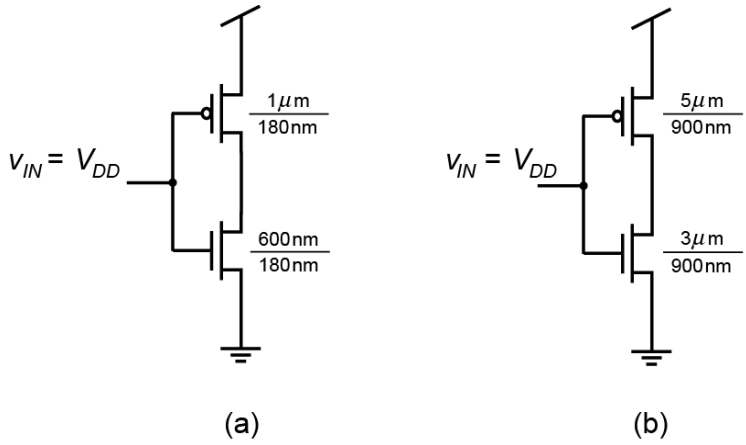

Figure P21.6: CMOS inverters

Problem 21.7

Consider a CMOS inverter designed in a CMOS process whose minimum length is 0.6 μm. Use the following parameters for this problem: $\kappa_n = \kappa_p = 0.7$, $V_{Tn} = 0.7$, $|V_{Tp}| = 0.9$, $\mu_n C_{ox} = 80\ \mu A/V^2$, $\mu_p C_{ox} = 40\ \mu A/V^2$, and $\phi_t = 26$ mV. The NMOS is sized with $W_n / L_n = 3\ \mu m / 0.6\ \mu m$. Assume that the supply voltage for the inverter is $V_{DD} = 0.5$ V.

a) Calculate the aspect ratio of the PMOS transistor such that the trip point of the inverter is at $V_{DD}/2$. How would you size the PMOS transistor to minimize the load capacitance?
b) Assume that the inverter is driving a 50 fF load capacitance and that the intrinsic capacitance is negligible compared to the load capacitance. Calculate the propagation delay of the inverter for the low-to-high output transition t_{pLH} with the sizing of part a).
c) Calculate the propagation delay of the inverter for the high-to-low output transition, t_{pHL} with the sizing of part a).
d) What is the average propagation delay of this inverter?

Problem 21.8

Suppose the inverter in Problem 21.7 is used to form a five-stage ring oscillator. The output of each stage is dominated by a 50 fF load capacitance as shown in Figure P21.8.

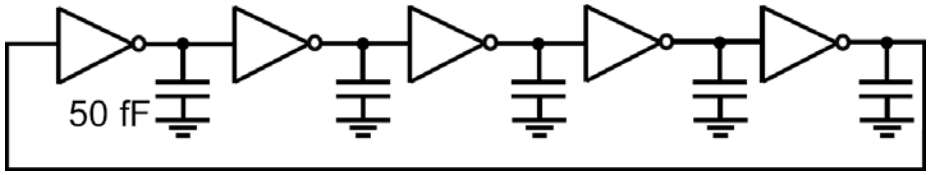

Figure P21.8: A five-state ring oscillator circuit.

a) Calculate the period of oscillator as a function of V_{DD} for subthreshold operation.

b) At V_{DD} = 0.5 V, calculate the dynamic power consumption of this ring oscillator.
c) Estimate the short-circuit power consumption for V_{DD} = 0.5 V. What is the ratio of short-circuit power consumption to dynamic power consumption in this ring oscillator?

Problem 21.9

Suppose we want to charge the capacitance *C* in the *RC* circuit of Figure 21.7 (a) from 0 to V_{DD} in a fixed time *T* with a constant current source (instead of with v_{IN}).

a) Calculate the energy dissipated in the resistor as a function of *T*.
b) If the current-source approximation is actually valid for v_{IN} that slowly changes from *0* to V_{DD} in a linear ramp-like fashion, what are the constraints on the rise time of the ramp?
c) By exploiting the properties of Fourier transforms, show how your time-domain analysis with a ramp in part b) is consistent with the frequency-domain viewpoint of Equation (21.50).

Problem 21.10

This problem requires the use of a circuit simulator such as SPICE. In this problem, we will explore the dependence of leakage current on the inputs to a gate via SPICE simulations. Consider the CMOS NAND gate shown in Figure P21.10.

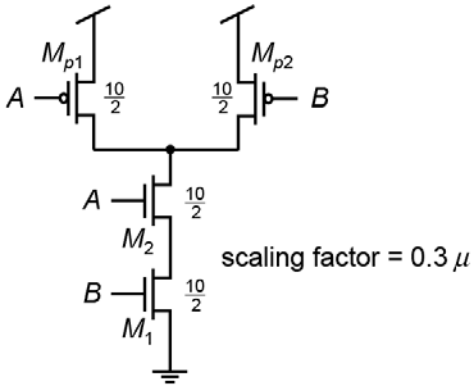

Figure P21.10: A CMOS NAND gate.

a) Using a model from a 0.6 μm CMOS process, simulate and find the leakage current of this NAND gate for all of its four input combinations.
b) Which input combination results in the highest leakage current? Which transistor(s) determine the leakage current for this input combination? Explain.
c) Which input combination results in the lowest leakage current? Which transistor(s) determine the leakage current for this input combination? Explain.