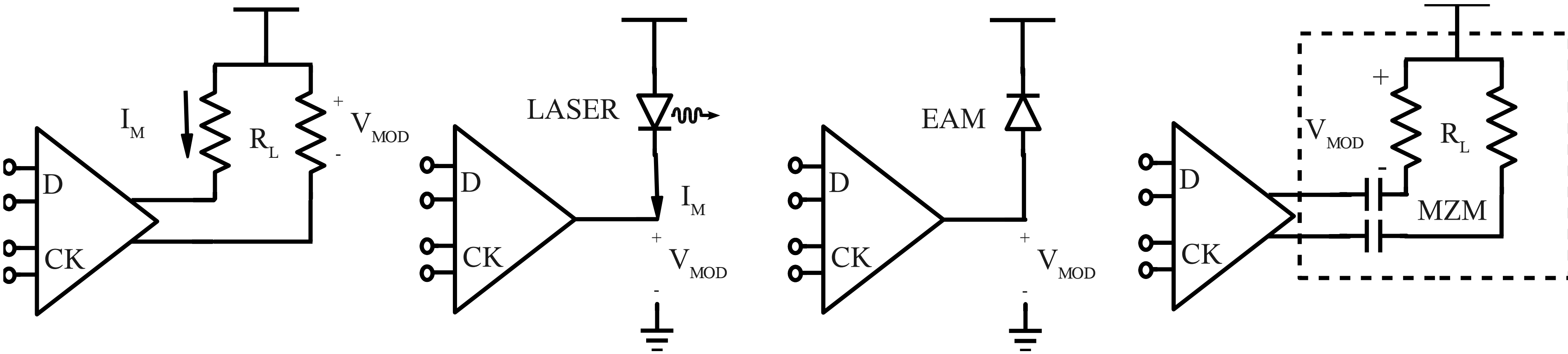
Broadband Drivers with Wave Shape Control for Optical Fiber and Backplane Applications

Recommended reading:
1) Chapters 7 and 8, Sackinger

Outline

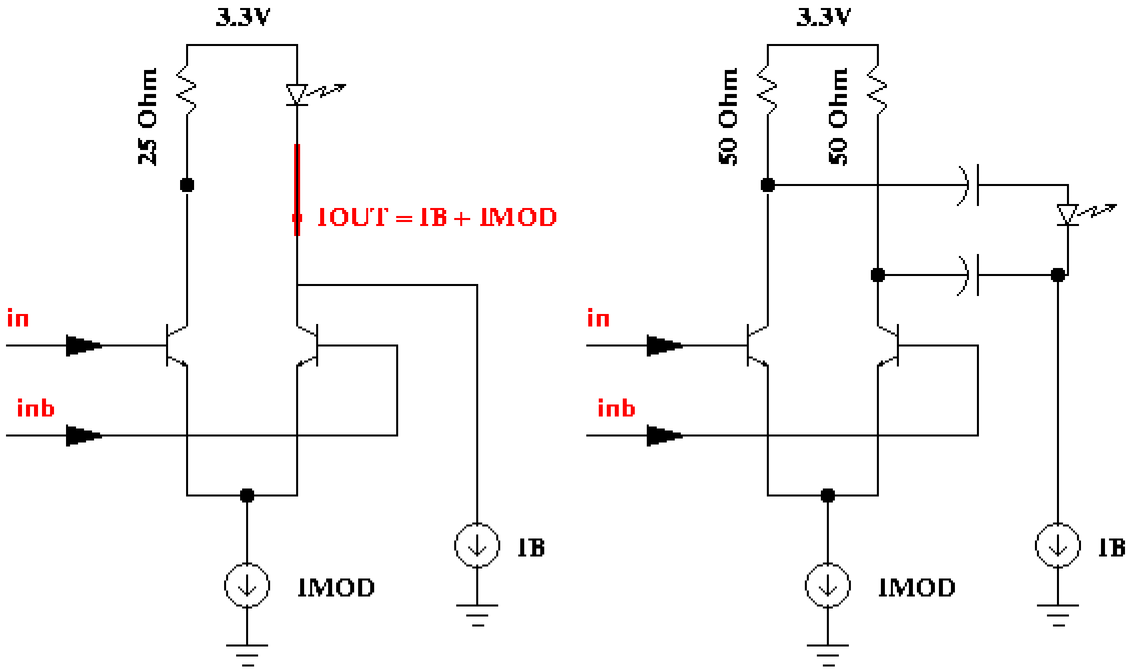
- Types of drivers
- Driver specification
- Driver building blocks and architecture
- Driver implementation and design examples

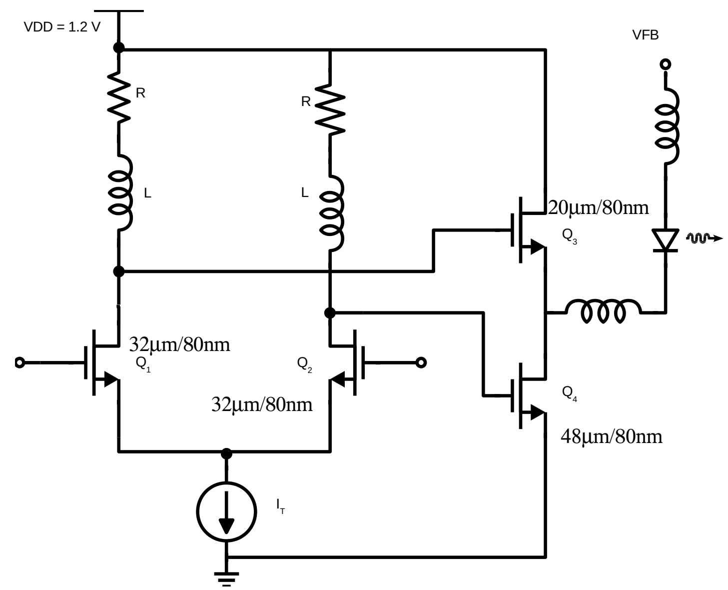
Types of drivers: backplane, cable



- I/O (R_L=50 Ω) backplane driver
- Coaxial cable (HDTV) (R_L=75 Ω)
- Laser driver
- EAM (Electro-Absorption Modulator) driver
- MZM (Mach-Zehnder Modulator) driver

Types of drivers: DFB/FB Laser, VCSEL

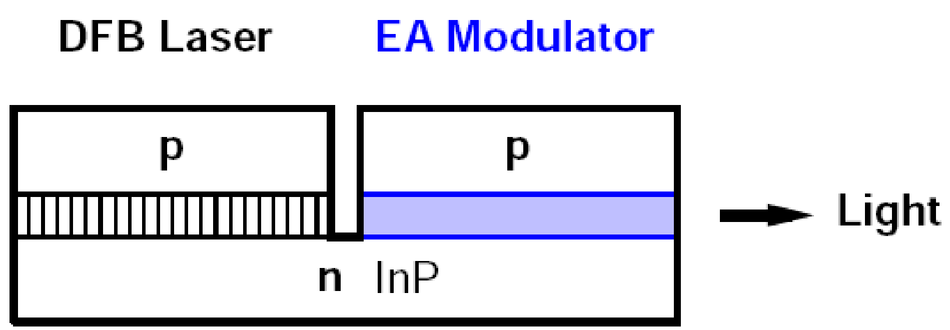




C. Kromer et al ISSCC 2005

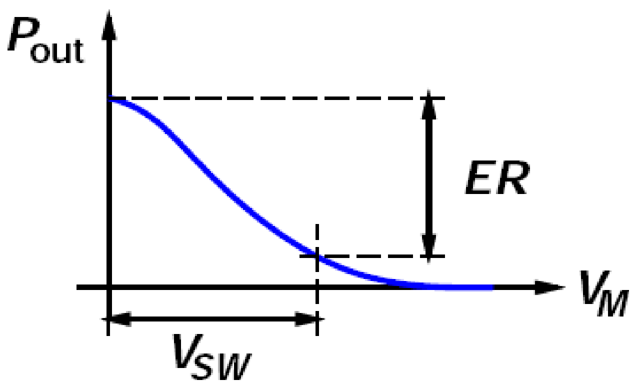
- Laser driver (R_L=5..25 Ω, C_L=0.2 .. 0.3 pF)

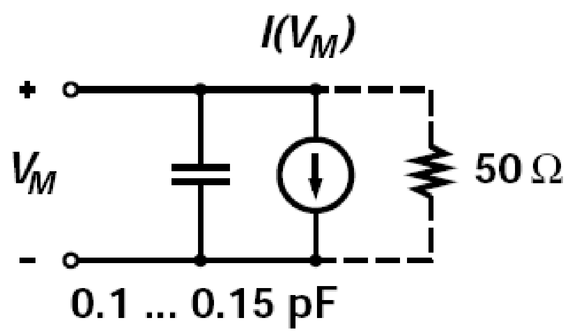
EAML = EA Modulator + Laser



[2]

Switching curve and electrical equivalent circuit:



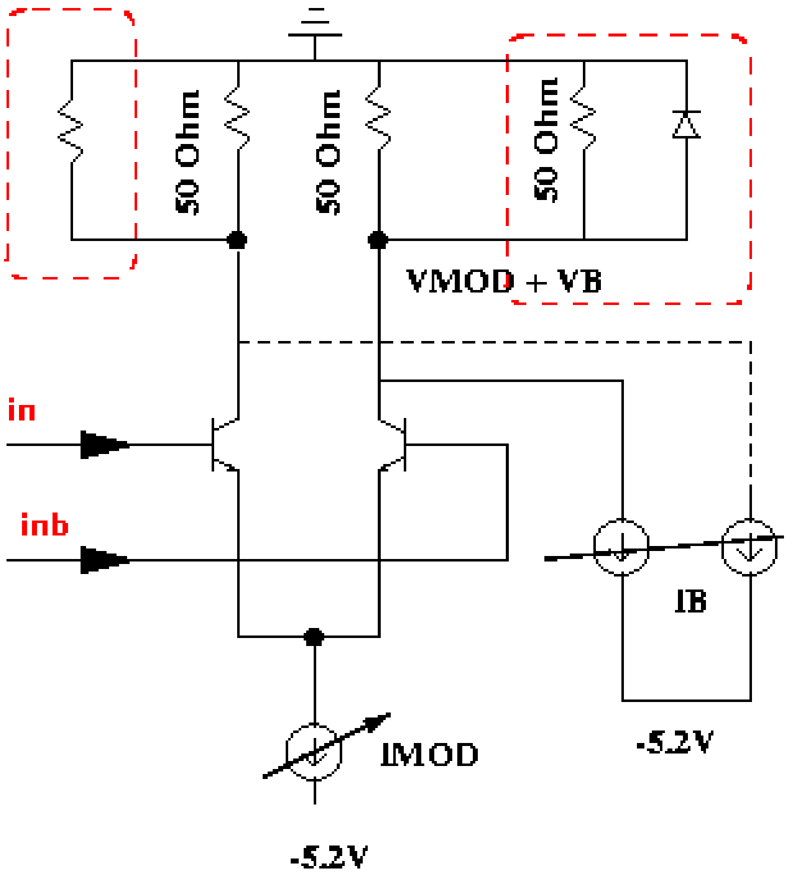


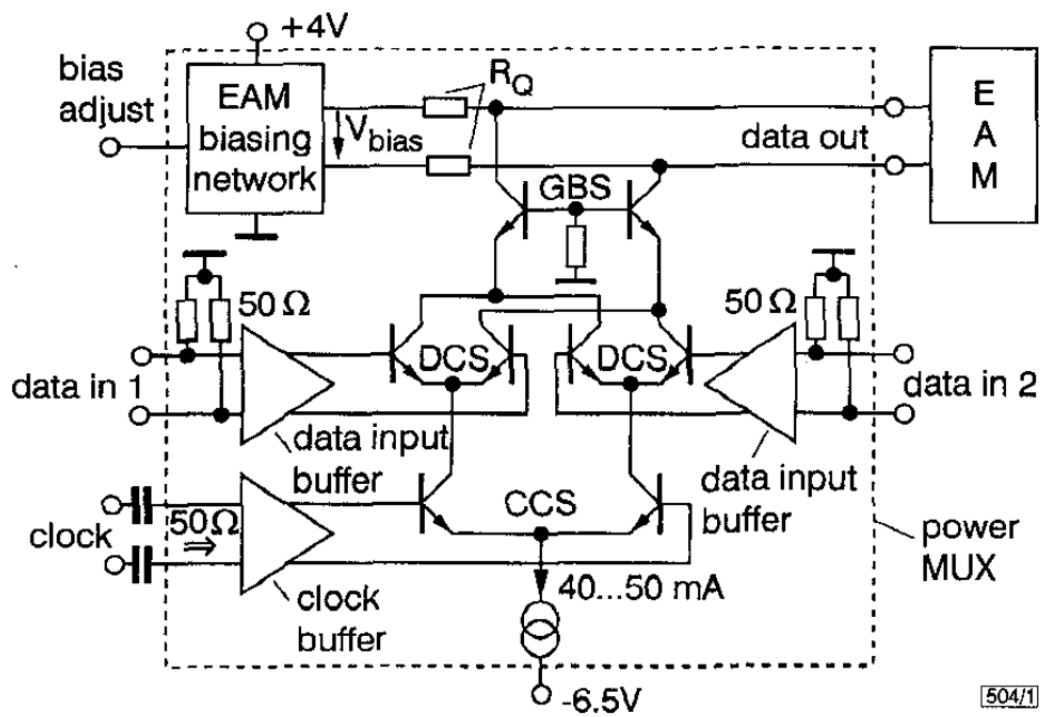
V_{SW} = 1.5 ... 4 V

ER = 11 ... 13 dB

- Reverse biased diode
  - → Capacitive load
  - → Nonlinear photocurrent
- Often parallel matching resistor

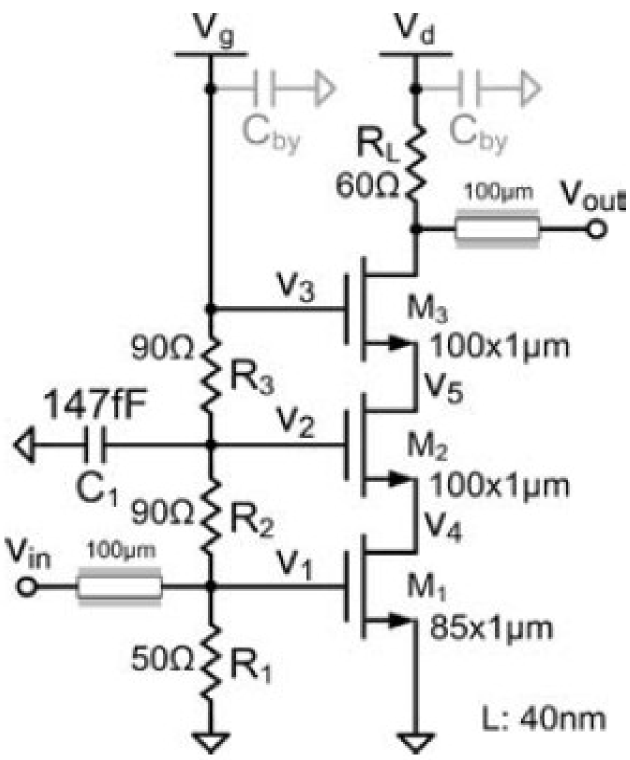
Types of drivers: EAM

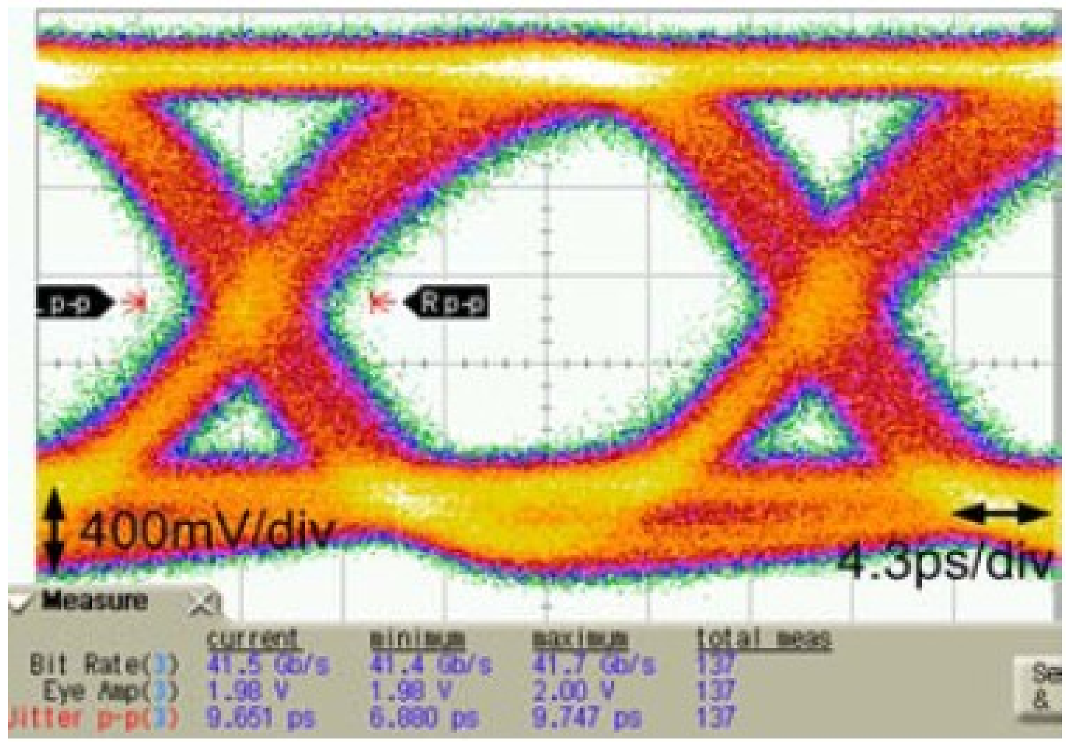




- EAM driver (R_L=50 Ω, C_L=0.05 .. 0.2 pF)

$2V_{pp}$, 40-Gb/s mod. driver in 45-nm SOI

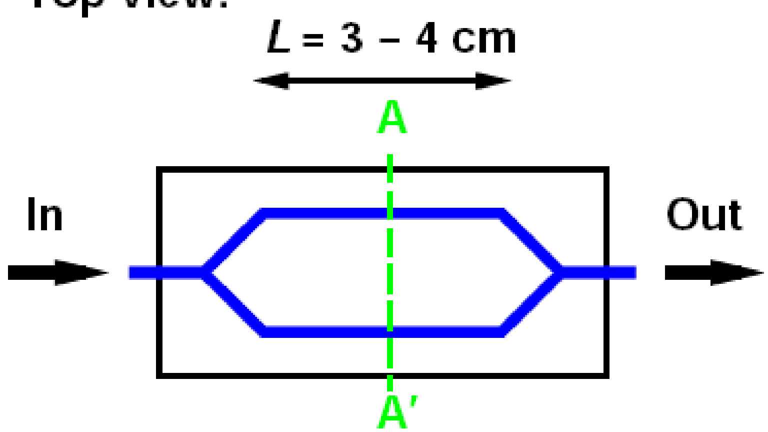




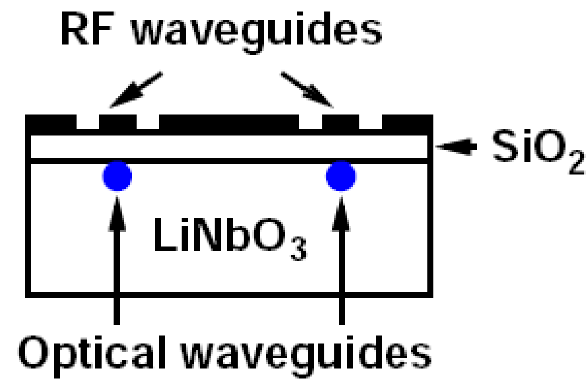
Based on PA super-cascode concept
(J. Buckwalter, UCSD, CICC-2010)

Types of drivers: Mach Zehnder Modulator

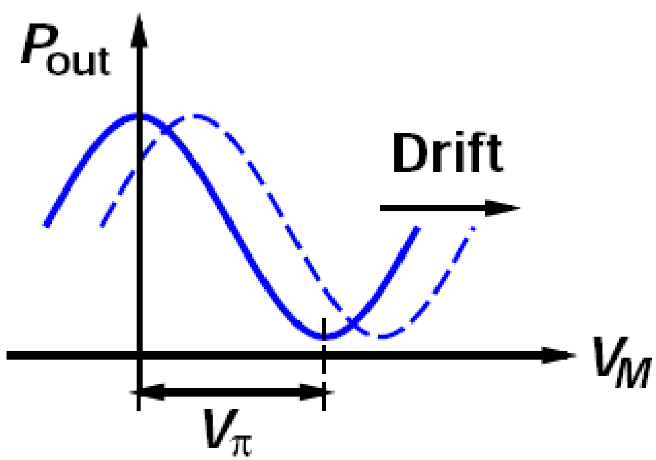
Top view:



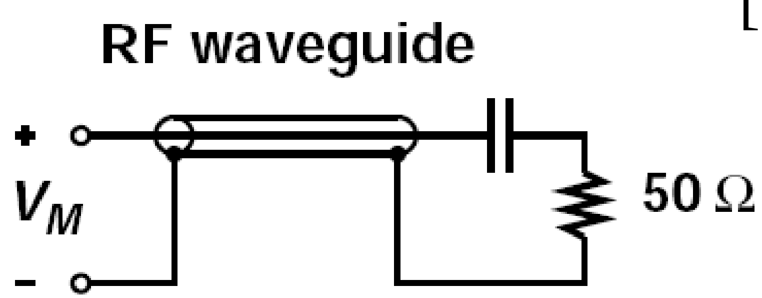
Cut A–A′:



[2]

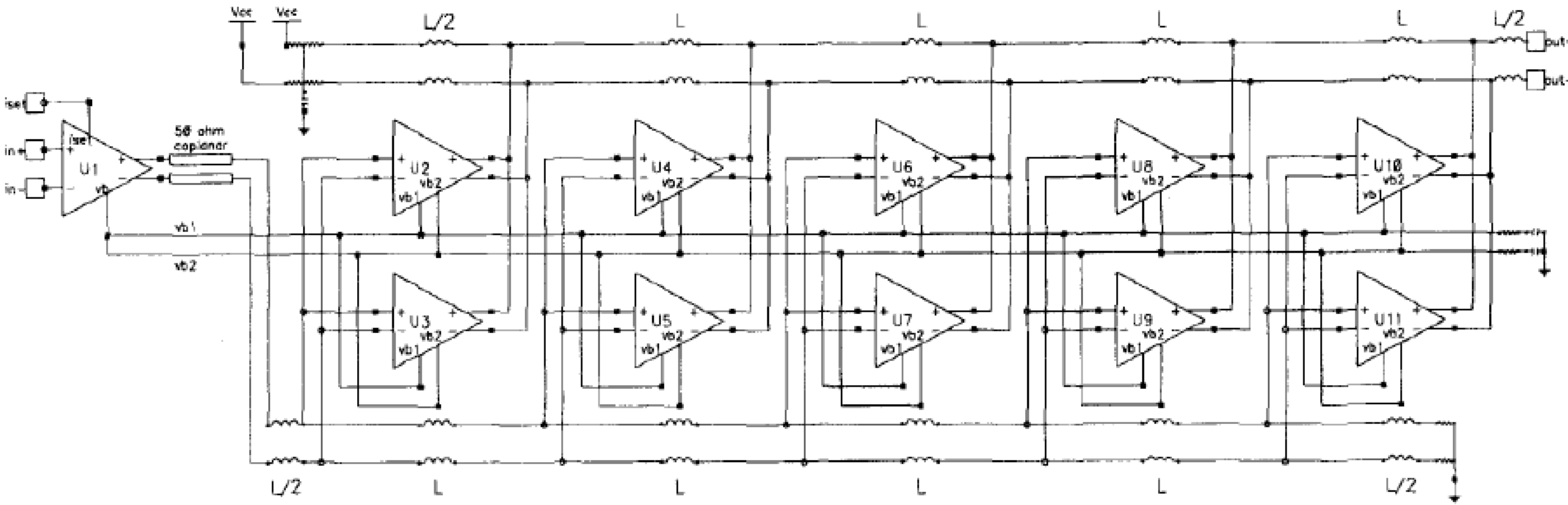


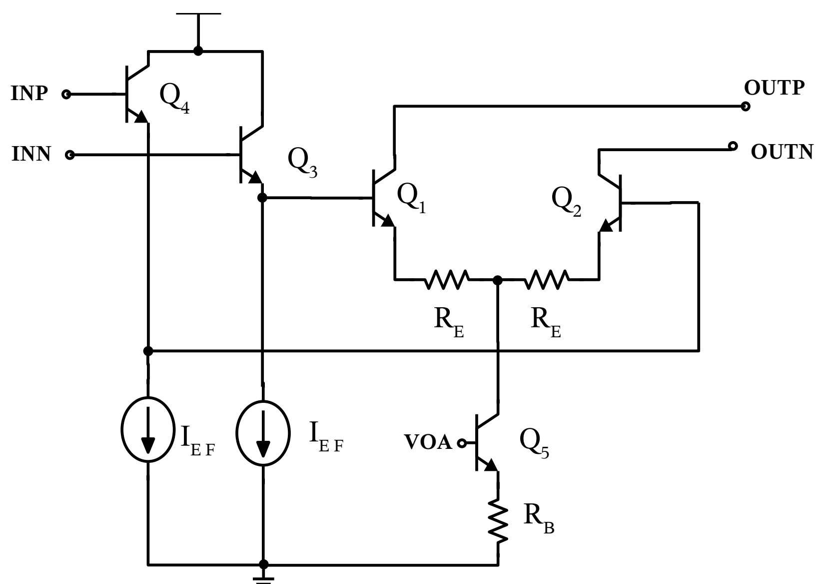
V_π = 4 ... 6 V
ER = 15 ... 17 dB



- Terminated transmission line
- Single– and dual–drive versions

Example of Mach-Zehnder Driver





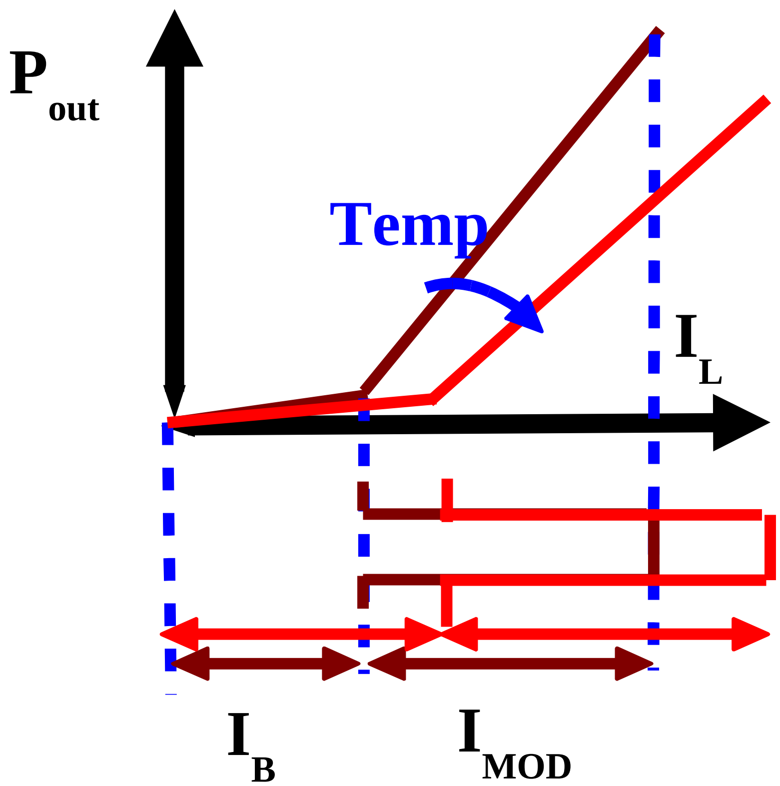
Outline

- Types of drivers
- Driver specification
- Driver building blocks and architecture
- Driver implementation and design examples

Driver Specification

- Modulation and bias current range (lasers)
- Voltage swing and bias voltage (modulators)
- Rise and fall time
- Input/output matching
- Pulse width distortion
- Jitter generation
- Eye-diagram mask test

Modulation and bias current range



Directly modulated lasers

- DFB, VCSEL

- I_B = 0 .. 80 (20) mA
- I_{MOD} = 5 .. 80 (15) mA

- Threshold and slope are temperature dependent
- DC or AC coupled

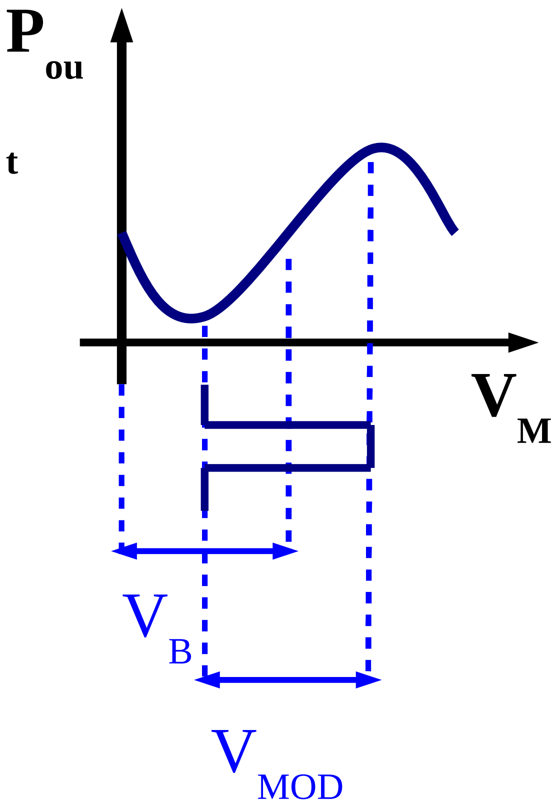
Voltage swing and bias voltage range

Externally modulated laser with EAM

- V_B = 0 .. 1 V
- V_{MOD} = 0.5 .. 3 V

- V_B (DC offset) must be adjustable from driver
- DC-coupled

Voltage swing and bias voltage range

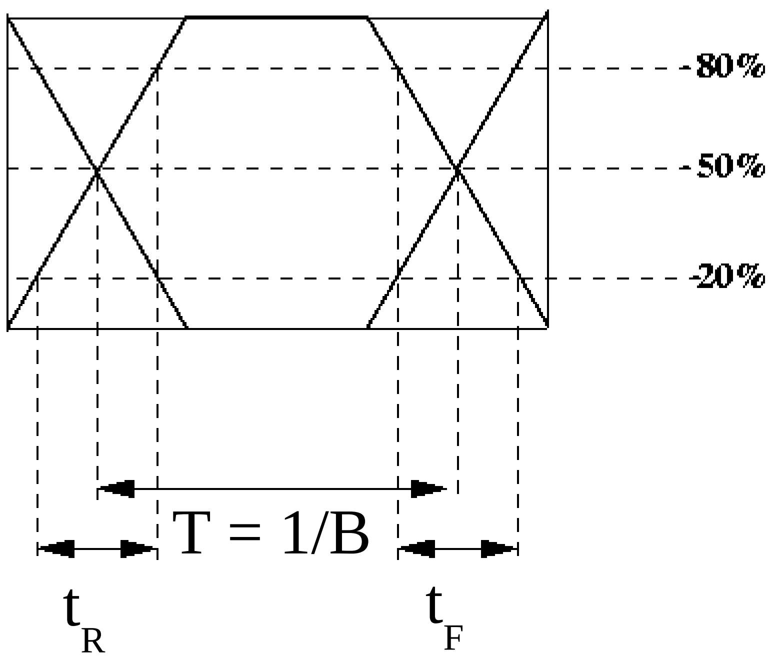


Externally modulated laser with MZM

- V_B = 1 .. 10 V
- V_{MOD} = 0.5 .. 5 V

- MZM V_B must be accurately set for $V_\pi/2$
- AC or DC coupled

Rise and fall time

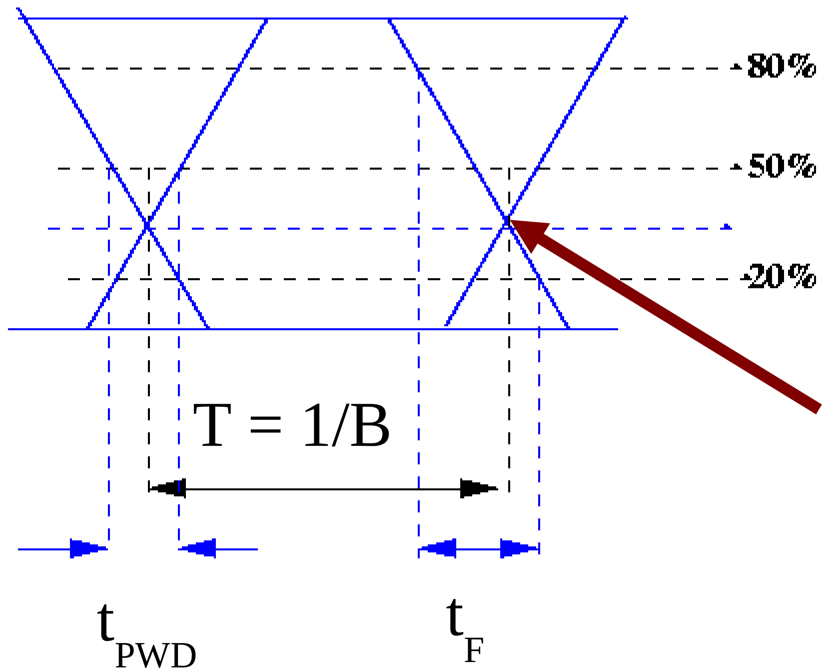


- B (or R_b) =bit rate
- T= period
- t_R and t_F
  - defined at 20% to 80%
  - less used: 10% to 90%

Input and output match: S_{11}, S_{22}

- < -15 dB for f < B/2
- < -10 dB for f < B
- < -5 dB for B<f<2B

Pulse width distortion (PWD or DCD)

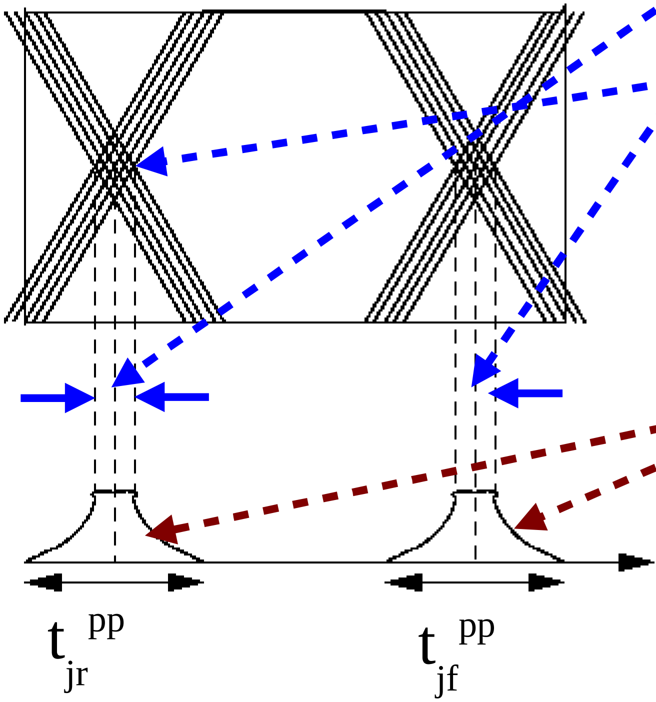


- T remains unchanged
- Eye crossing <> 50%

Eye crossing

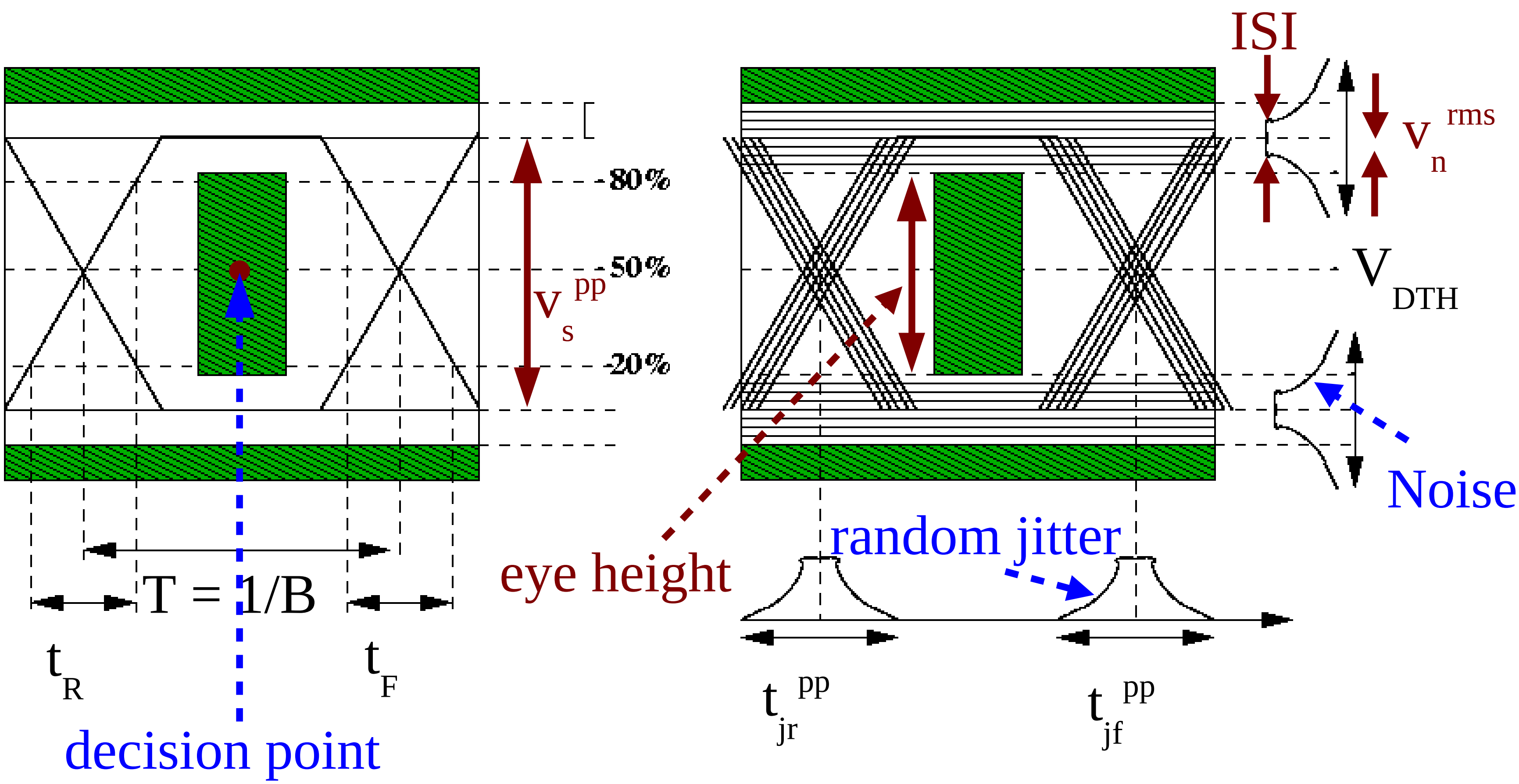
- Pulse width distorted

Jitter generation



- Deterministic jitter
  - double-edging
  - Peak-to-peak spec
- Random jitter
  - rms spec.
  - $t_j^{pp} = 14 \times t_j^{rms}$

Eye mask test

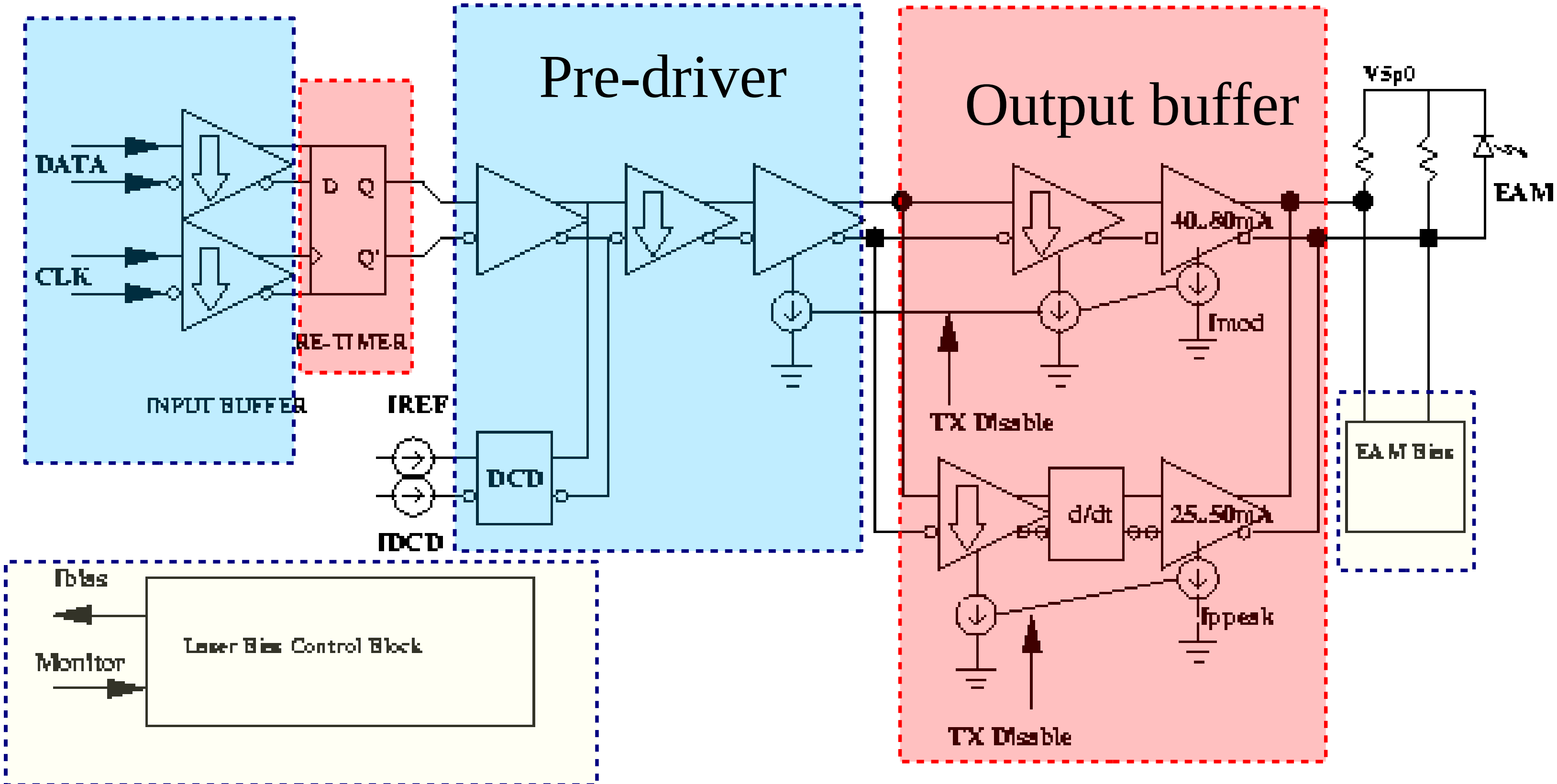


$Q = 1/(2Bt_j^{rms})$ $Q = v_s^{pp}/(2v_n^{rms})$

Outline

- Types of drivers
- Driver specification
- Driver building blocks and architecture
- Driver implementation and design examples

Driver architecture: traditional



- Input buffer
- Optional DFF re-timer
- Pre-driver
- Output buffer

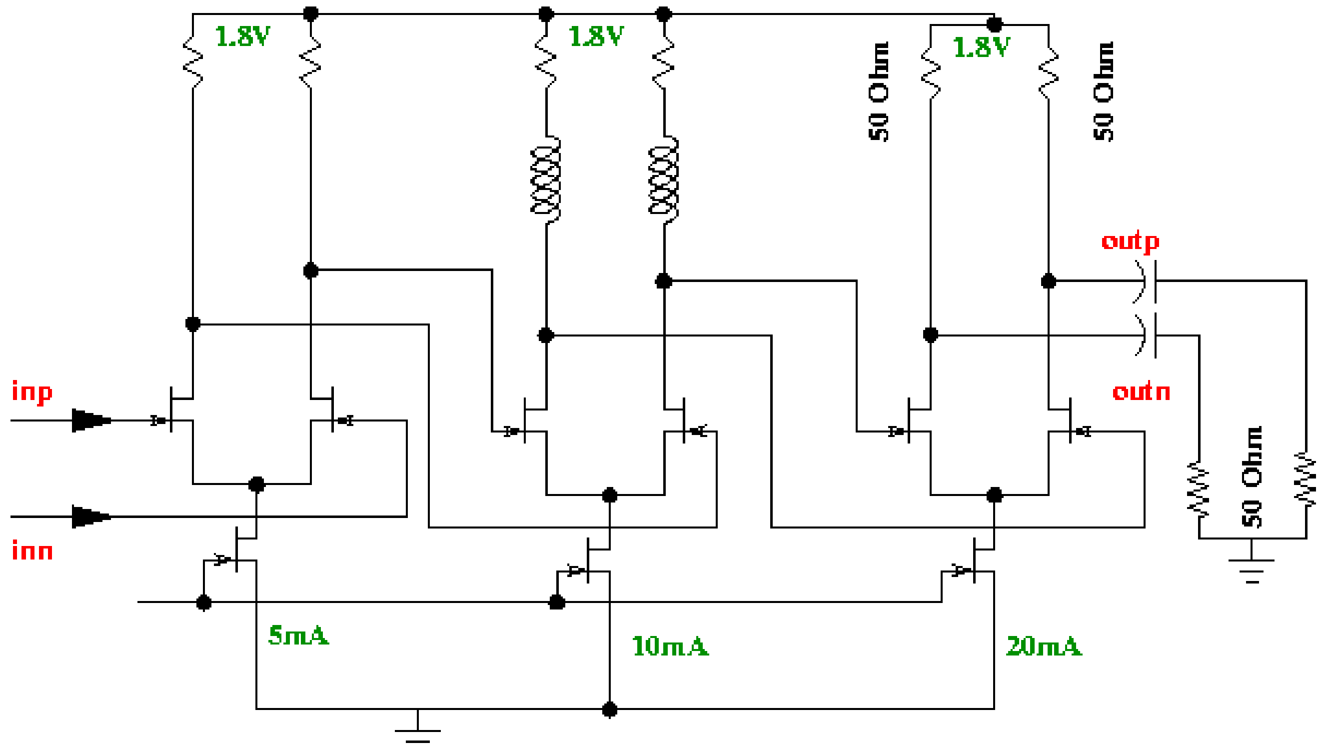
Driver architecture: DAC

- Latest trend, especially in long-haul fiberoptics
- Output swing limited to 400mVpp per side (to date)
- InP HBT, SiGe HBT and 65-nm CMOS

Driver building blocks

- Input buffer
- Pulse-width (duty cycle) control circuit
- Output buffer
  - with amplitude control (all)
  - with pre-emphasis control (VCSEL/DFB, equalizer)
  - with DC offset control (EAM)

Output buffer: 10 Gb/s 1.8V 0.18 μm CMOS



- Inductive peaking in penultimate stage » use 3-term ind.
- $L = CR^2/3.1(2.4)$ for best group delay (flat gain response)

M.M. Green et al. ISSCC-2002

0.13μm CMOS design example

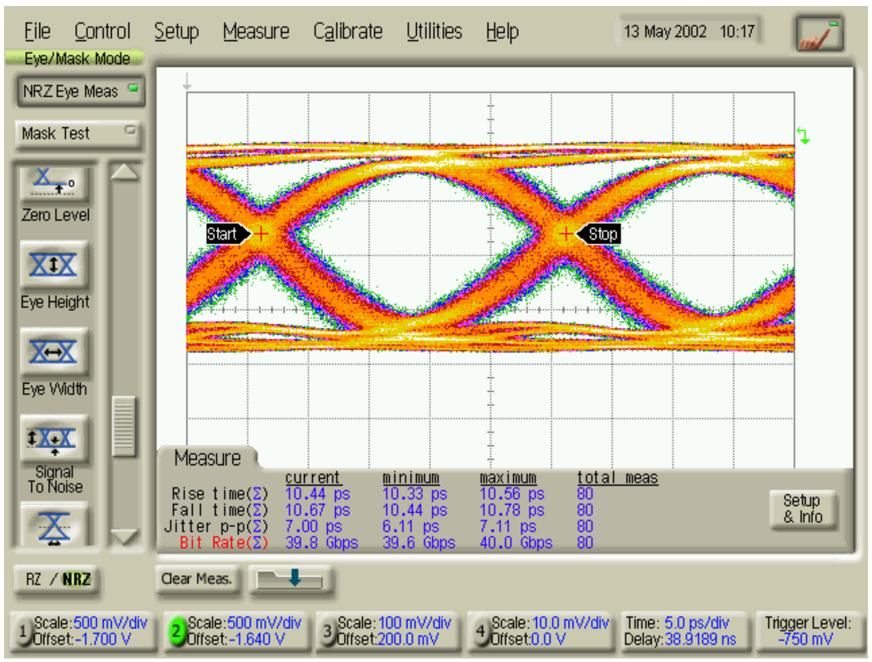
- $\Delta V = 0.6\ V_{pp}$ per side
- $I_{MOD} = 24$ mA
- $I_{MOD} / (J_{pfT}) = W\ (Q_{1,2})$
- $W = 24mA/(0.3mA/\mu m) = 80\ \mu m$
- $W_f = 4\ \mu m$, $N_f = 20$
- $V_{eff} = 0.3V$; $g_m = 64$ mS

0.13µm CMOS design example (ii)

- $\tau = R_G(C_{gs} + 3C_{gd}) + 25\,(C_{db} + C_{gd} + C_{PAD})$
- $\tau = 10(100\text{ fF} + 120\text{ fF}) + 25\,(140\text{ fF} + 40\text{ fF} + 50\text{ fF})$ $= 2.2\text{ ps} + 5.75\text{ ps} \Rightarrow BW_{3dB} = 20\text{ GHz}$
- In reality input node time constant limited by previous stage R_o
- To improve speed:
  - add inductive peaking,
  - use distributed topology or else
  - reduce swing

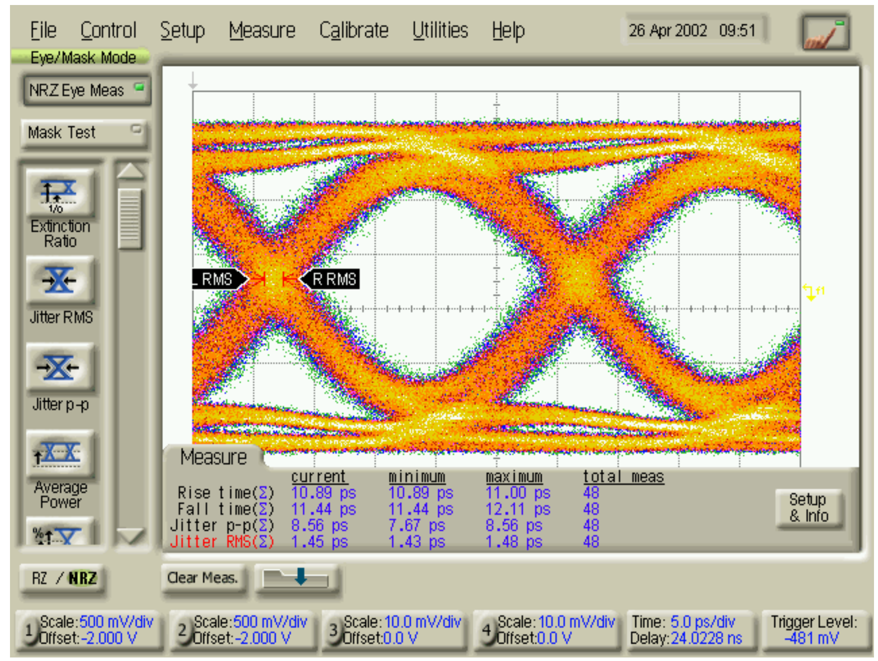
Output amplitude control applied at 40 Gb/s in GaAs p-HEMT driver

Low amplitude



Output swing of 1.7 V

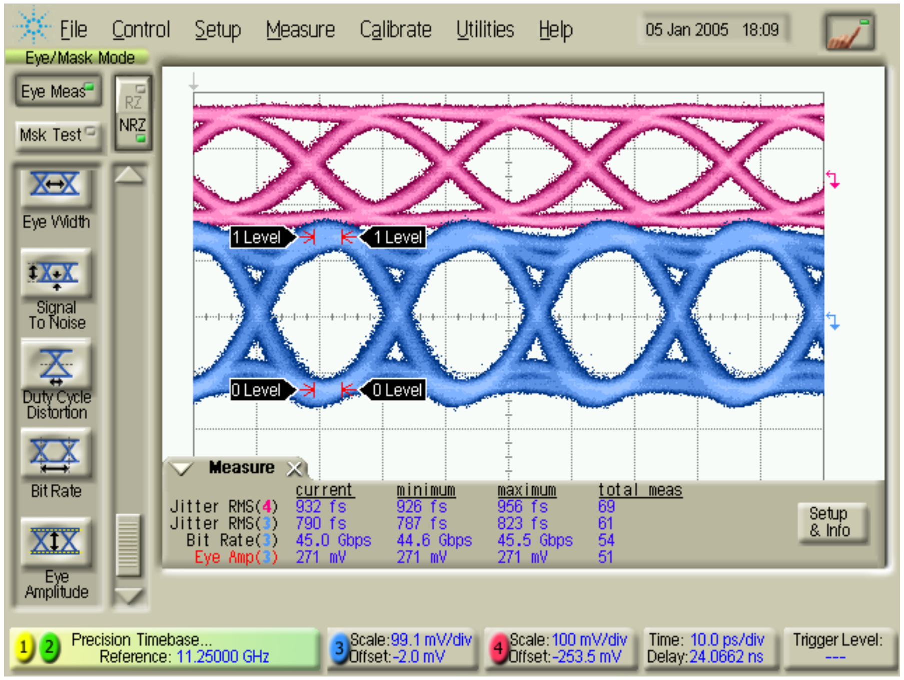
Maximum amplitude

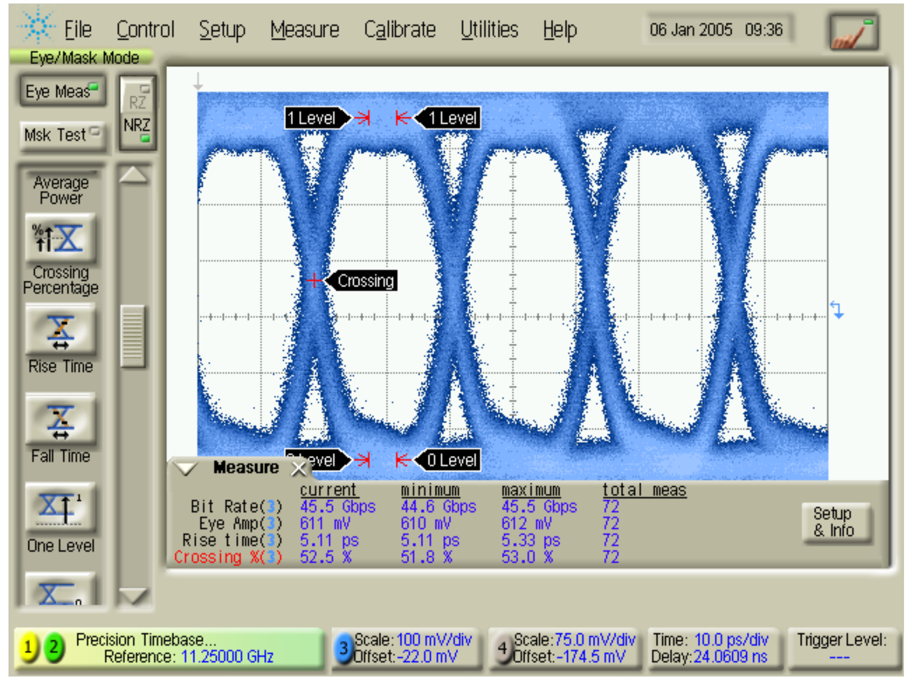


Output swing of 3 V

D. McPherson et al. GaAs IC Symposium -2002

Output amplitude control in 45-Gb/s SiGe BiCMOS driver



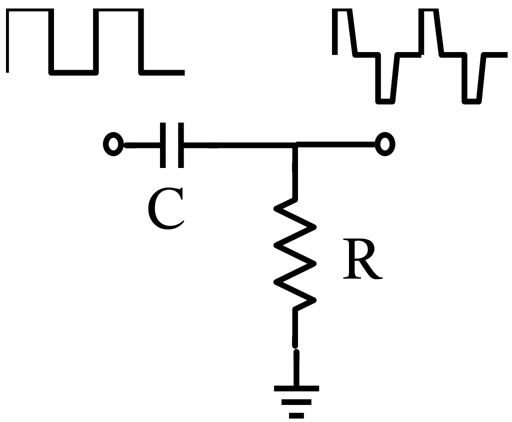


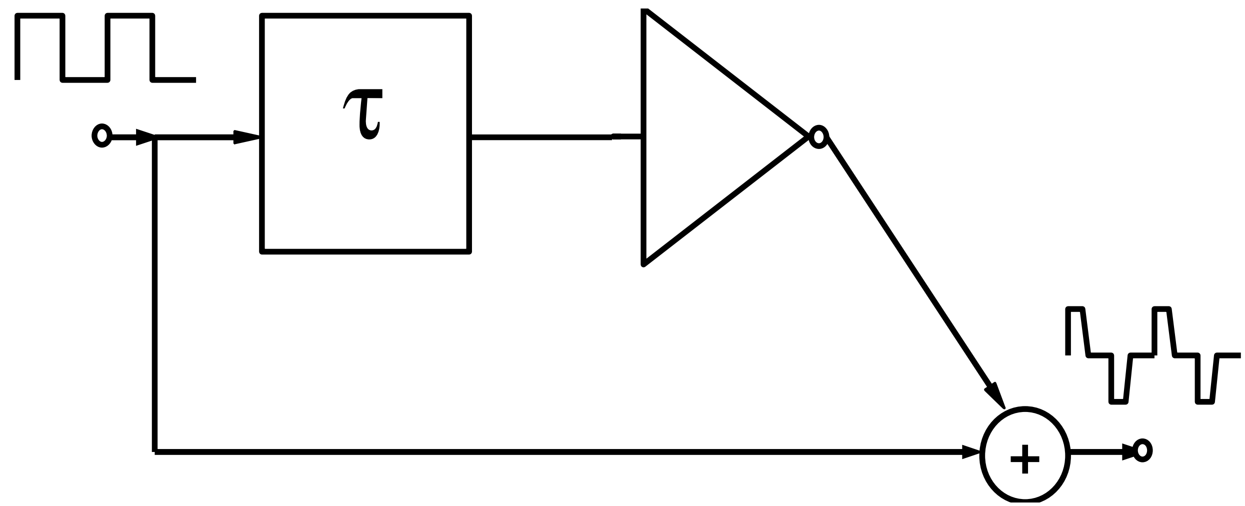
Output: 611 mV$_{pp}$ - per side

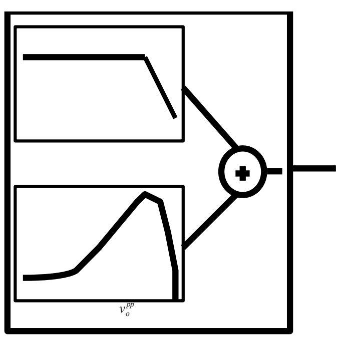
Input (top)
Output (bottom): 270 mV$_{pp}$ - per side

T. Dickson (JSSC, Aug. 2006)

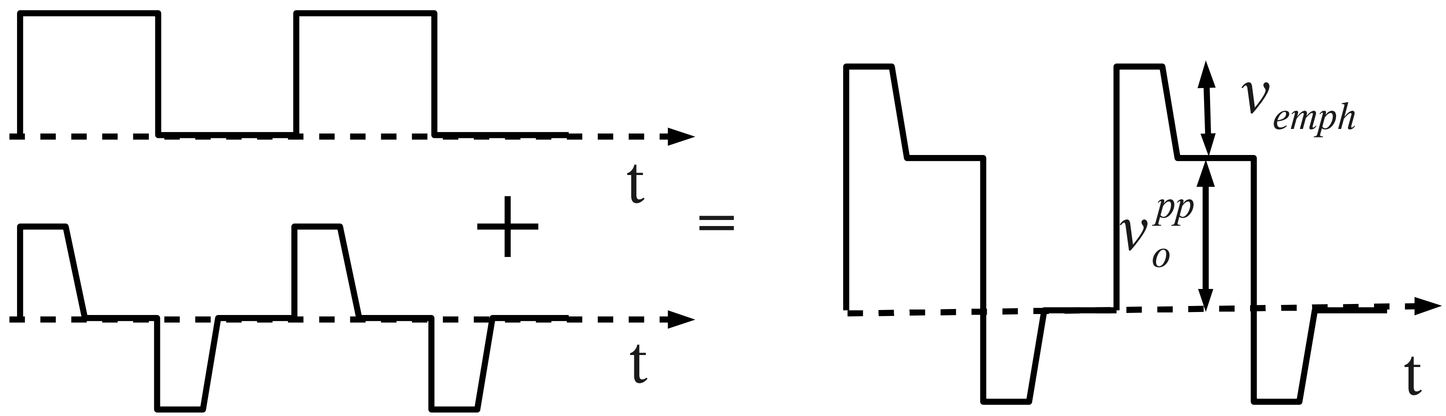
Pre-emphasis control concept





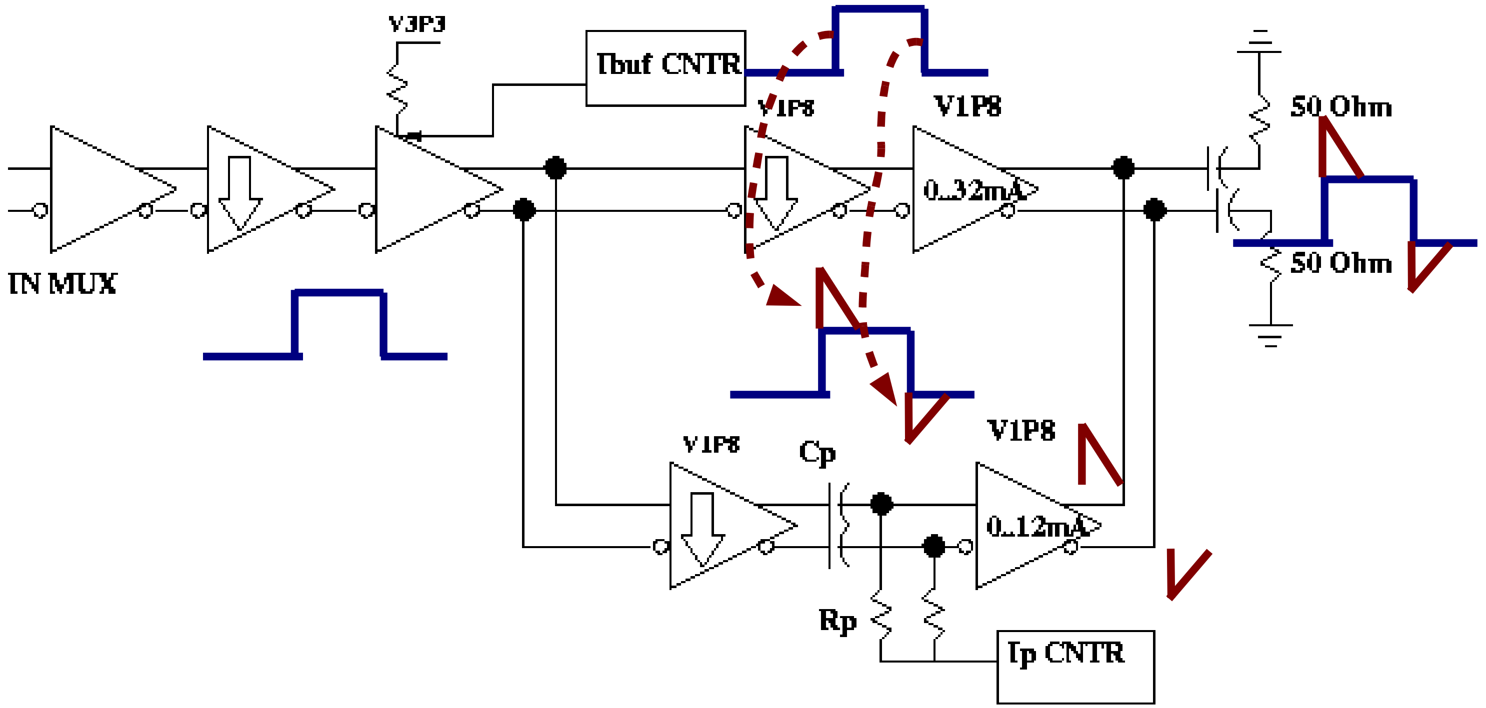


Frequency domain



Output buffer with analog pre-emphasis

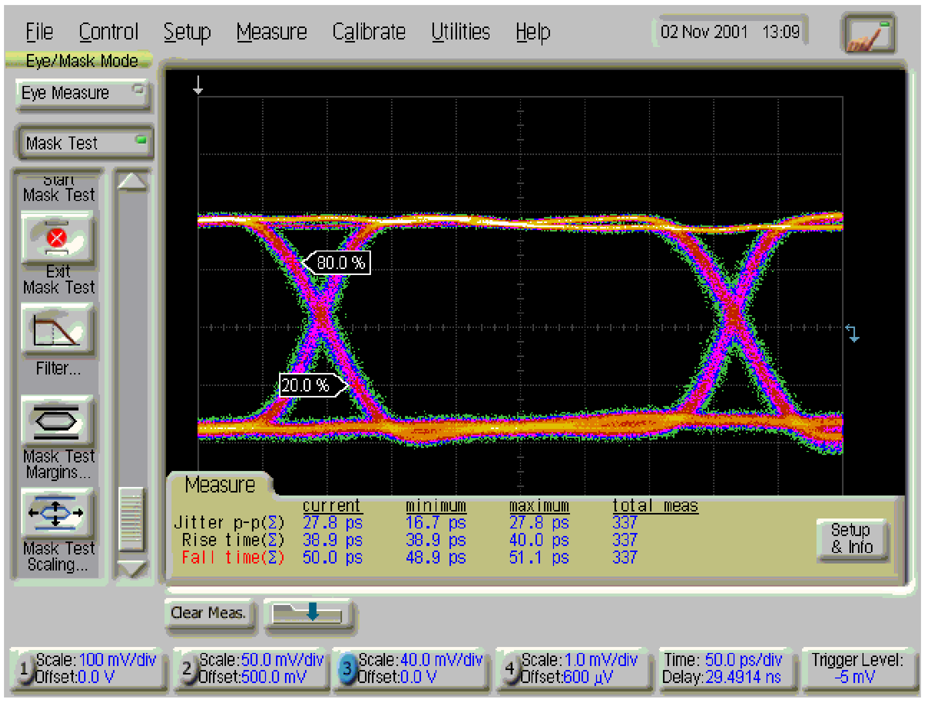
400–800mV/side, up to 50% peaking, to max 800mV per side.

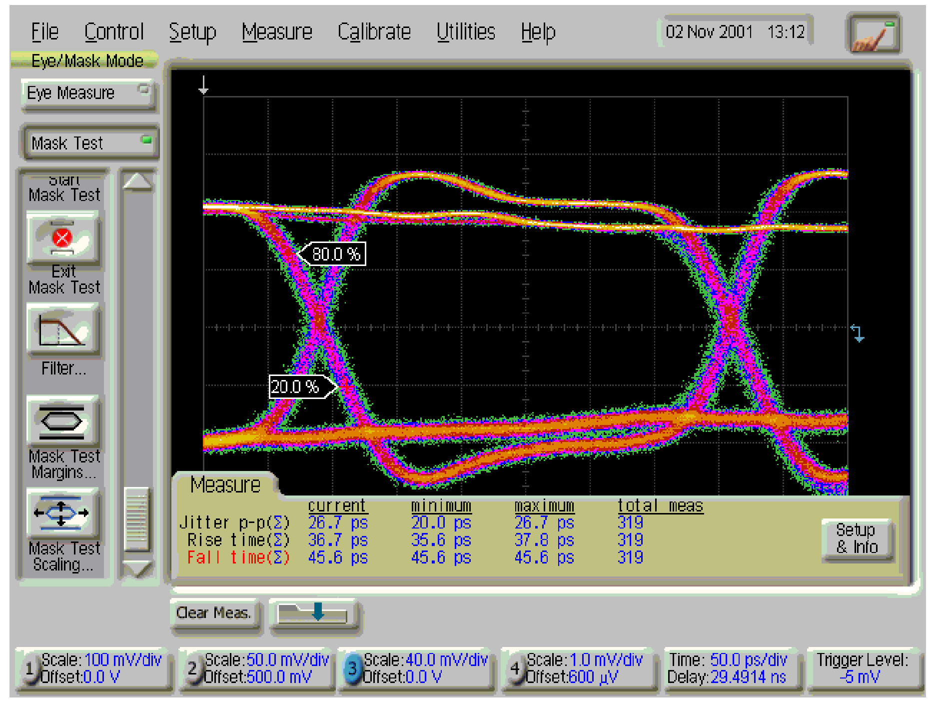


- main path with amplitude control
- Parallel path with differentiator and current summer

Pre-emphasis in 3.125-Gb/s backplane driver

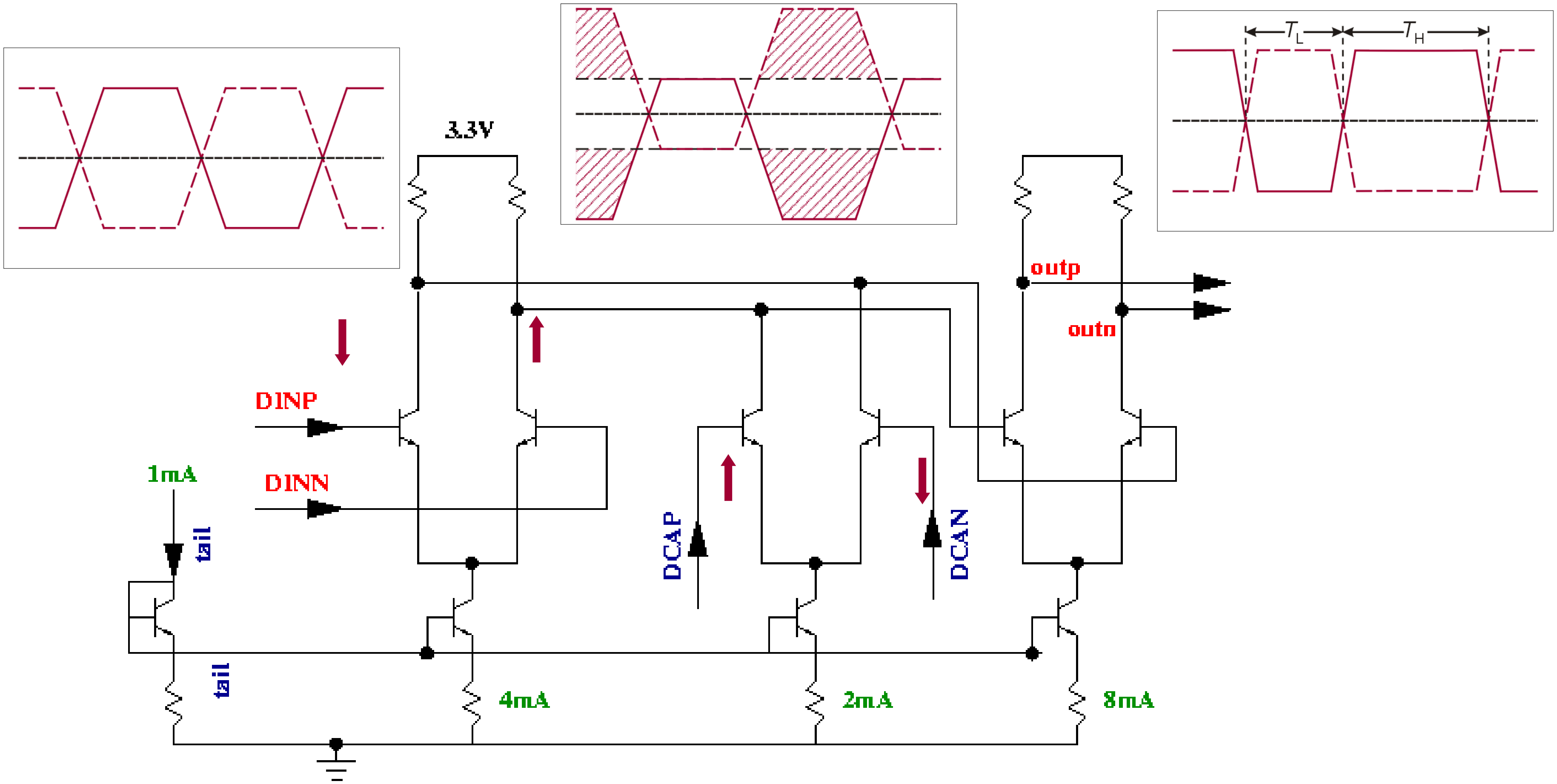
No peaking | **25% peaking**





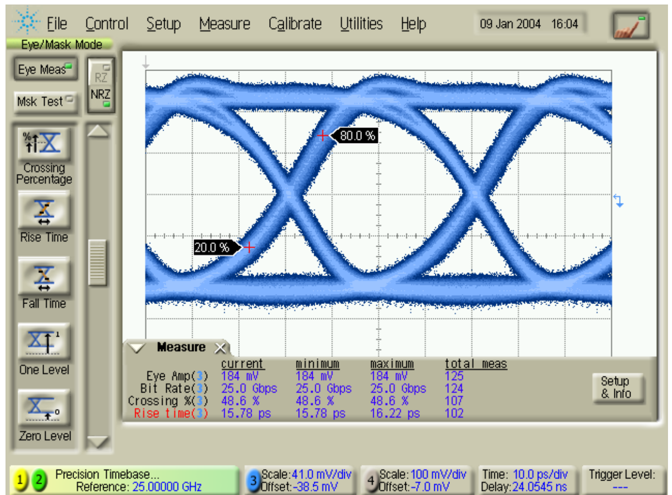
Courtesy of Quake Technologies, 2001

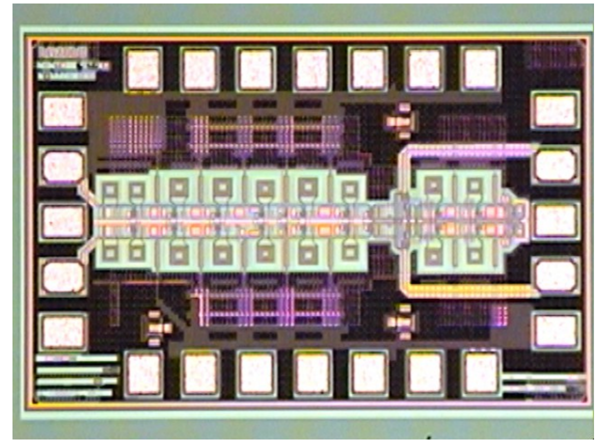
Pulse-Width Control Concept



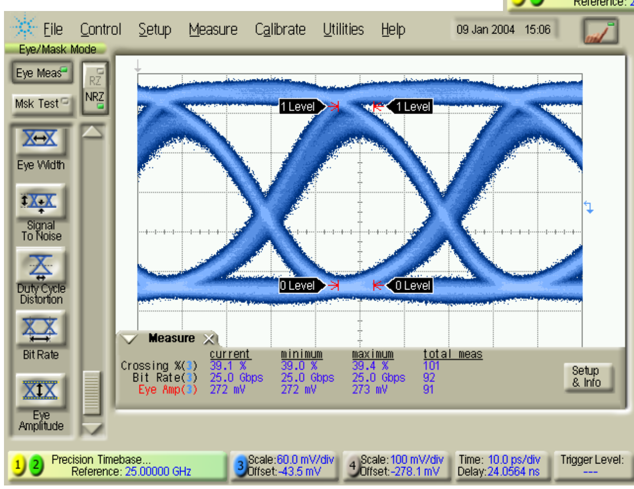
- Pre- and post hard limiter required
- High speed data signal *DIN* + DC control *DCAP*

PW control in 25-Gb/s 0.13μm CMOS driver

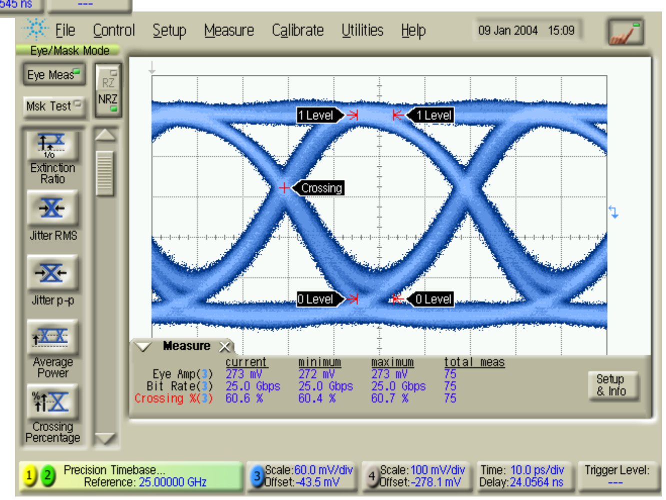




50%



40%

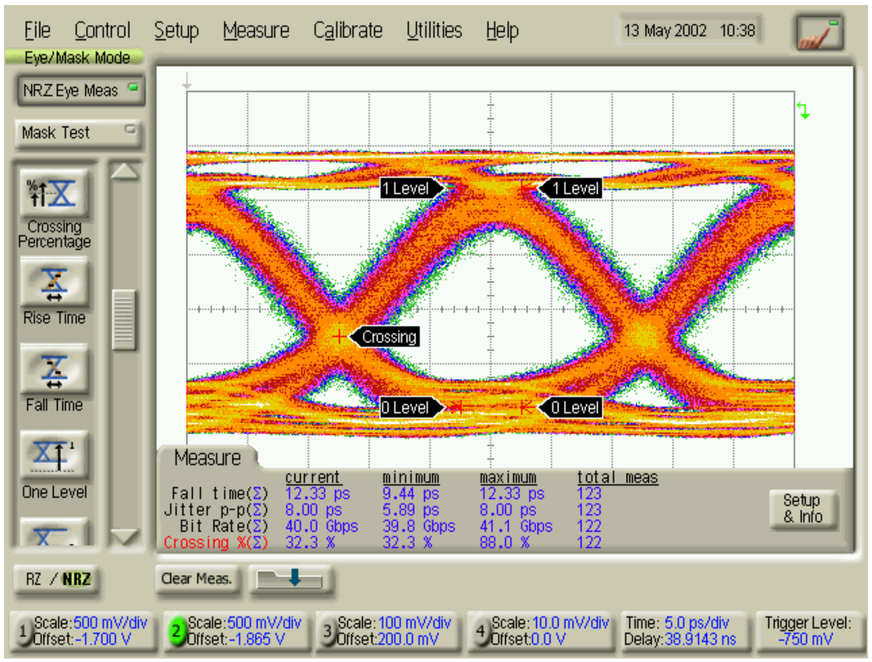


60%

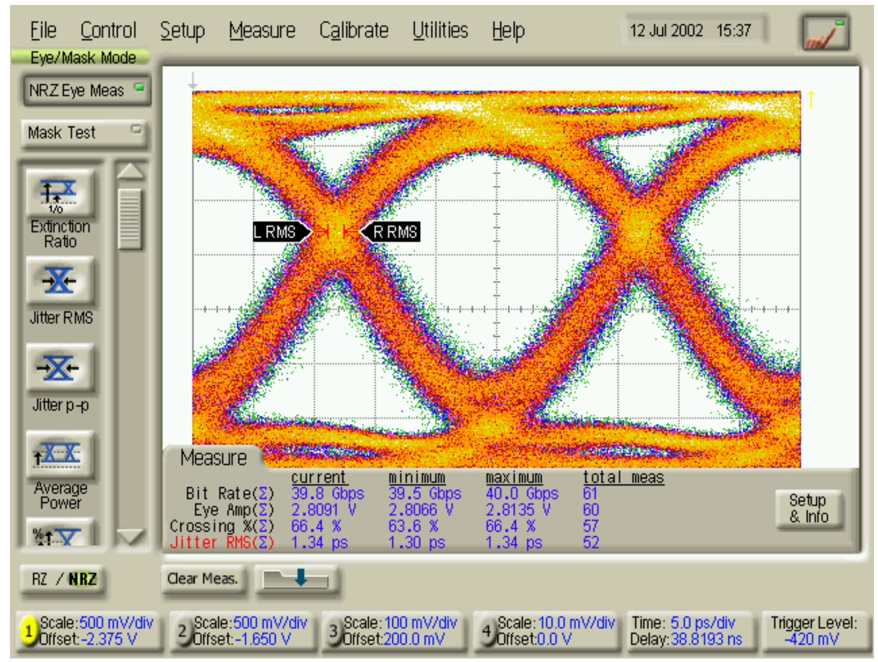
P. Westergaard et al. CICC-2004

PW control at 40 Gb/s in GaAs p-HEMT driver

30% DCD

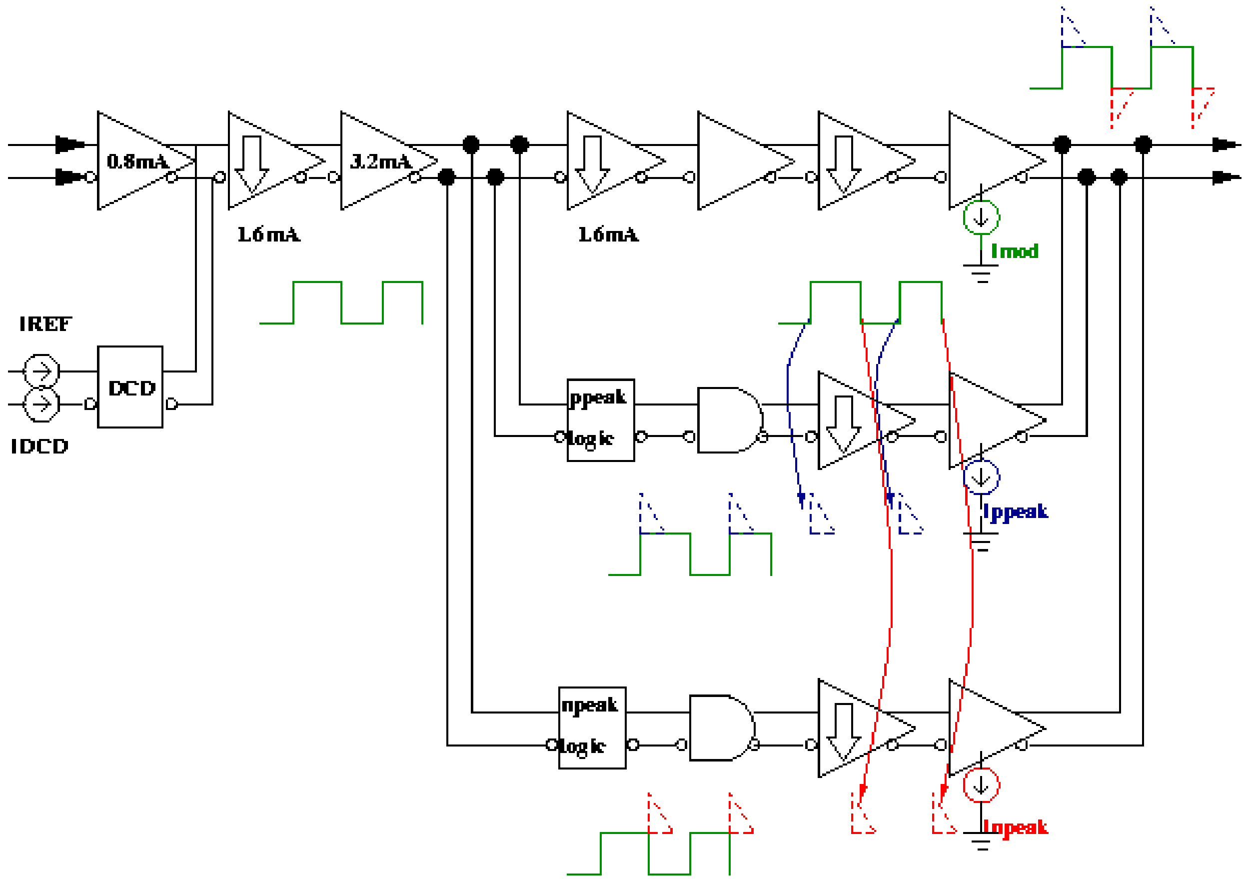


66% DCD



D. McPherson et al. GaAs IC Symposium -2002

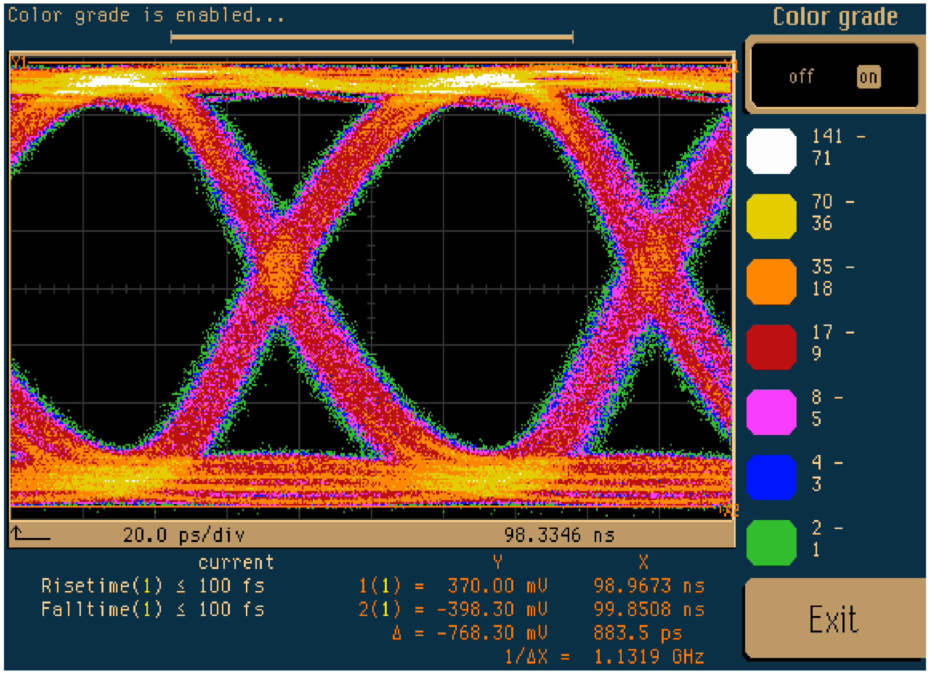
Output buffer with digital pre-emphasis



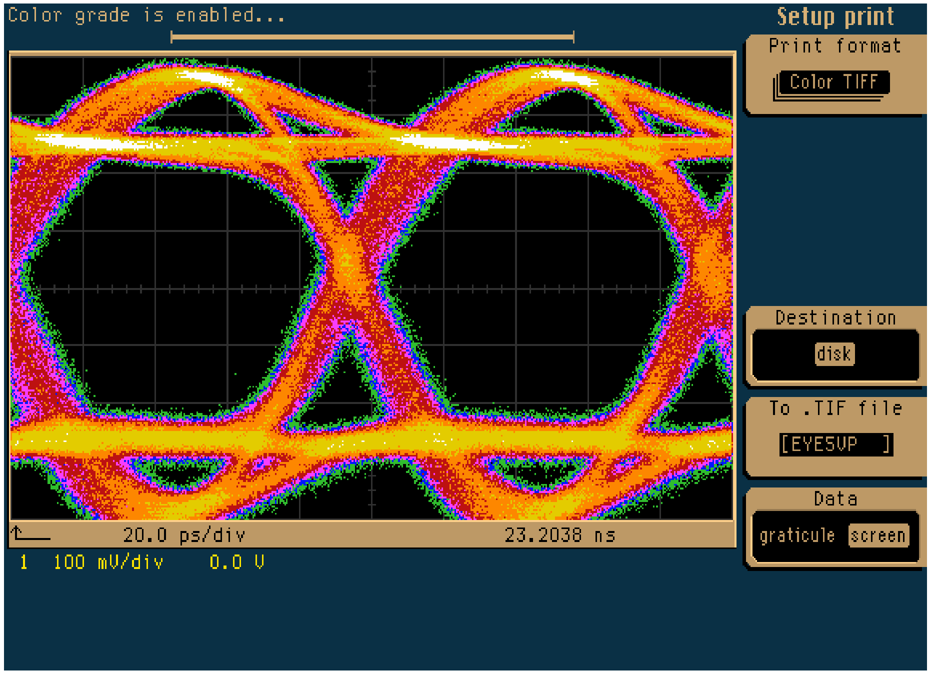
- main path with amplitude control
- two parallel paths with differentiator for leading and falling edge, respectively

Pre-emphasis control with 800 mV$_{pp}$ per side in 10-Gb/s SiGe BiCMOS VCSEL driver

No peaking



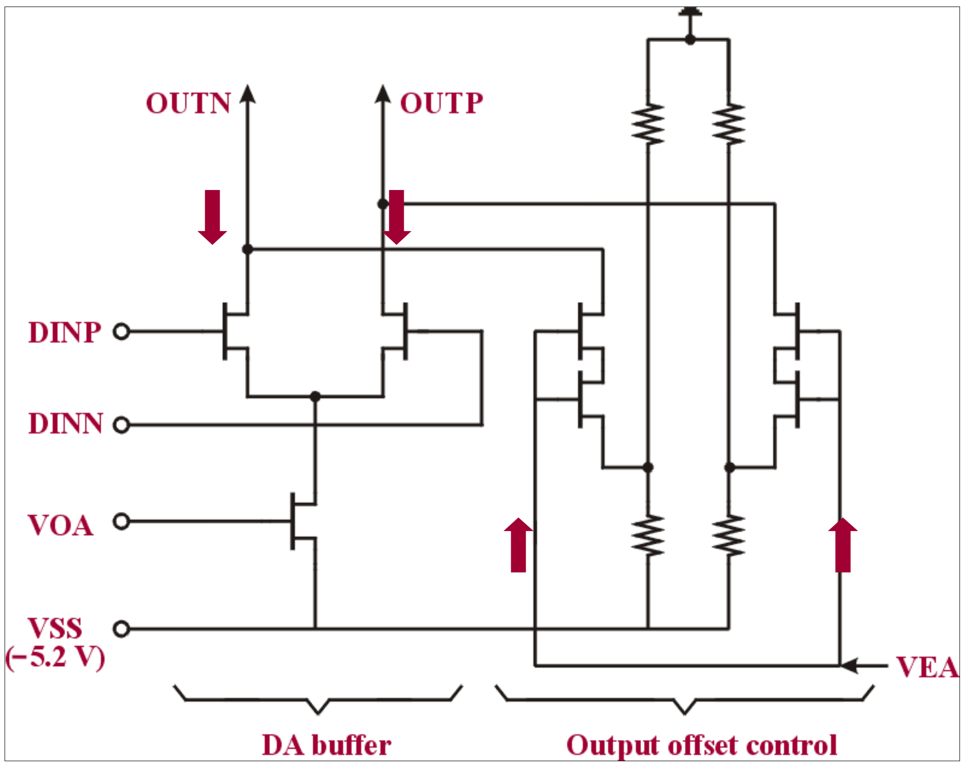
25% peaking



S. P. Voinigescu et al. CICC-2001

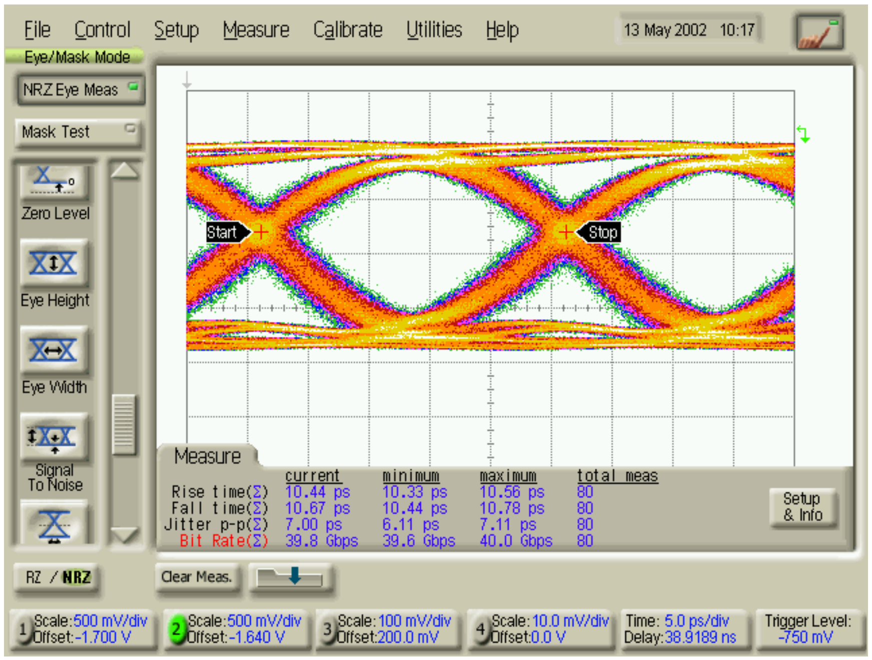
Output DC offset control implementation

Output offset control



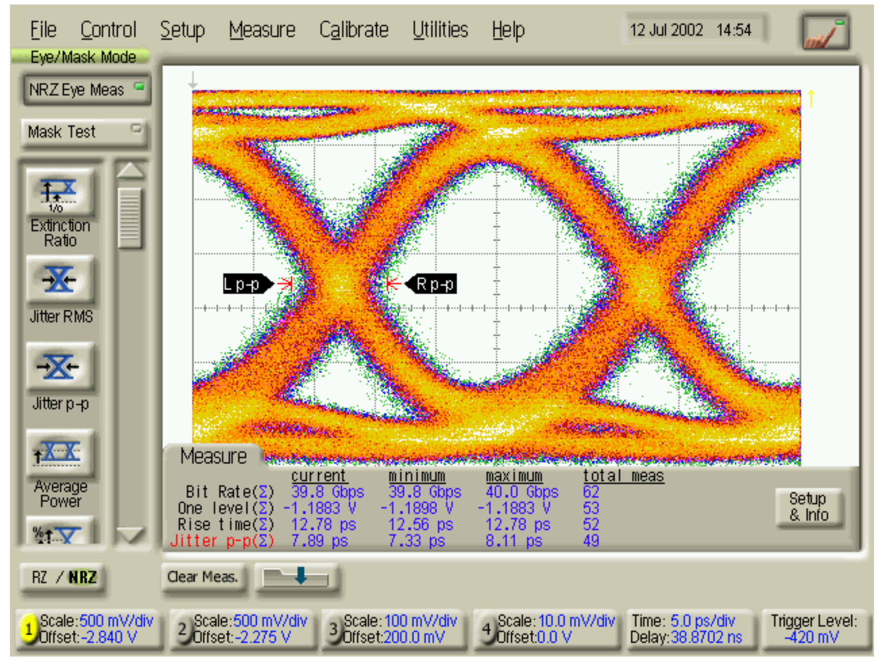
Output DC offset control applied at 40 Gb/s

Minimum offset



"1" level at -0.2 V

Maximum offset



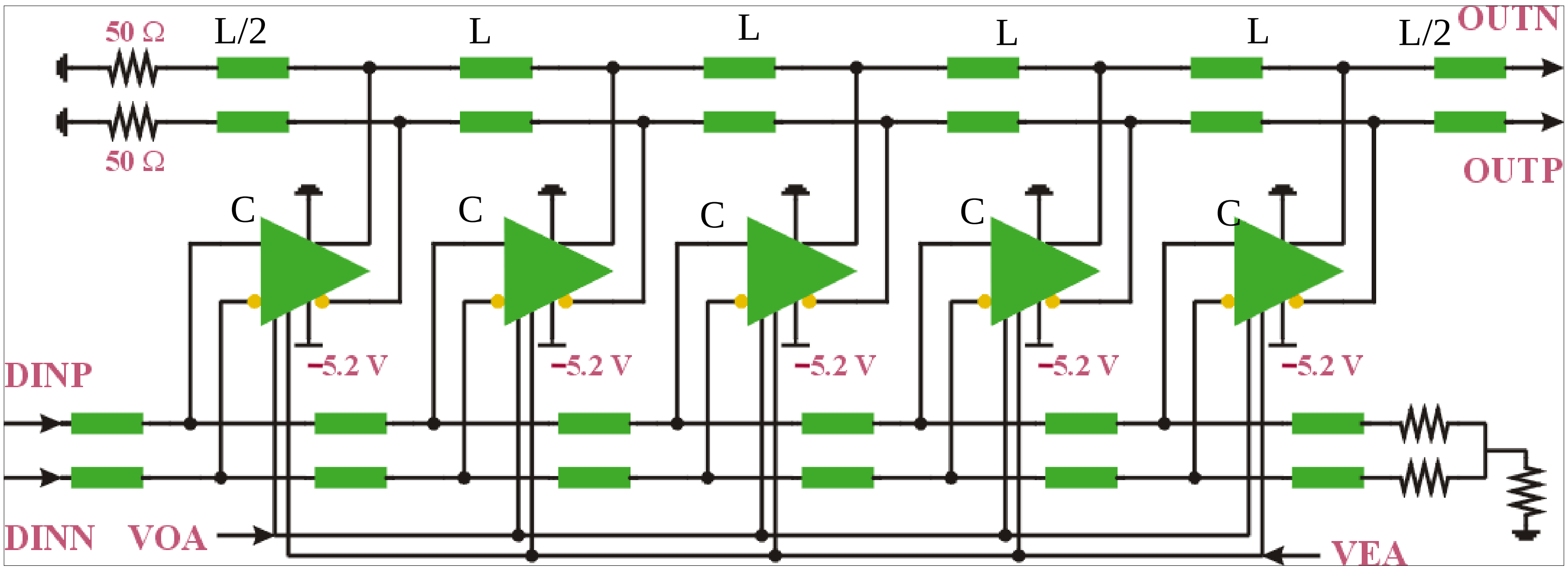
"1" level of –1.2 V

D. McPherson et al. GaAs IC Symposium -2002

Distributed output stage

Lumped output:

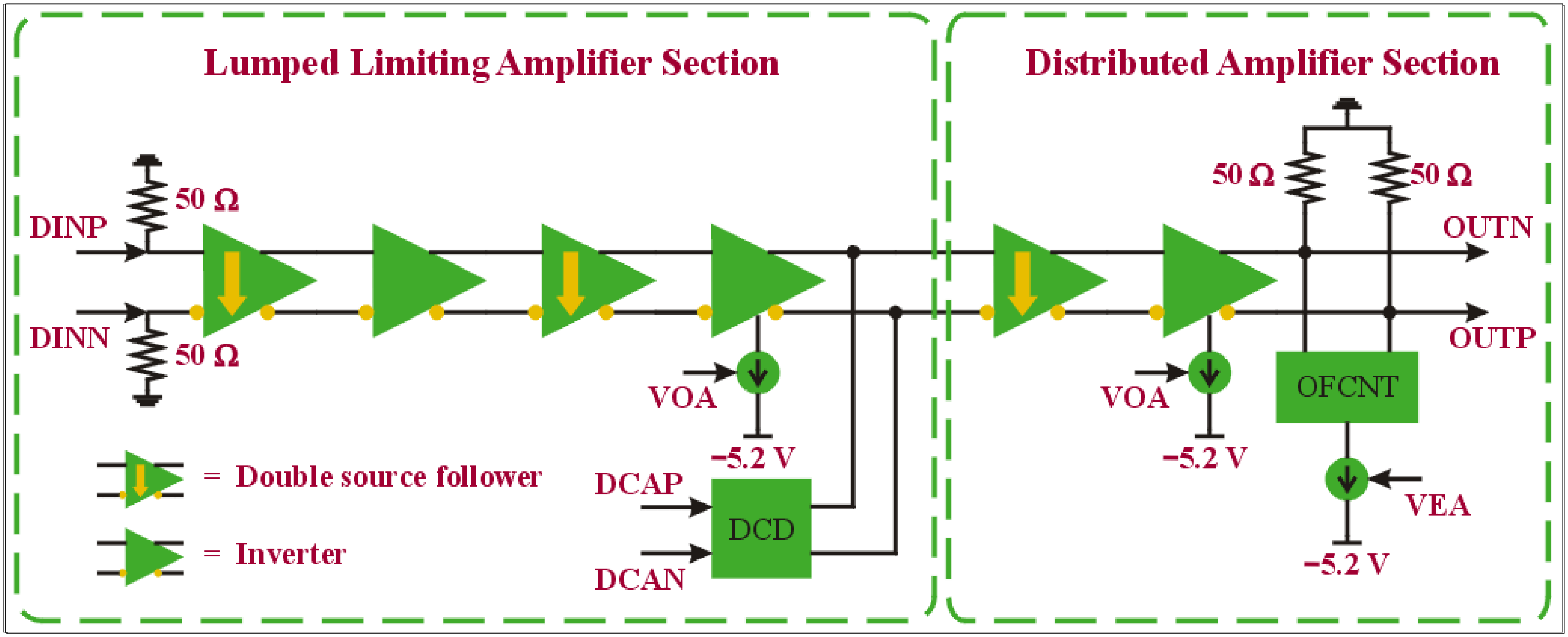
$$BW_{3\text{dB}} = \frac{1}{\pi * R_L * C_T}$$



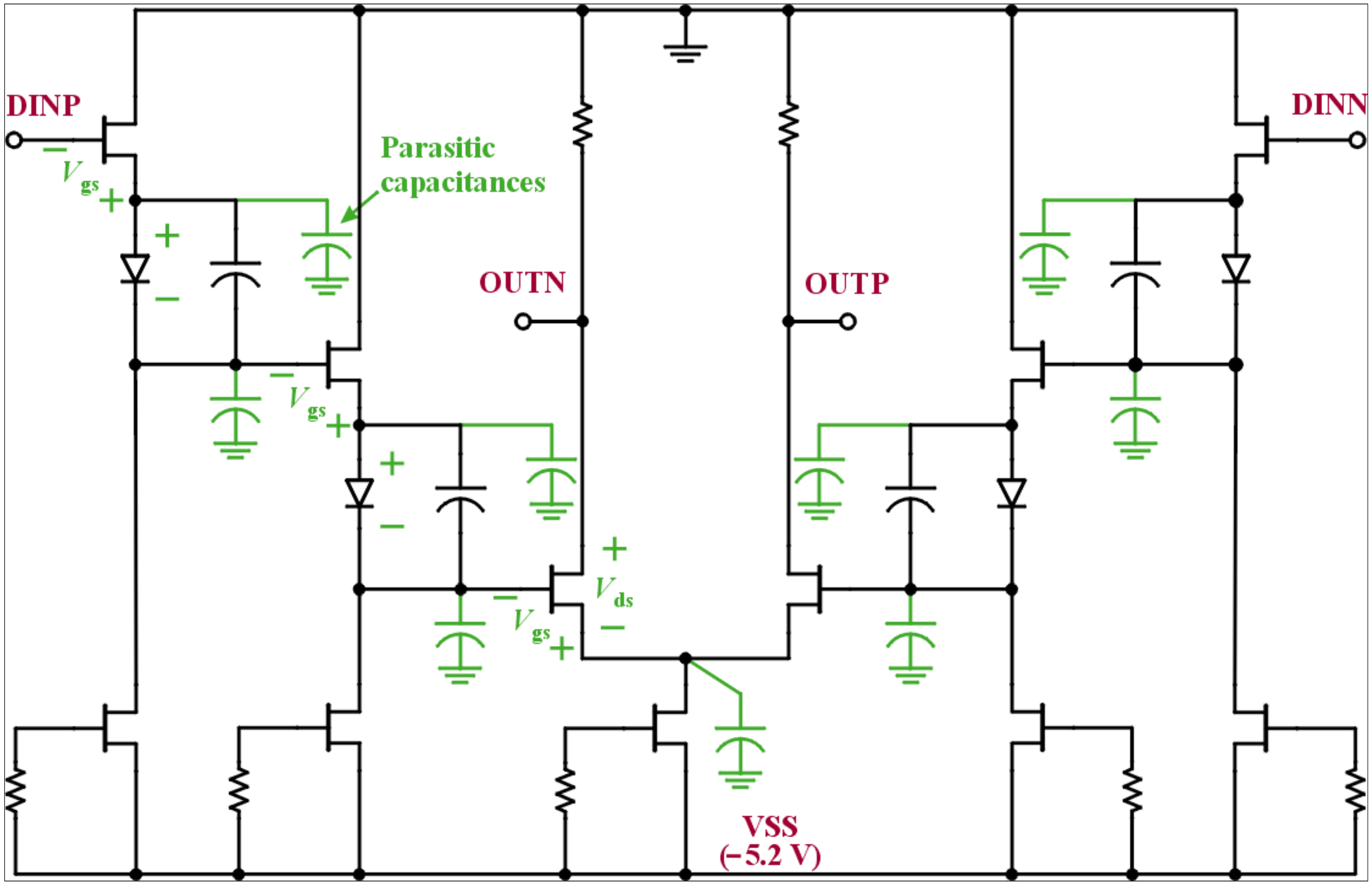
Distributed output:

$$C_T = n \times C \qquad Z_O = \sqrt{\frac{L}{C}} \qquad BW_{3\text{dB}} = \frac{1}{\pi \times \sqrt{L \times C}}$$

40-Gb/s EA driver schematic

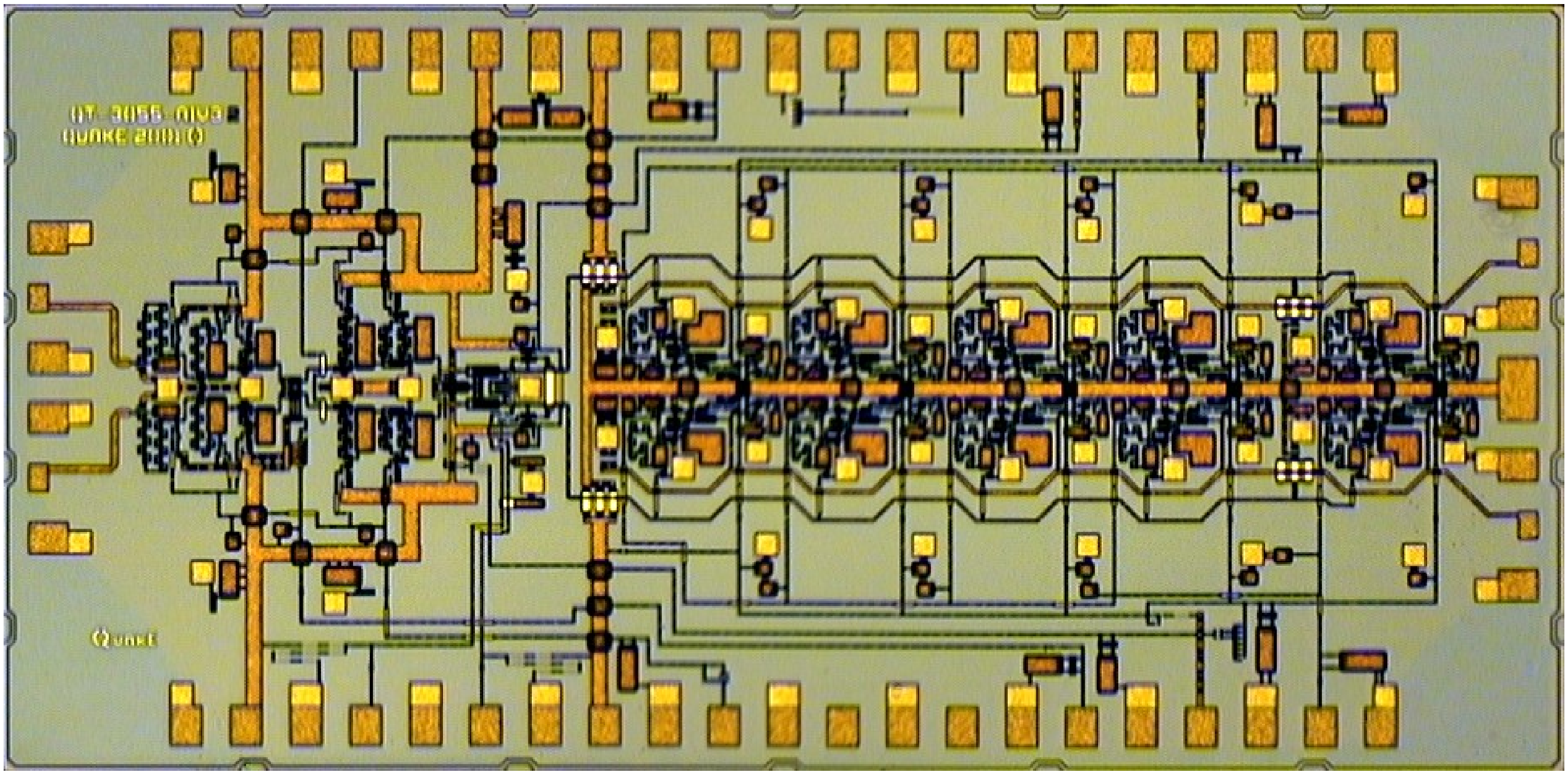


Gain block architecture



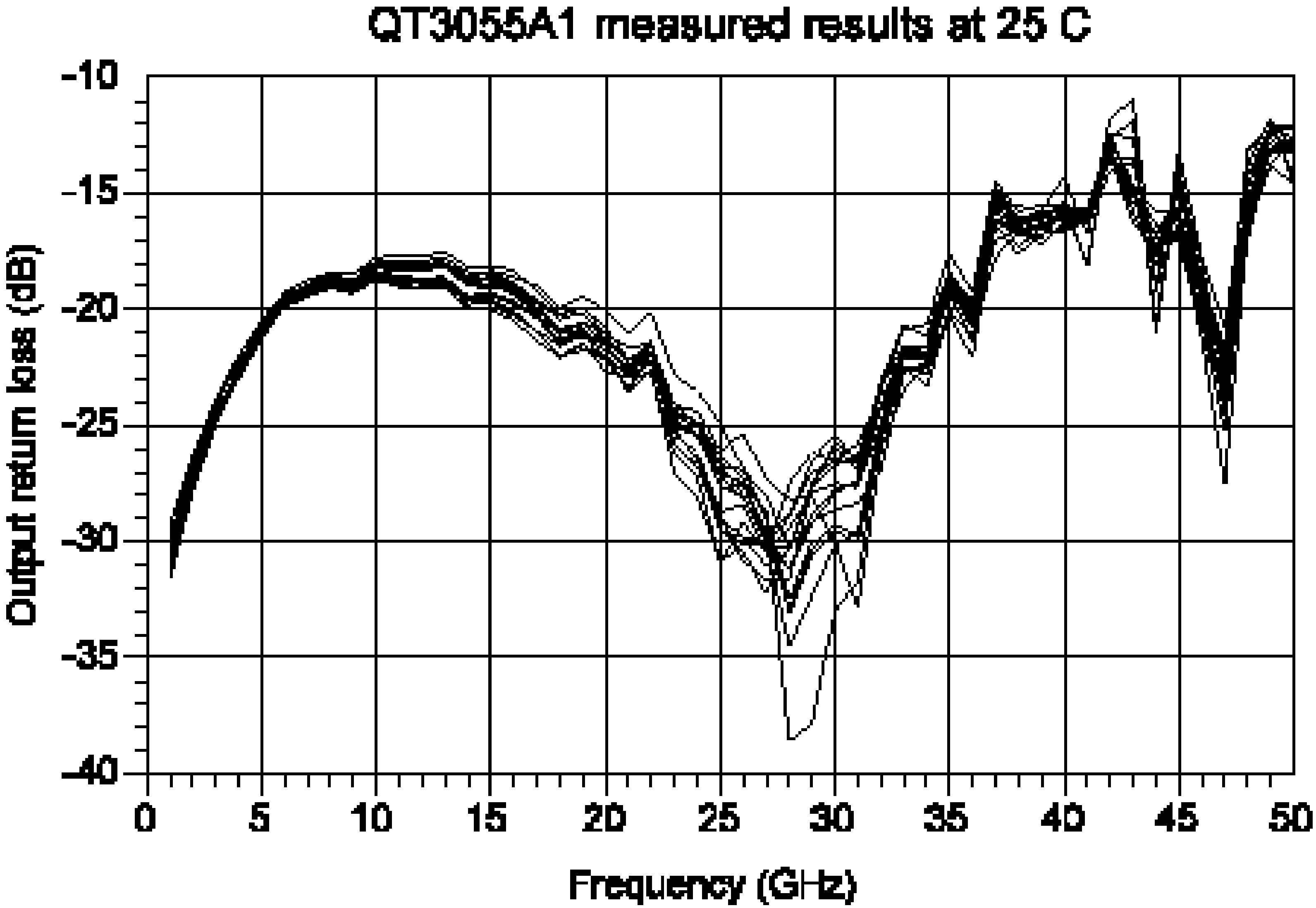
D. McPherson et. al. GaAs IC Symposium -2002

40-Gb/s EA modulator driver layout



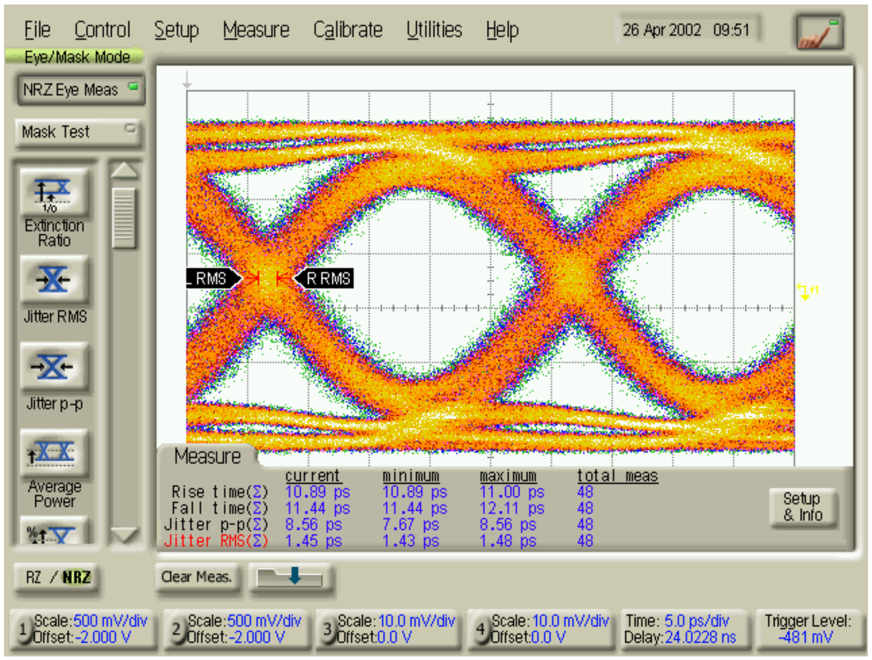
D. McPherson et. al. GaAs IC Symposium -2002

On-Wafer S22 Measurements: 18 parts

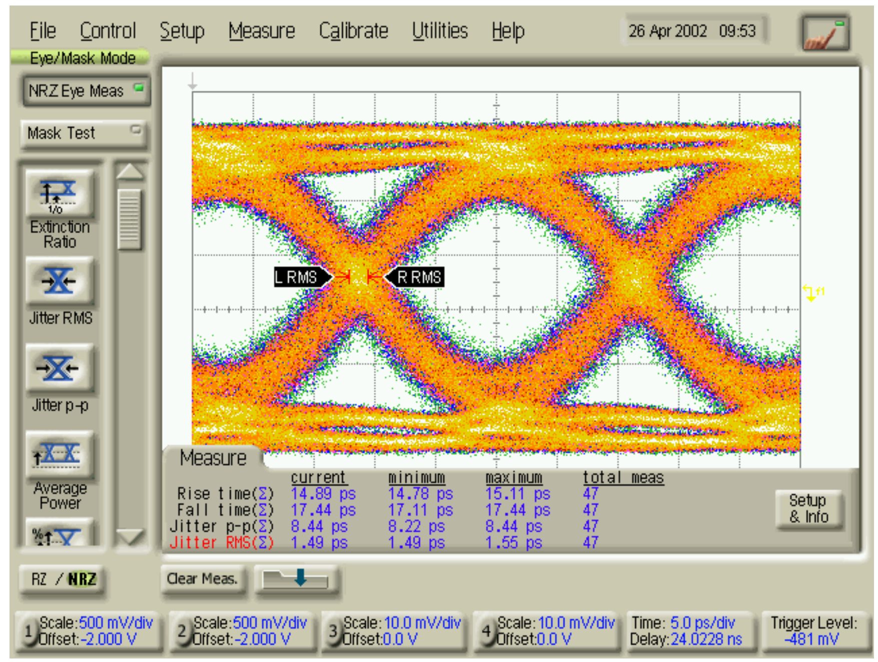


Nominal eye-diagrams

40 Gb/s



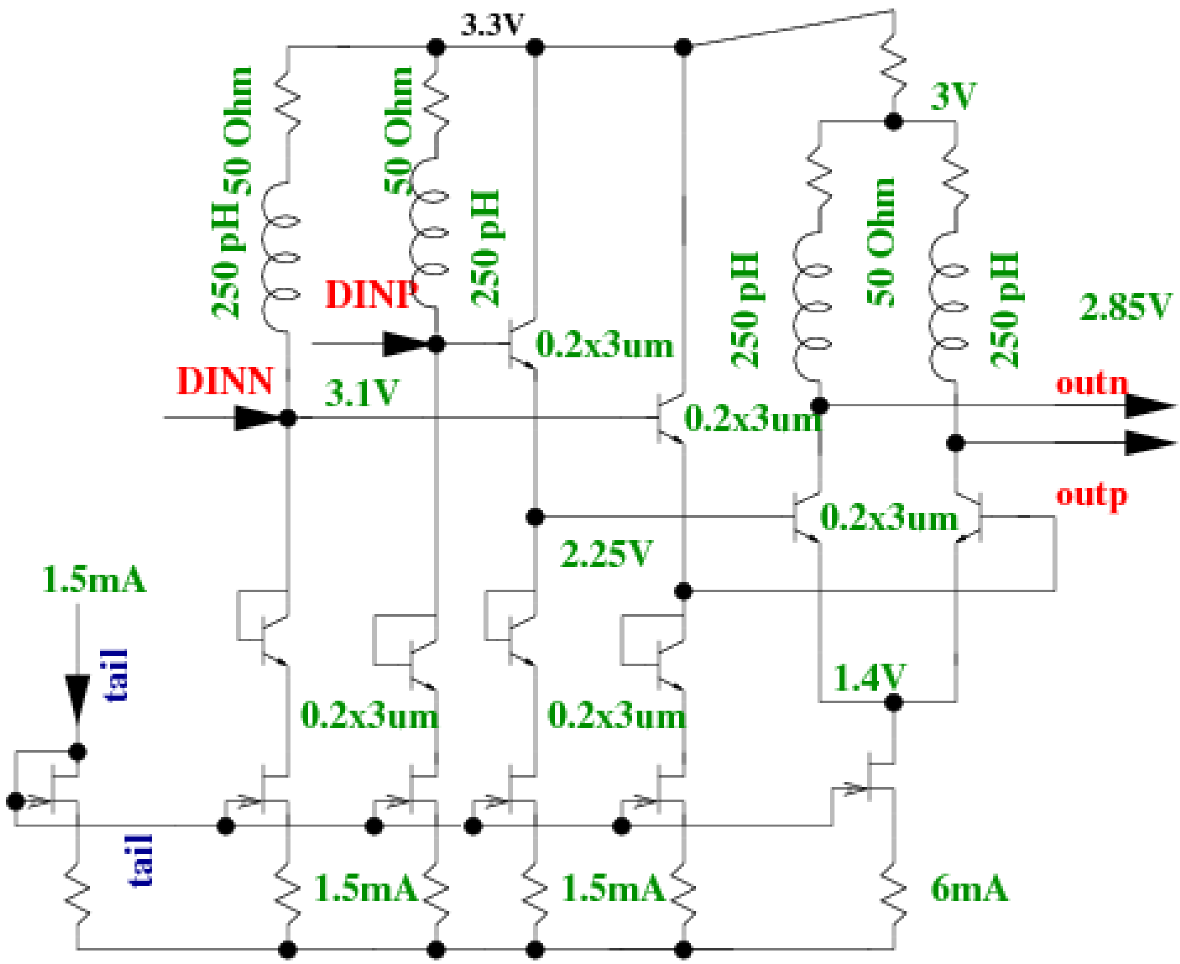
44 Gb/s



- Output swing of 3.0 V_{p-p} per side
- Rise/fall times are 10.9/11.4 ps
- Jitter is 8.6 ps (peak to peak)

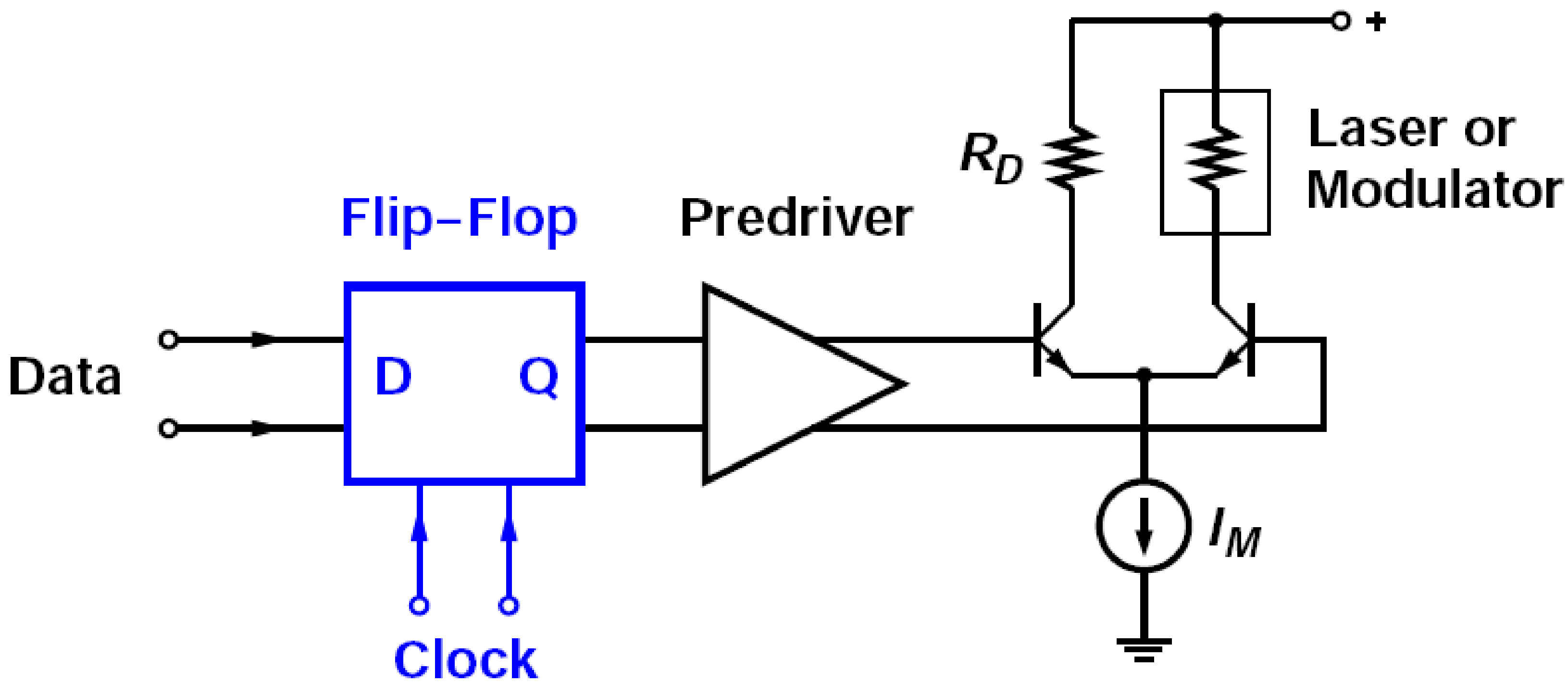
Pre-driver

SiGe BiCMOS input buffer example



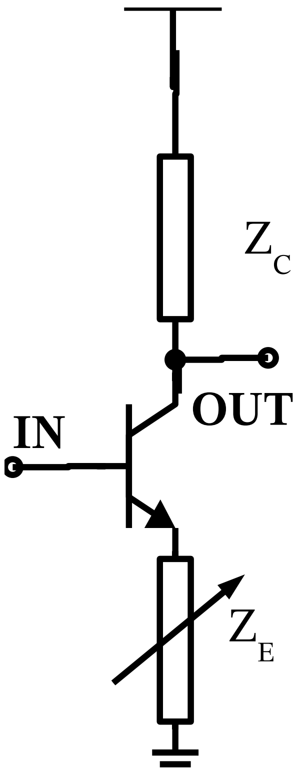
Total current = 9mA, Power = 30mW

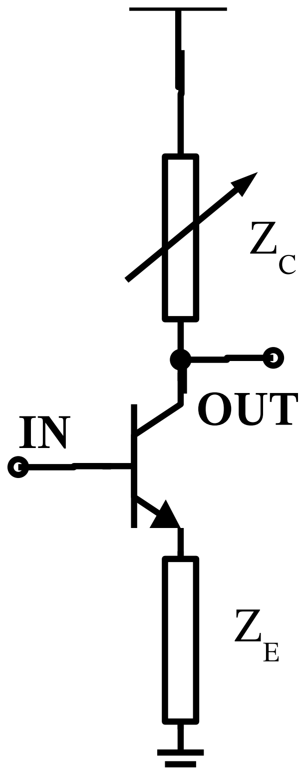
Optional retimer

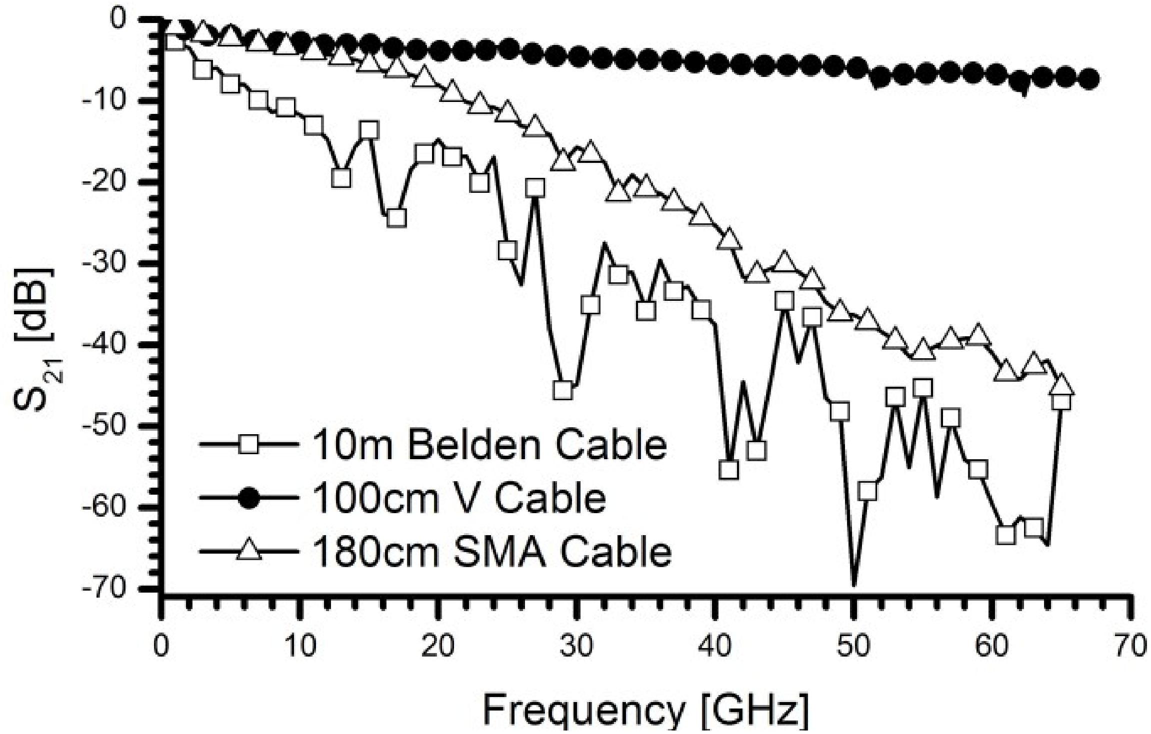


[2]

Receiver linear pre-emphasis concept for cable equalizers



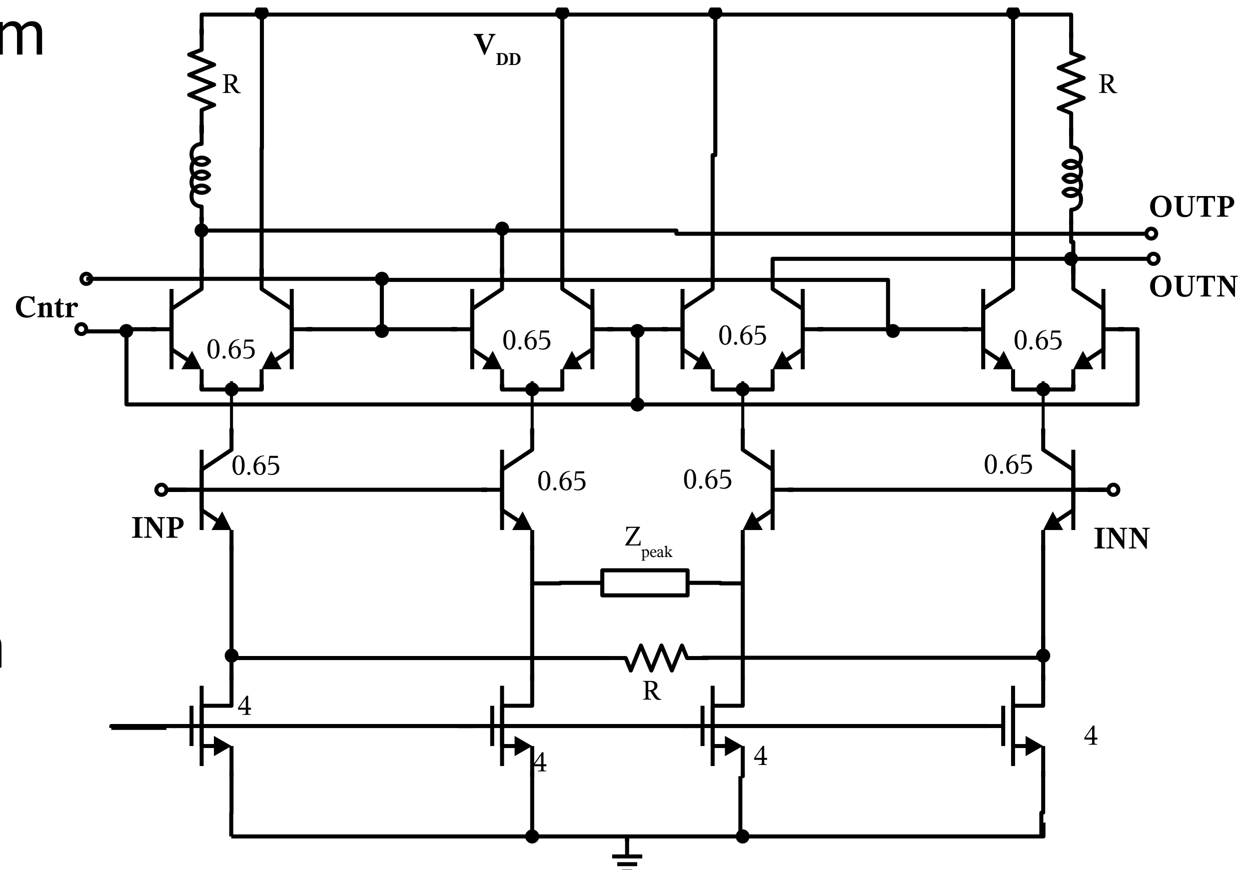




Gilbert-cell based driver pre-emphasis

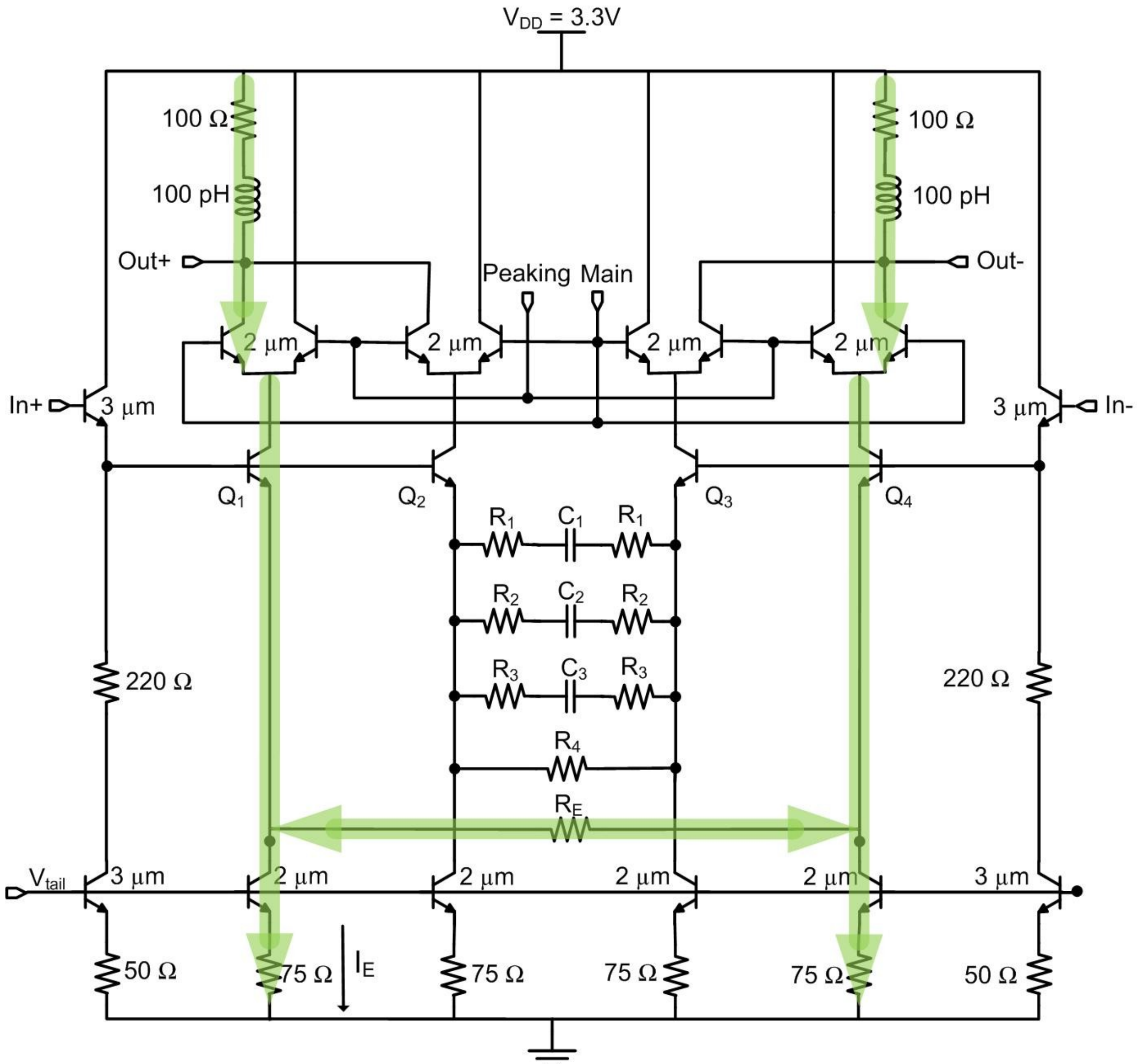
Summing outputs from

- a stage with constant gain vs. freq
- a stage with peaking gain (with capacitive degeneration)



•H. Shakiba, Gennum, ISSCC-1999
•2.5Gb/s cable equalizer

Low-frequency path



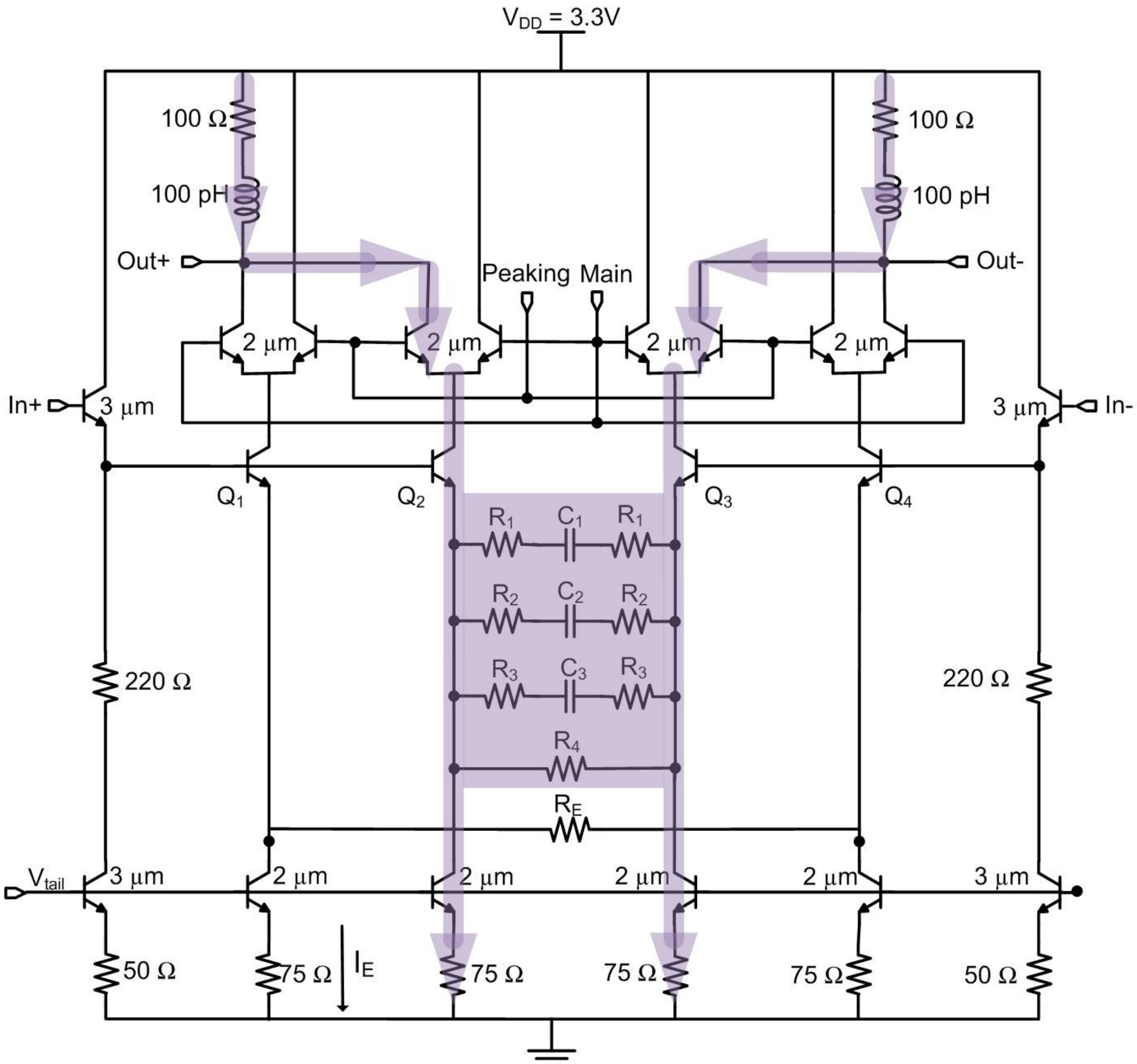
$$i_1 = \frac{g_m}{(Z_{CS} \parallel \frac{R_E}{2})g_m + 1} v_i$$

$$i_2 = \frac{g_m}{(Z_{CS} \parallel \frac{Z_E}{2})g_m + 1} v_i$$

$$v_o = -[\beta i_1 + (1-\beta) i_2] Z_L$$

A. Balteanu, BCTM 2009

High-frequency path



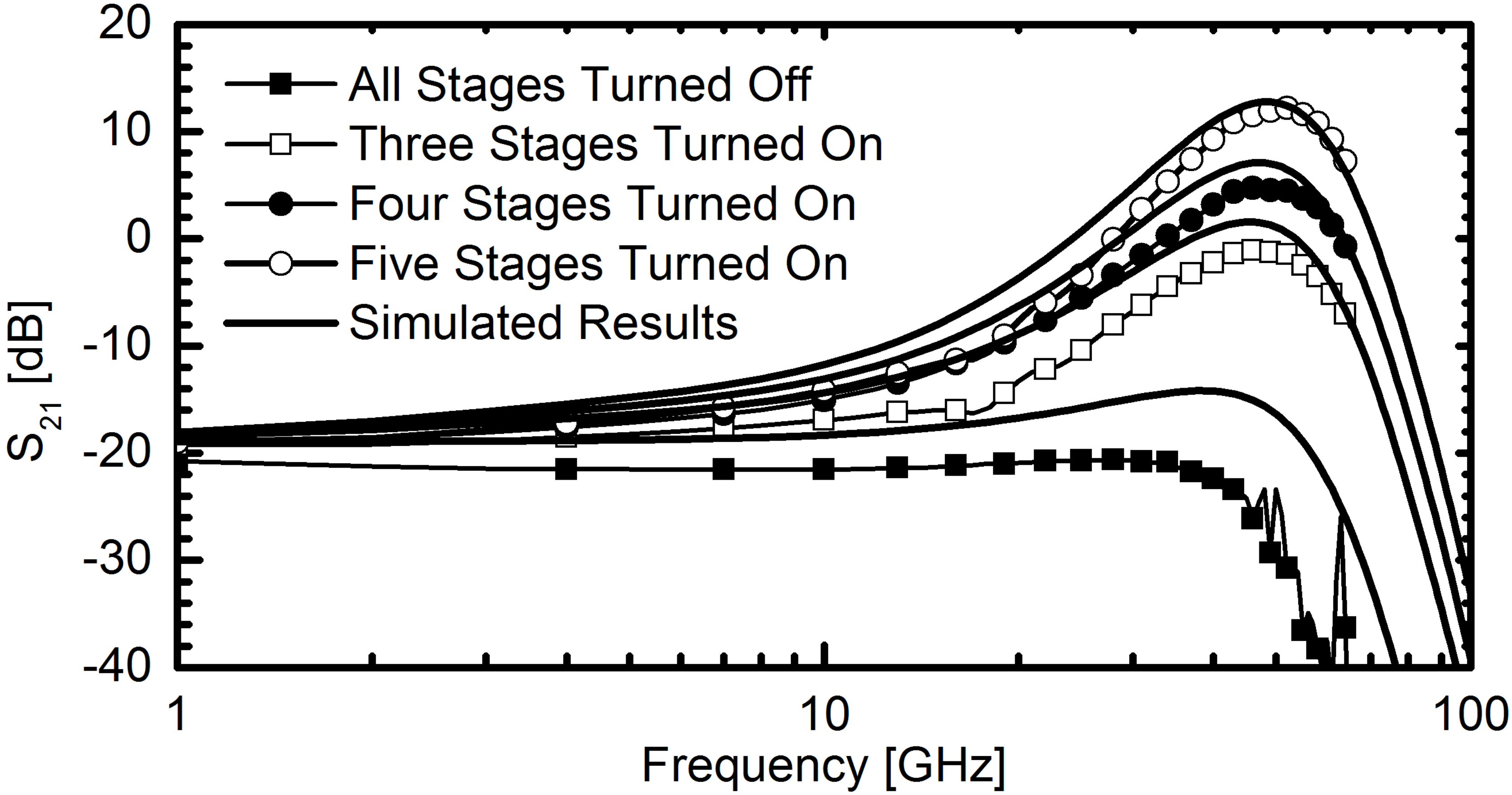
$$i_1 = \frac{g_m}{(Z_{CS} \parallel \frac{R_E}{2})g_m + 1} v_i$$

$$i_2 = \frac{g_m}{(Z_{CS} \parallel \frac{Z_E}{2})g_m + 1} v_i$$

$$v_o = -[\beta i_1 + (1-\beta) i_2] Z_L$$

A. Balteanu, BCTM 2009

Compensates for cable loss vs. freq.



A. Balteanu, BCTM 2009

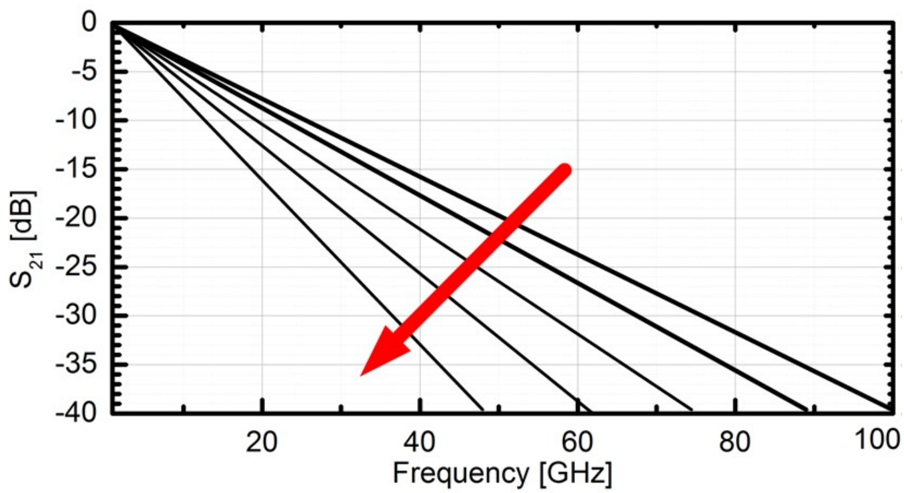
Examples of 40+Gb/s equalizers, drivers and DACs with waveshape control

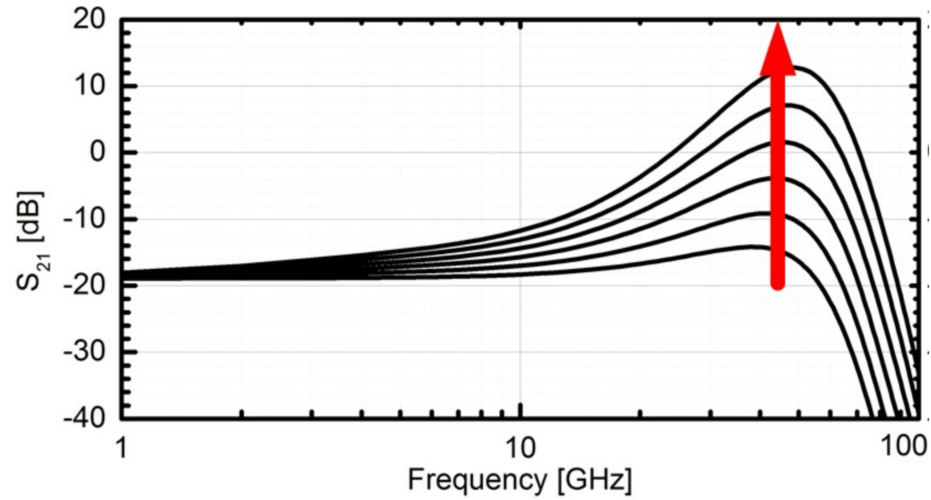
A 1.8V SiGe BiCMOS Cable Equalizer with 40-dB Peaking Control up to 60 GHz

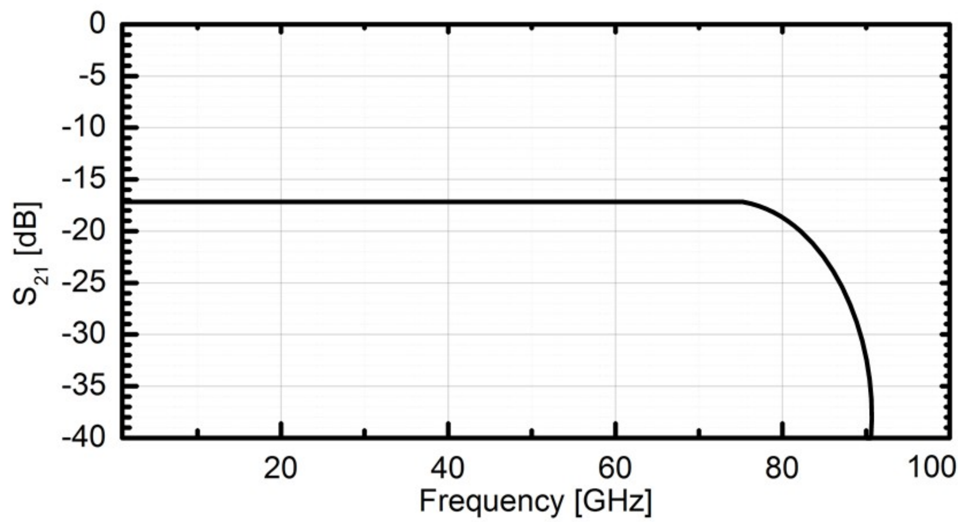
Ioannis Sarkas and Sorin Voinigescu

CSICS 2012

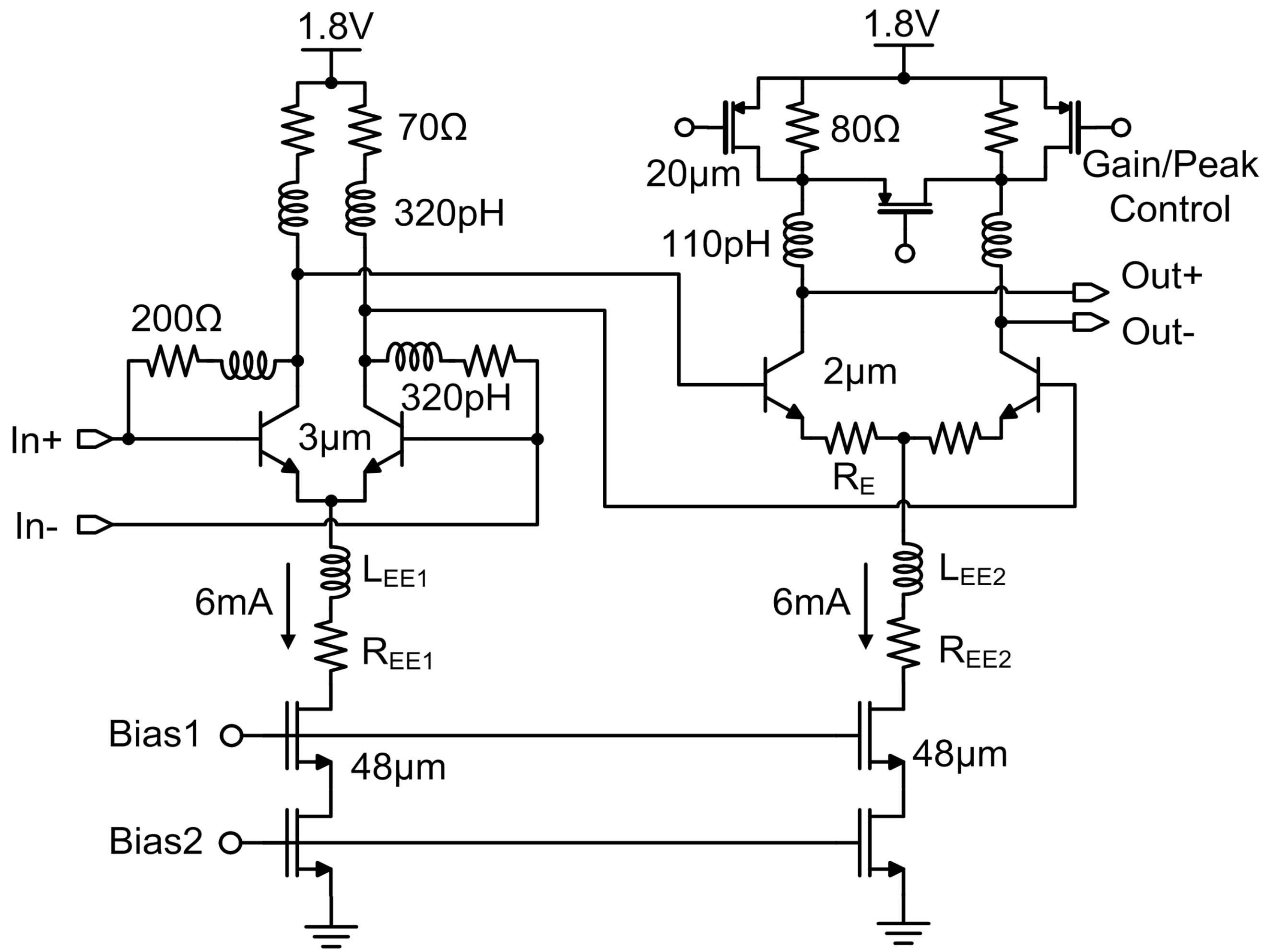
Continuous Time Linear Equalizers

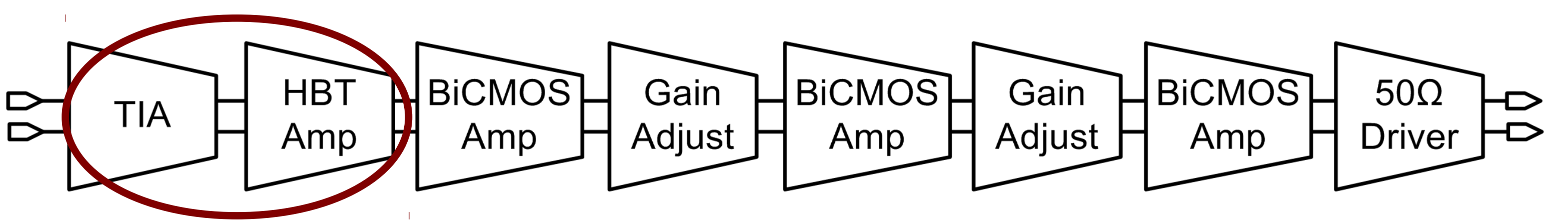




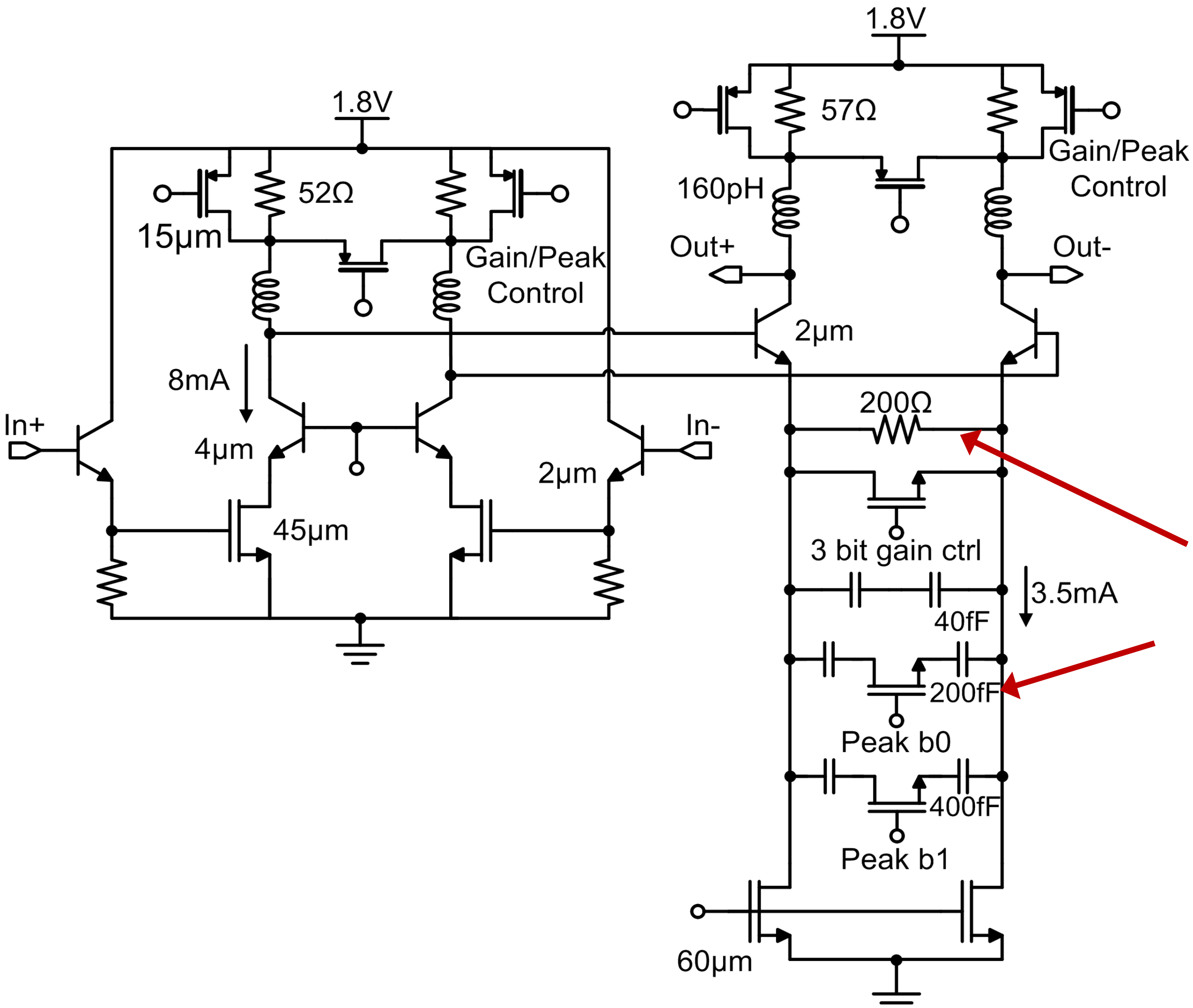


First Two Stages



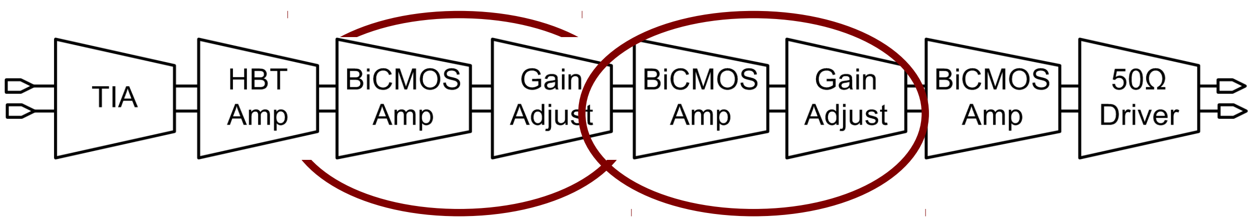


Middle Stages

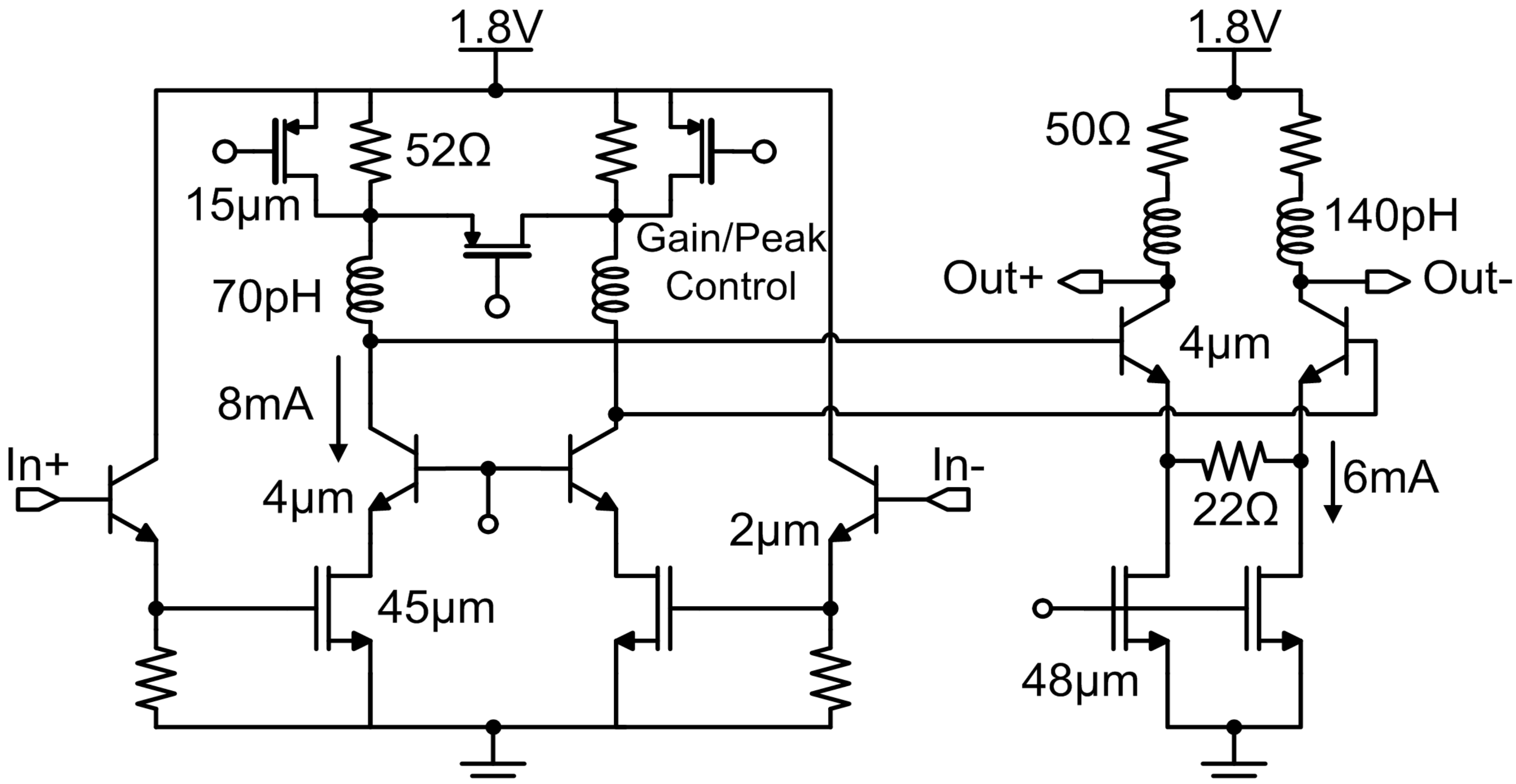


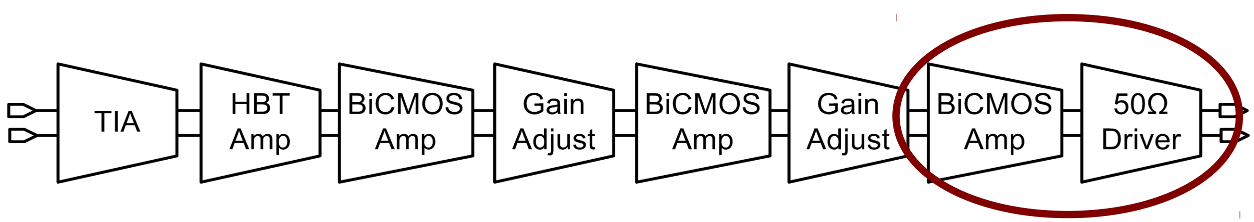
Adjustable DC gain also Important for linearity

Adjustable zero frequency



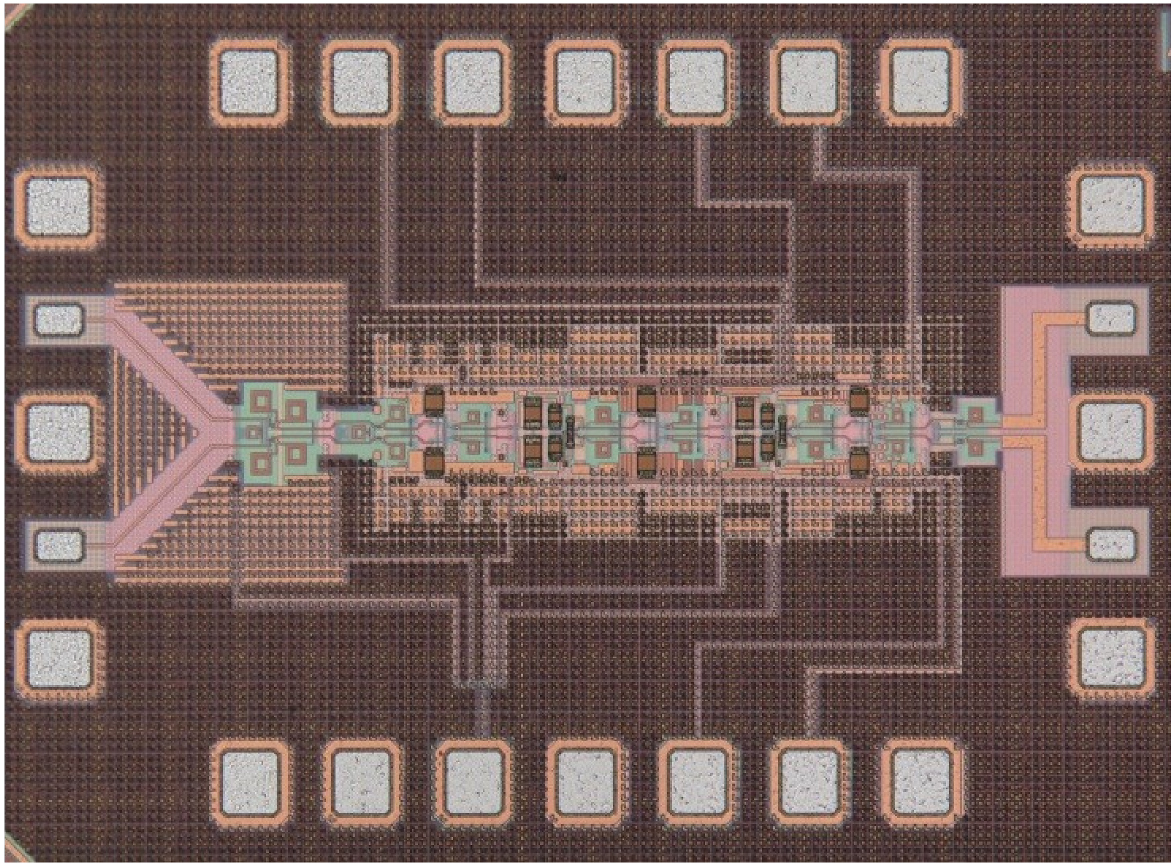
Output Driver & Predriver





58

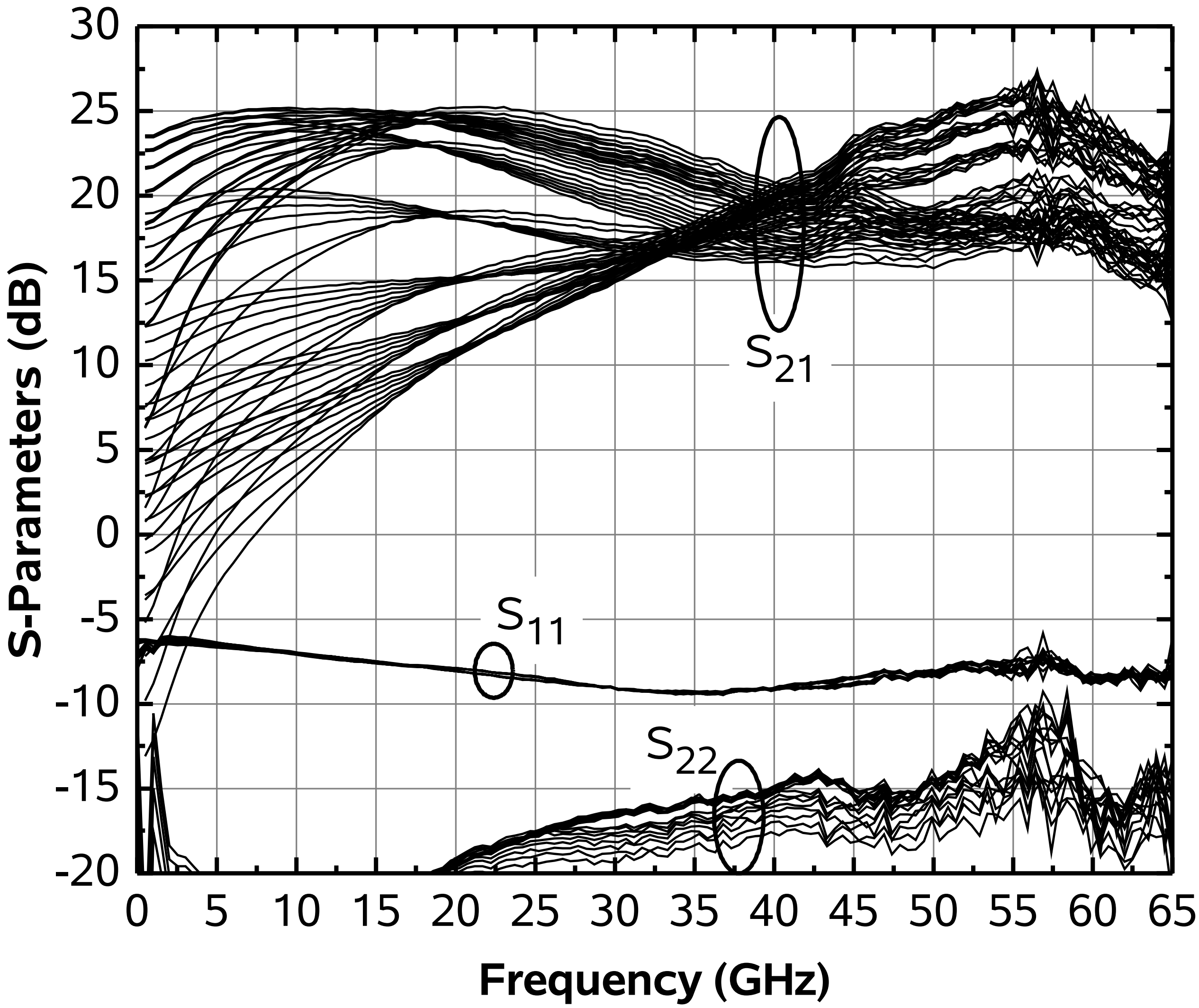
Die Photo



- STMicroelectronics' 130nm SiGe BiCMOS process with f_T / f_{MAX} =220/280 GHz
- 1×0.7mm P_{DC} = 250mW

59

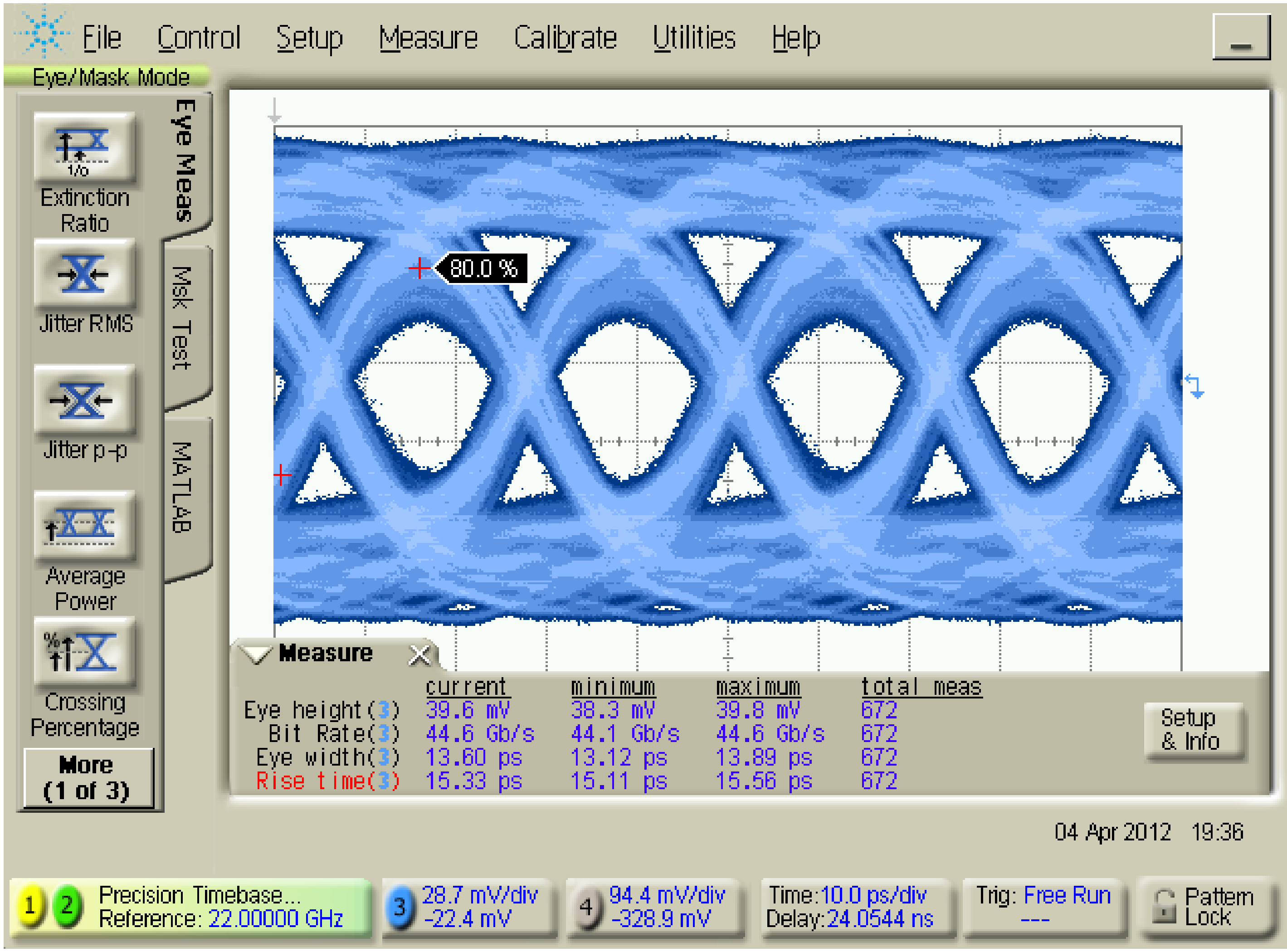
Equalizer S-parameters



Bits grouped:

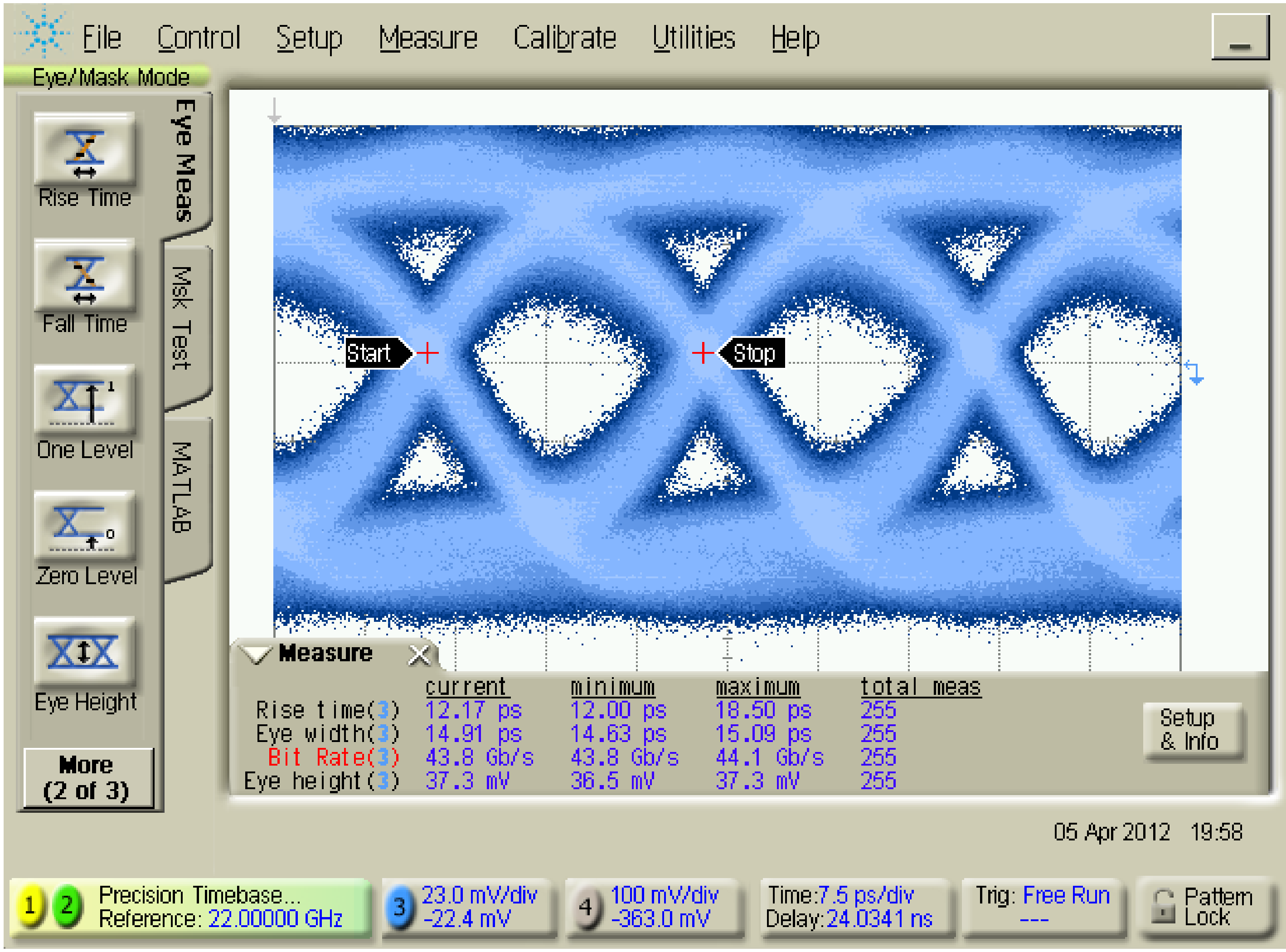
- 3 gain
- 2 peaking
- 1 gain-inductive peaking

6.1m Cable – 44-Gb/s Equalized Eye



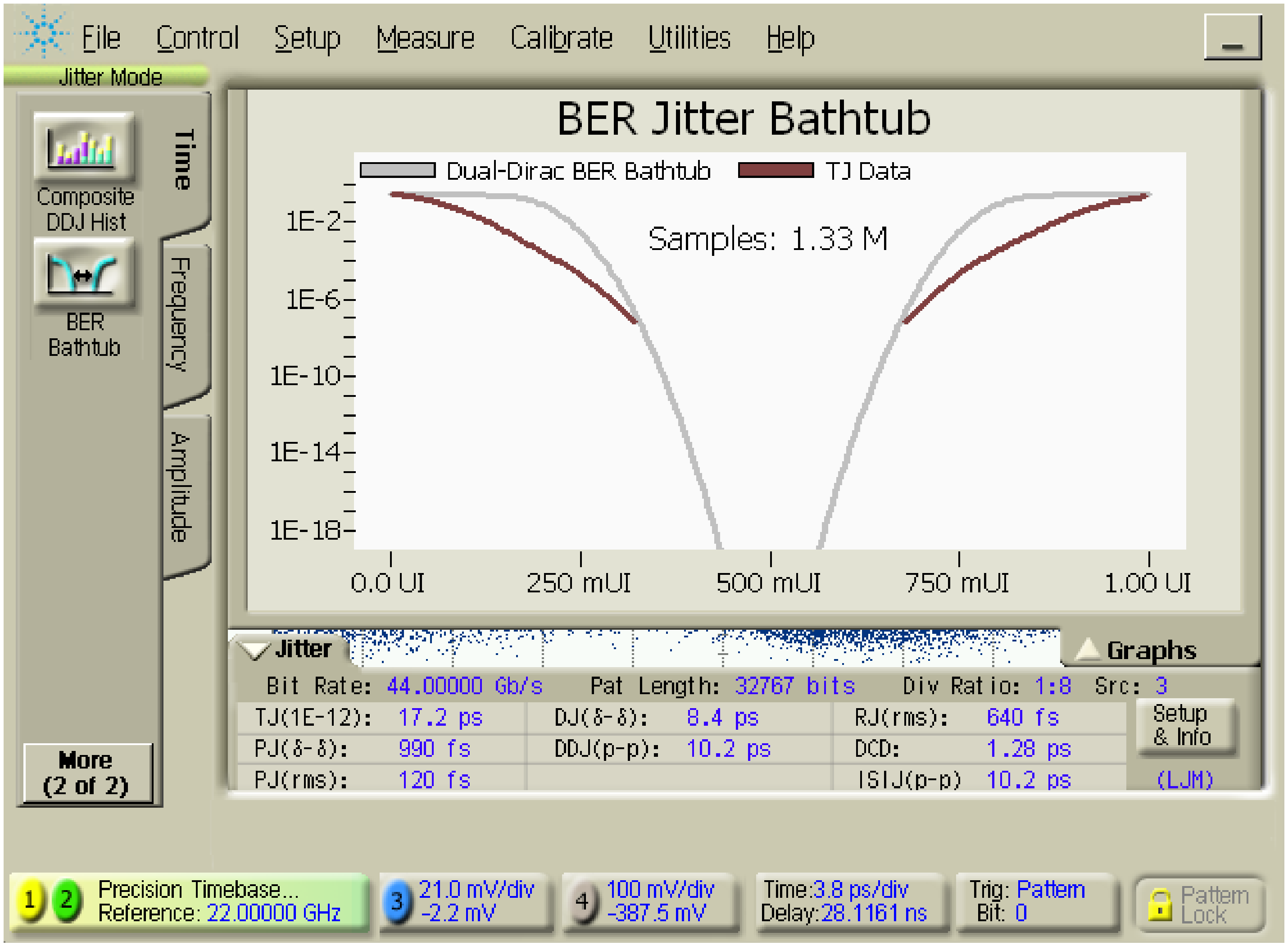
2^7-1 length

6.1m Cable – 44-Gb/s Equalized Eye



2^{31}-1 length

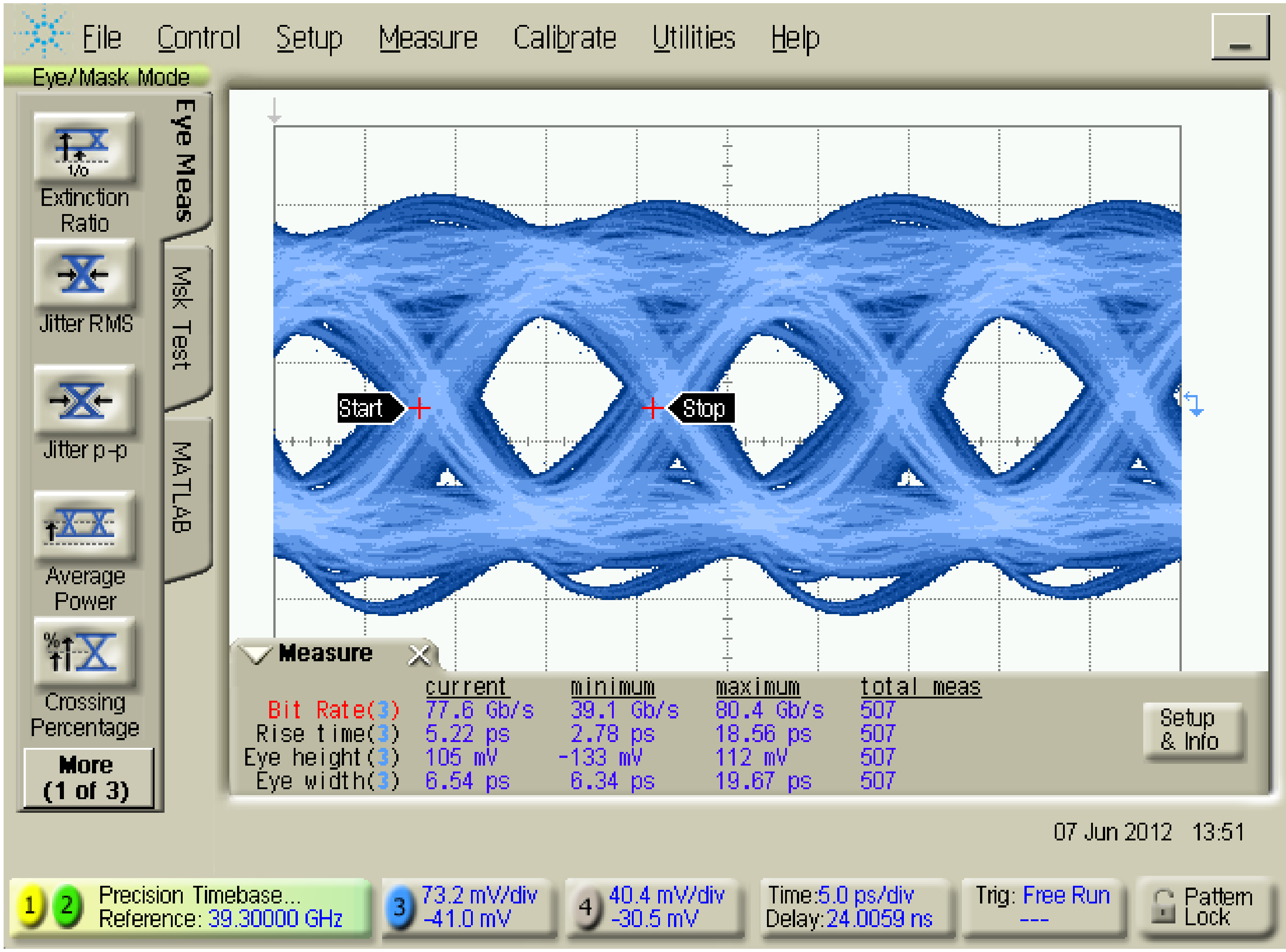
6.1m Cable – 44-Gb/s Bathtub



2^{15}-1 length

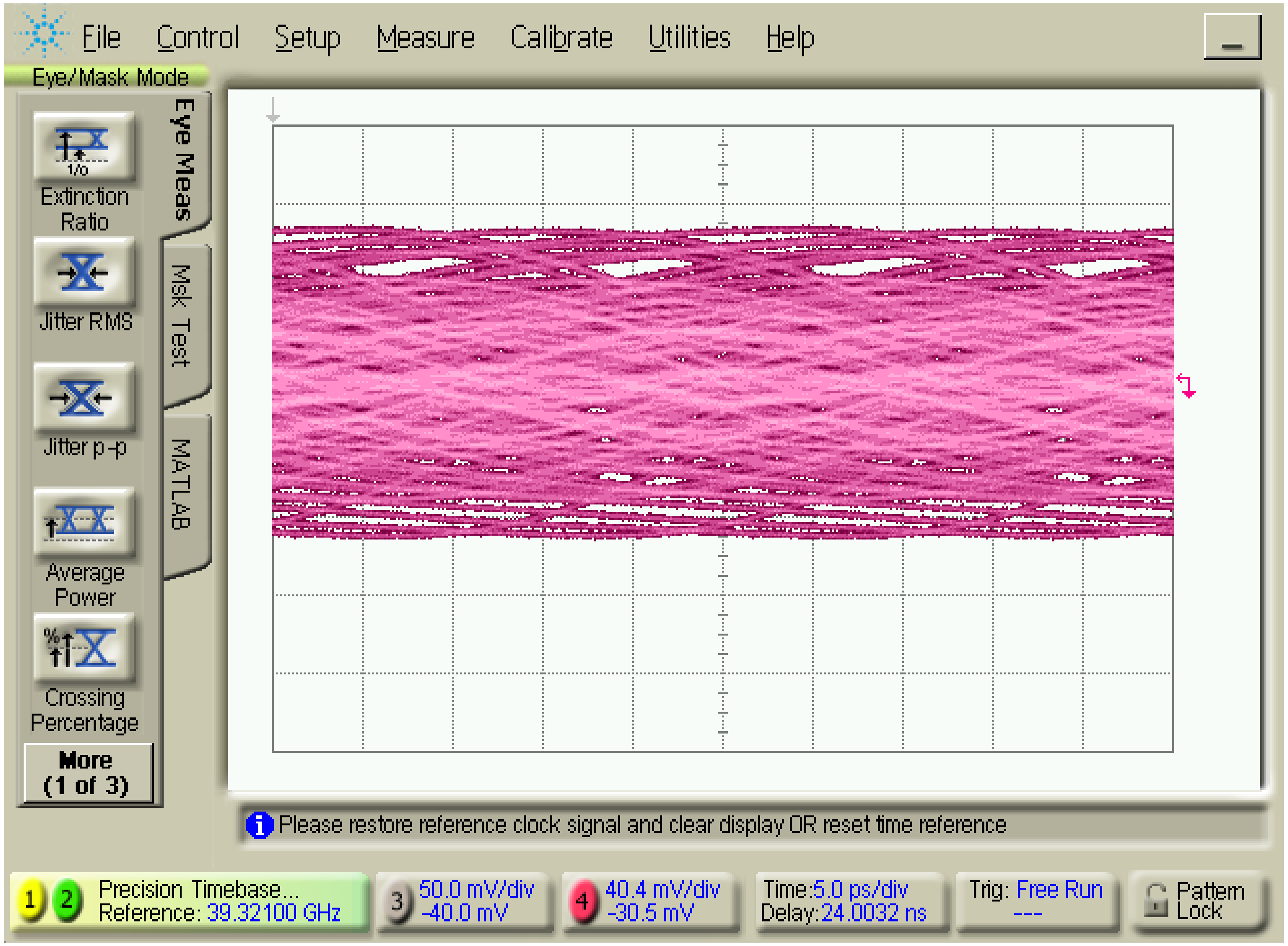
Setup for Cable Equalization @ 80Gb/s

80-Gb/s PRBS Output



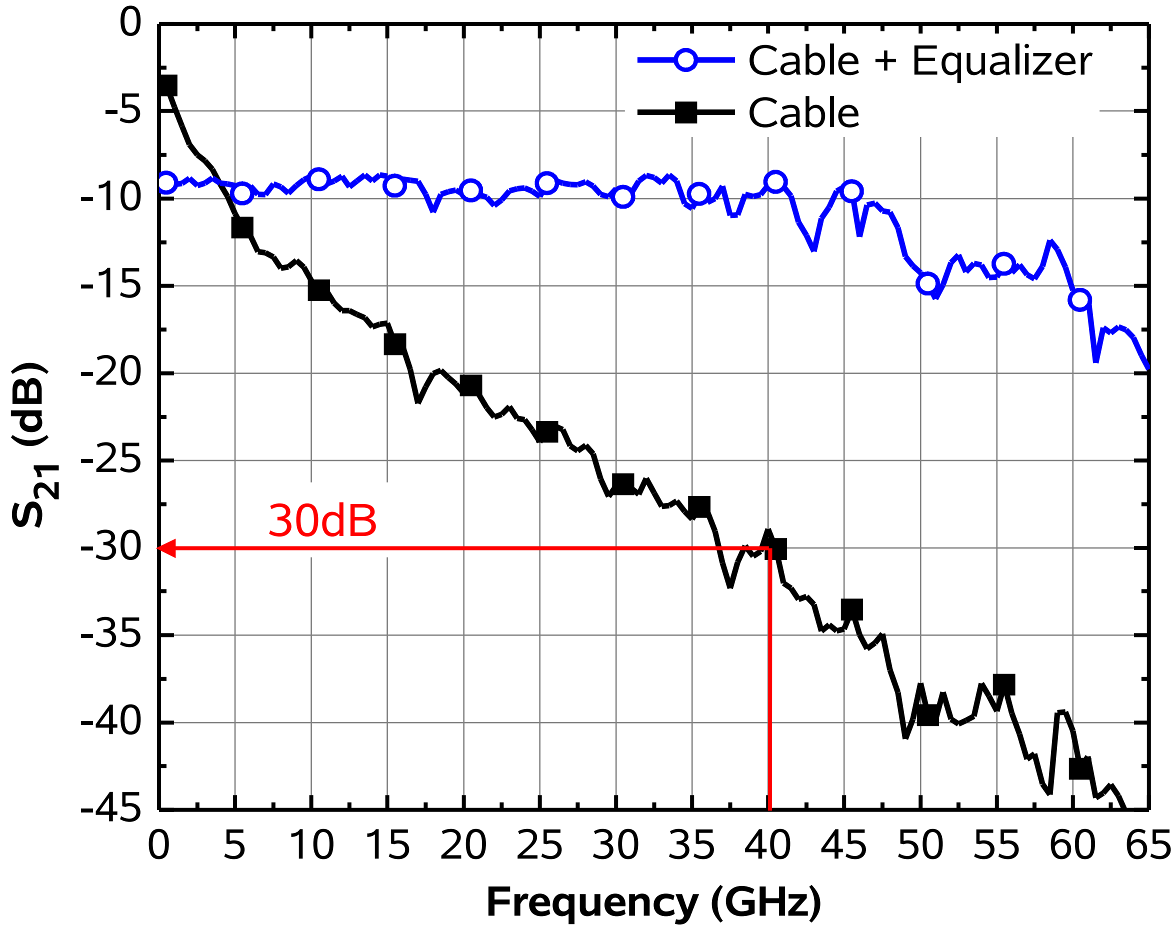
2^7-1 length

2.7m Output Eyes



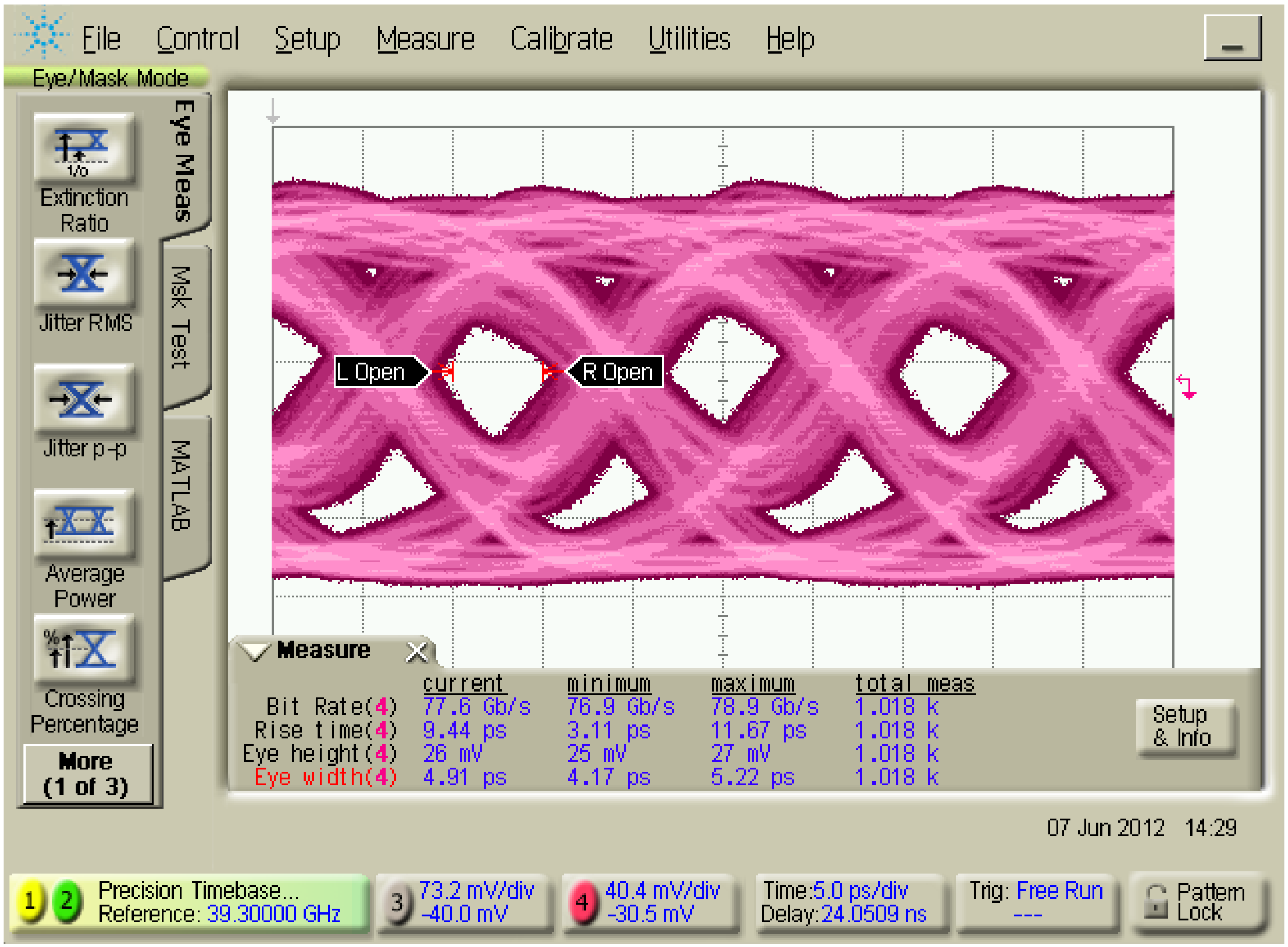
2^7-1 length

3.9m Cable Equalized S-parameters

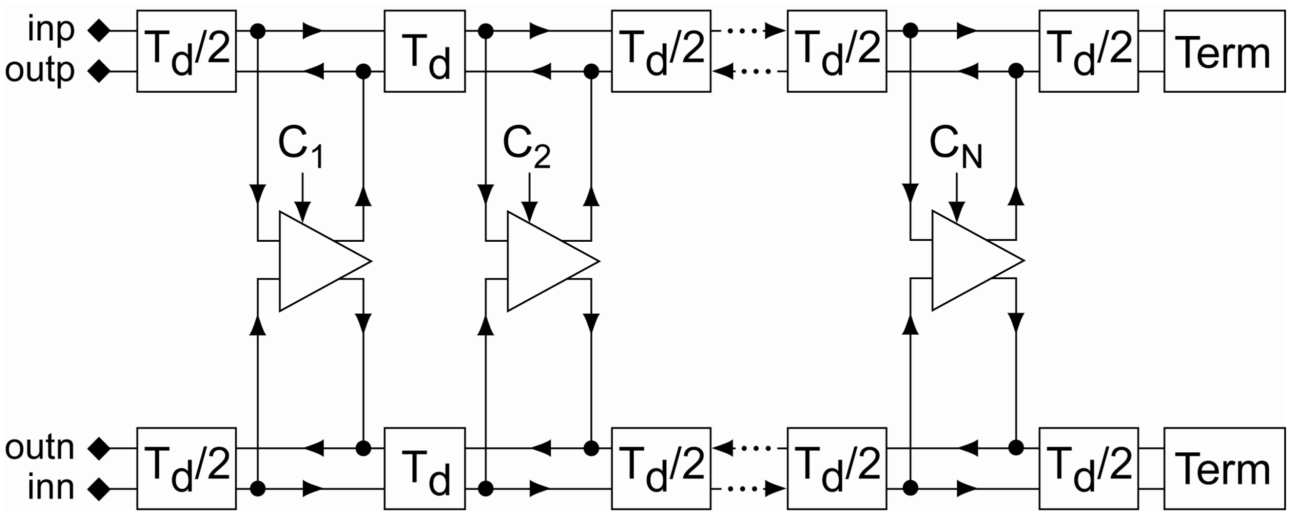


- 30dB loss @ 40GHz
- BW = 50GHz after equalization

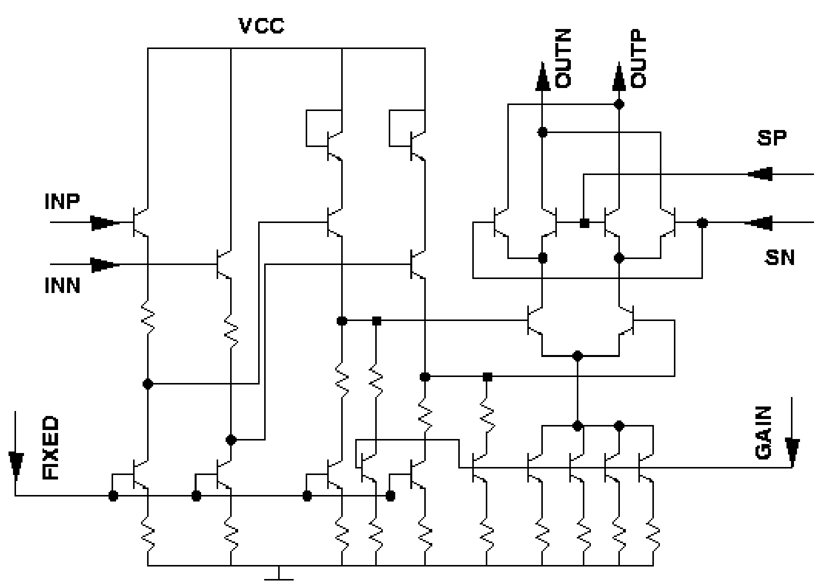
3.9m Cable – Equalized Eye



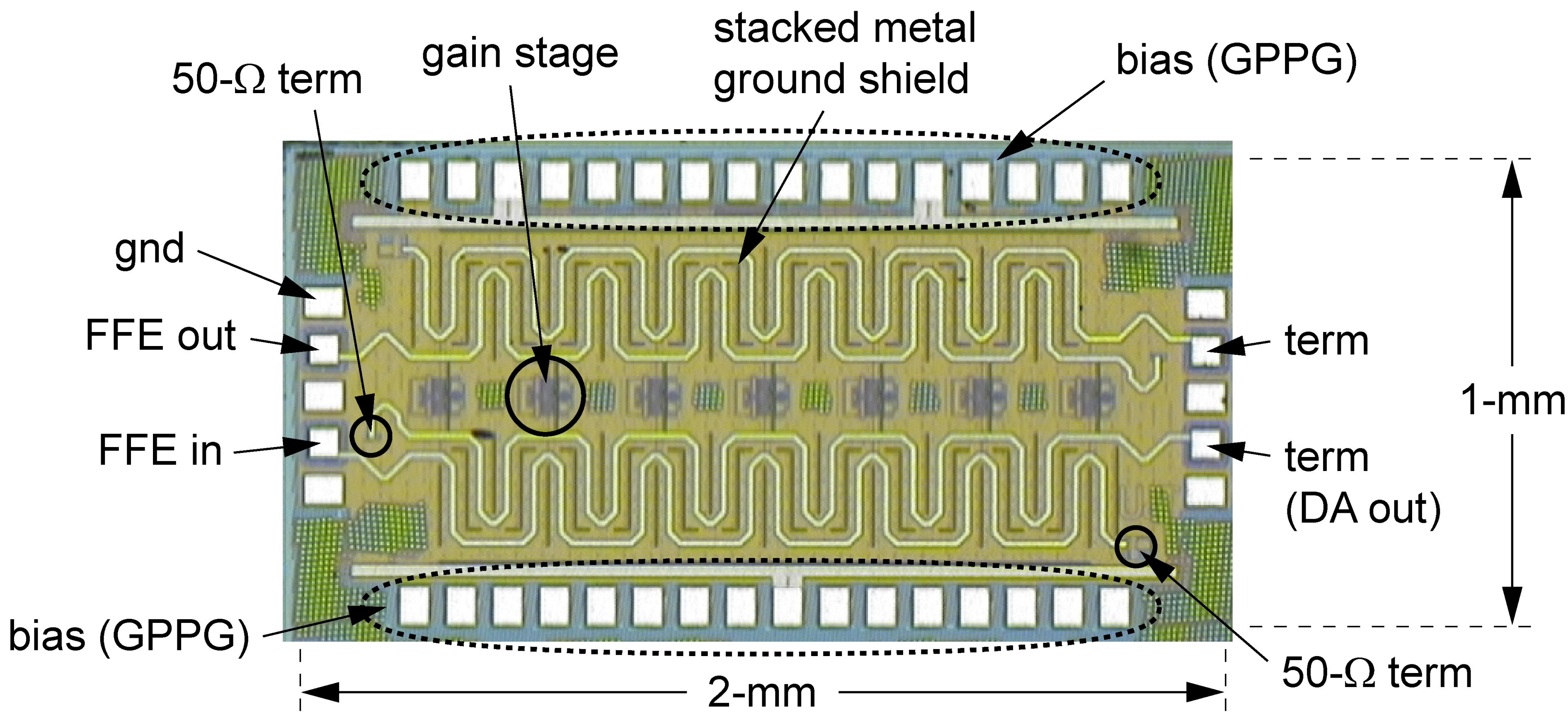
Distributed 49-Gb/s equalizer in 0.18μm SiGe BiCMOS



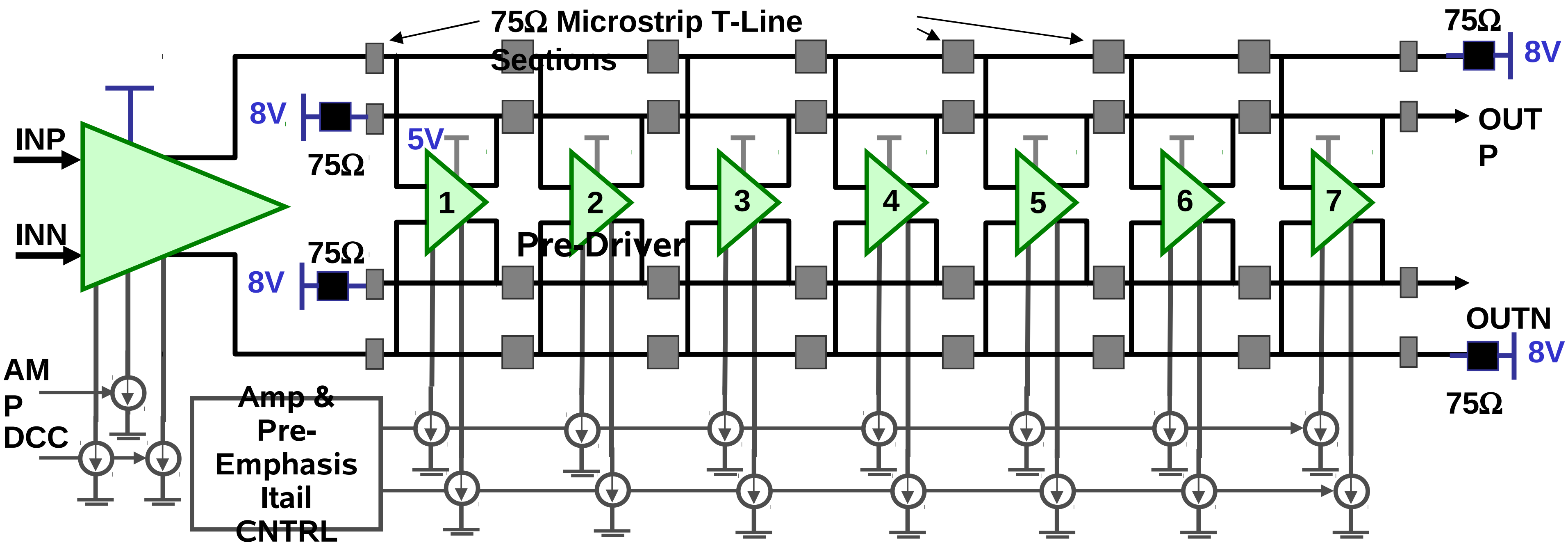
A. Hazneci CSICS-2004



SiGe BiCMOS distributed amplifier/equalizer layout

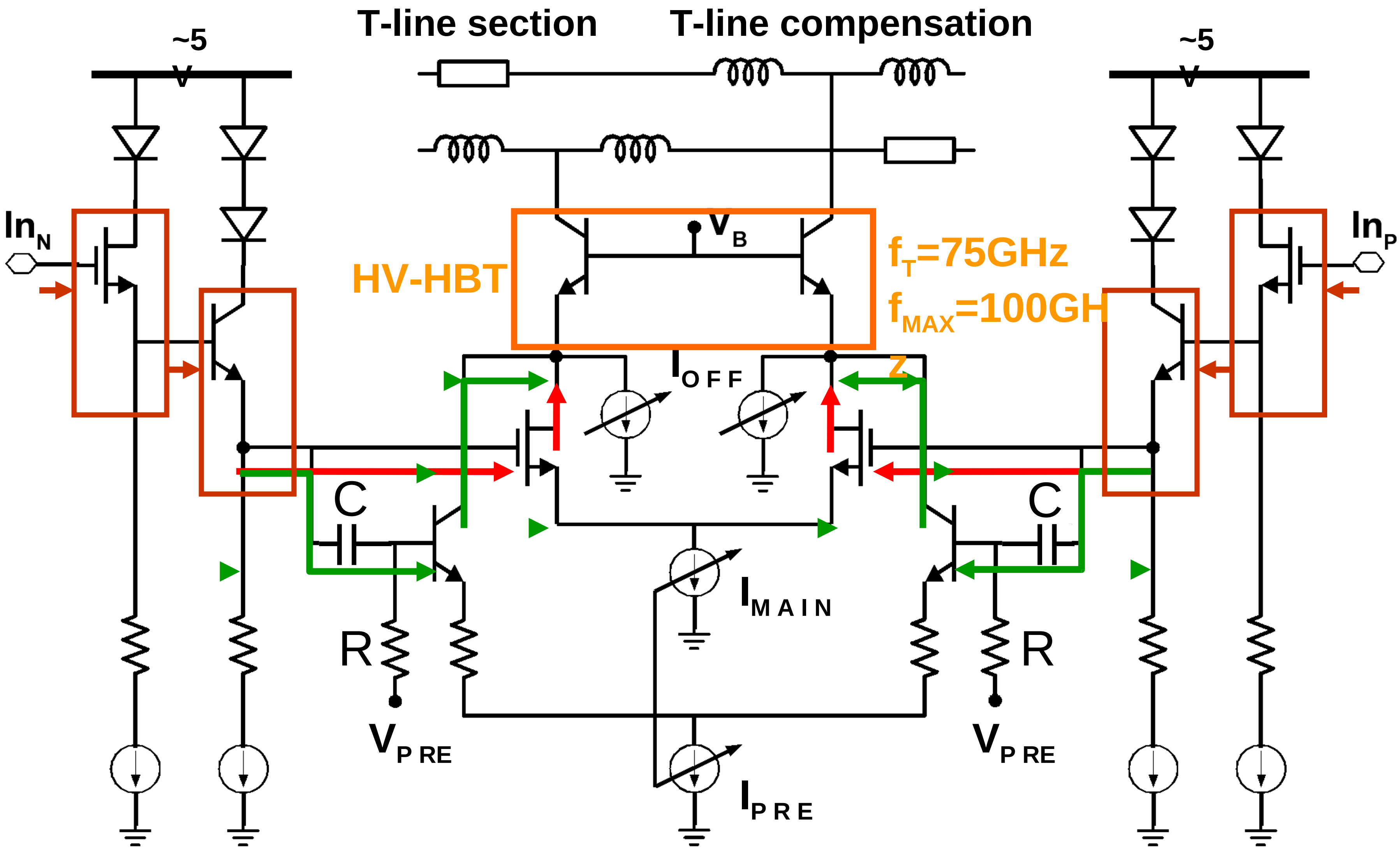


40-Gb/s Distributed Cable Driver with Pre-emphasis Control (R.Aroca, CSICS-2007)



- $I_{OUT} = 5V_{pp}/(75\Omega//75\Omega)$ = 133mA → 19mA/section
- Must fully switch the DA → predriver: $1.5V_{pp}$, 40mA
- Gain of predriver = 1.5/0.2 = 18dB, 3dB/stage → 6 stages
- Amplitude control is implemented in both the DA and predriver

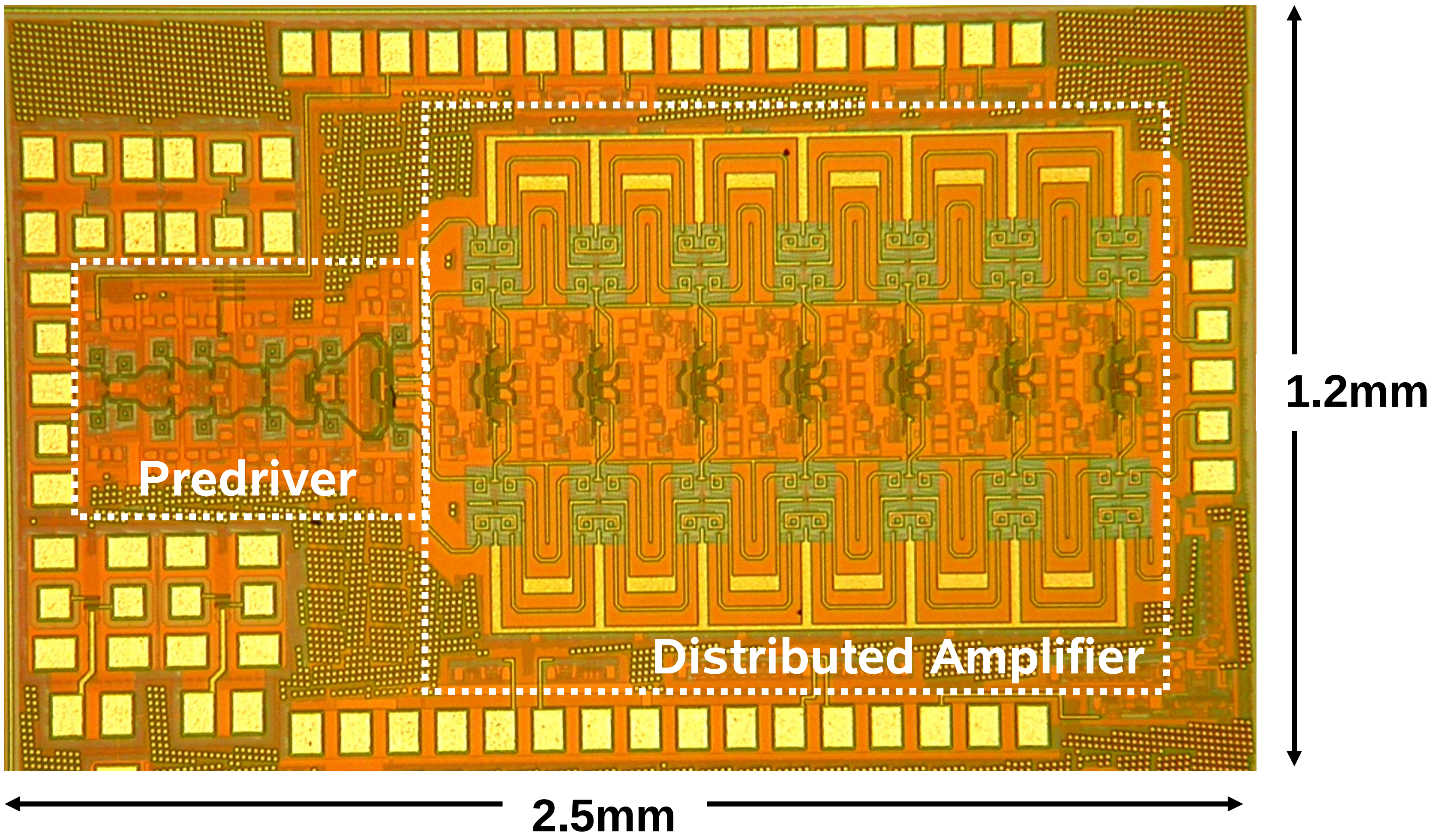
DA Section Schematic



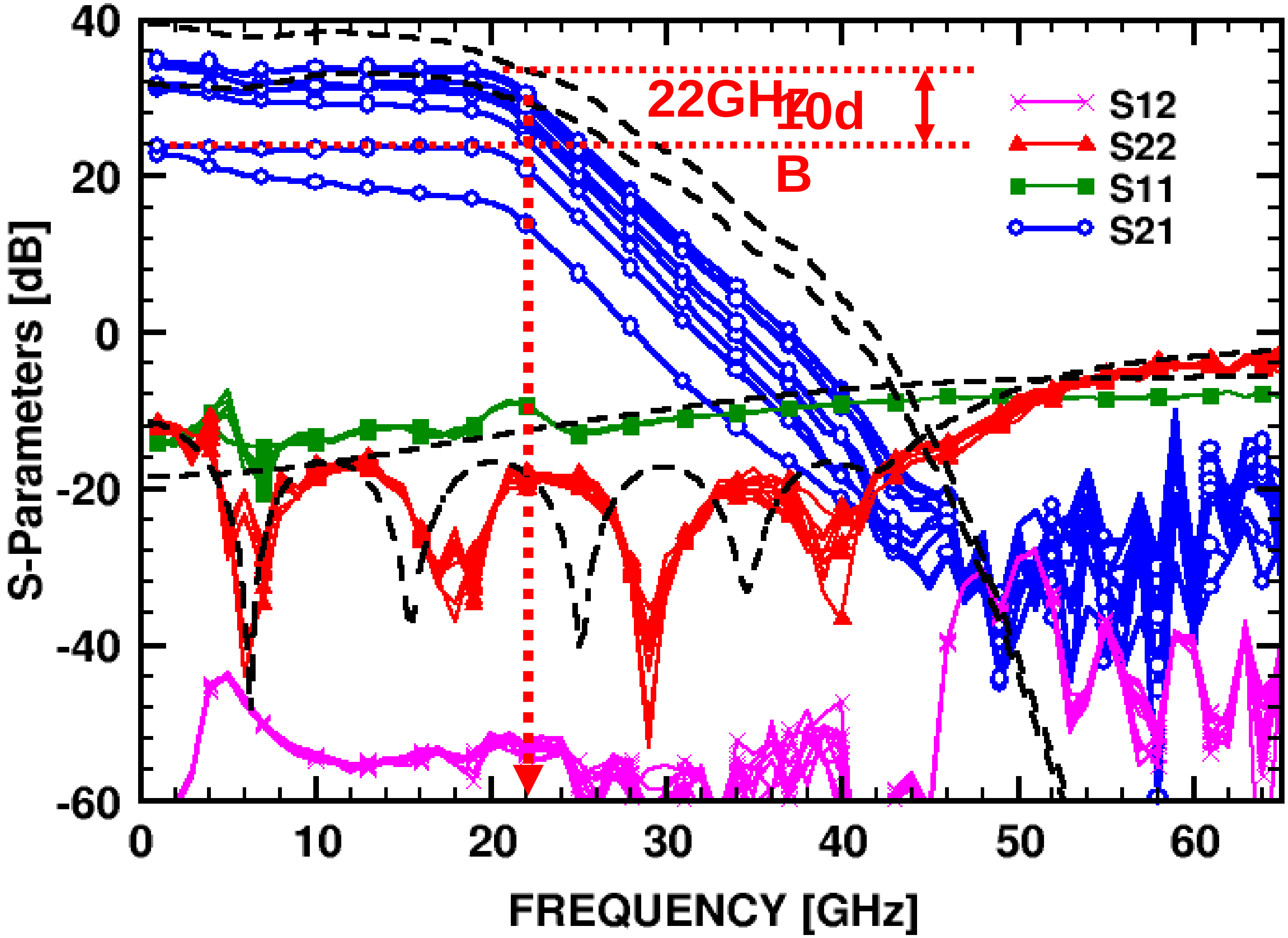
0.18µm n-MOSFETs f_T=50GHz, f_{MAX}=75GHz

RC-HPF & Digital HBT f_T=160GHz, f_{MAX}=160GHz

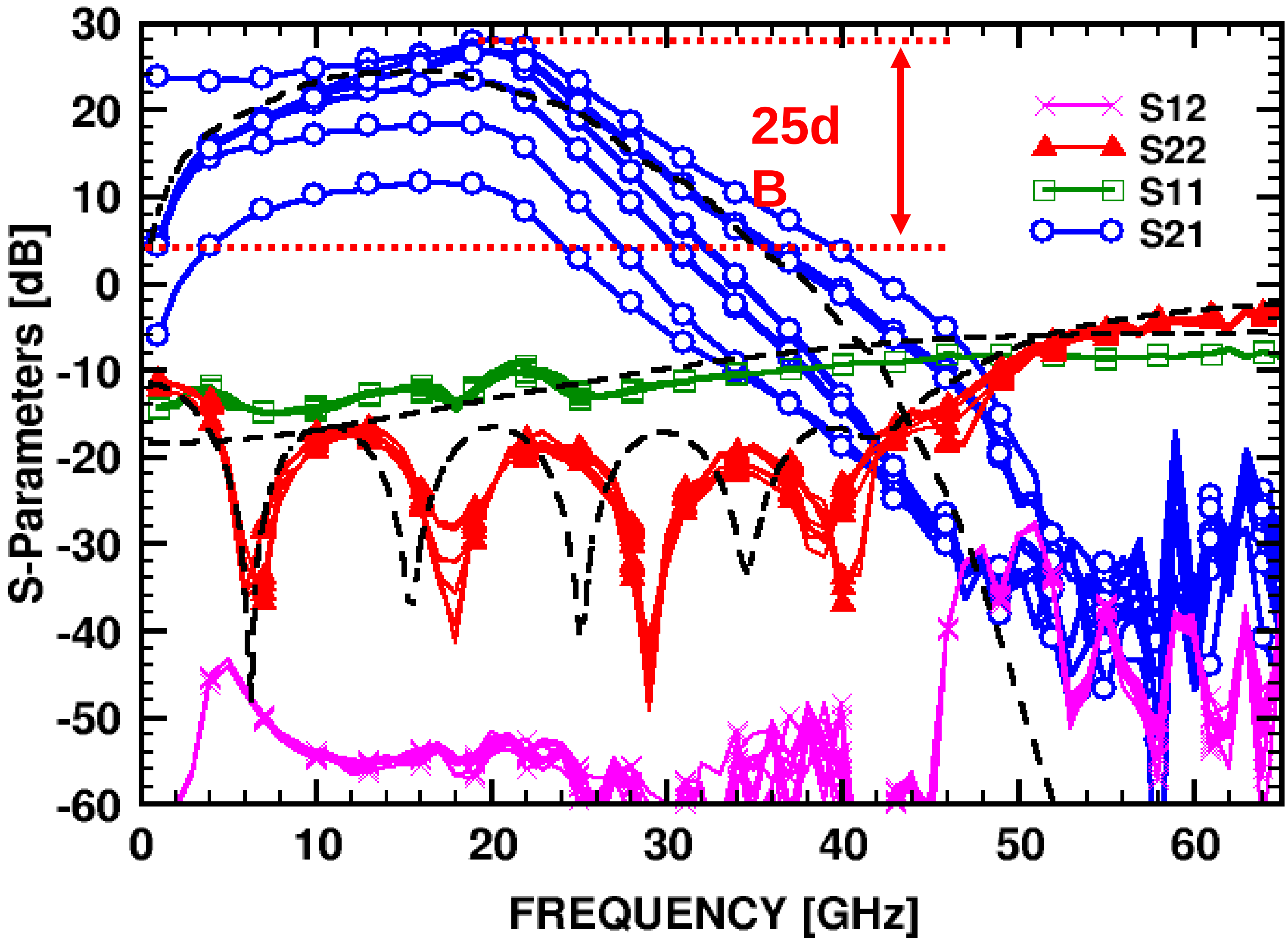
Driver Microphotograph



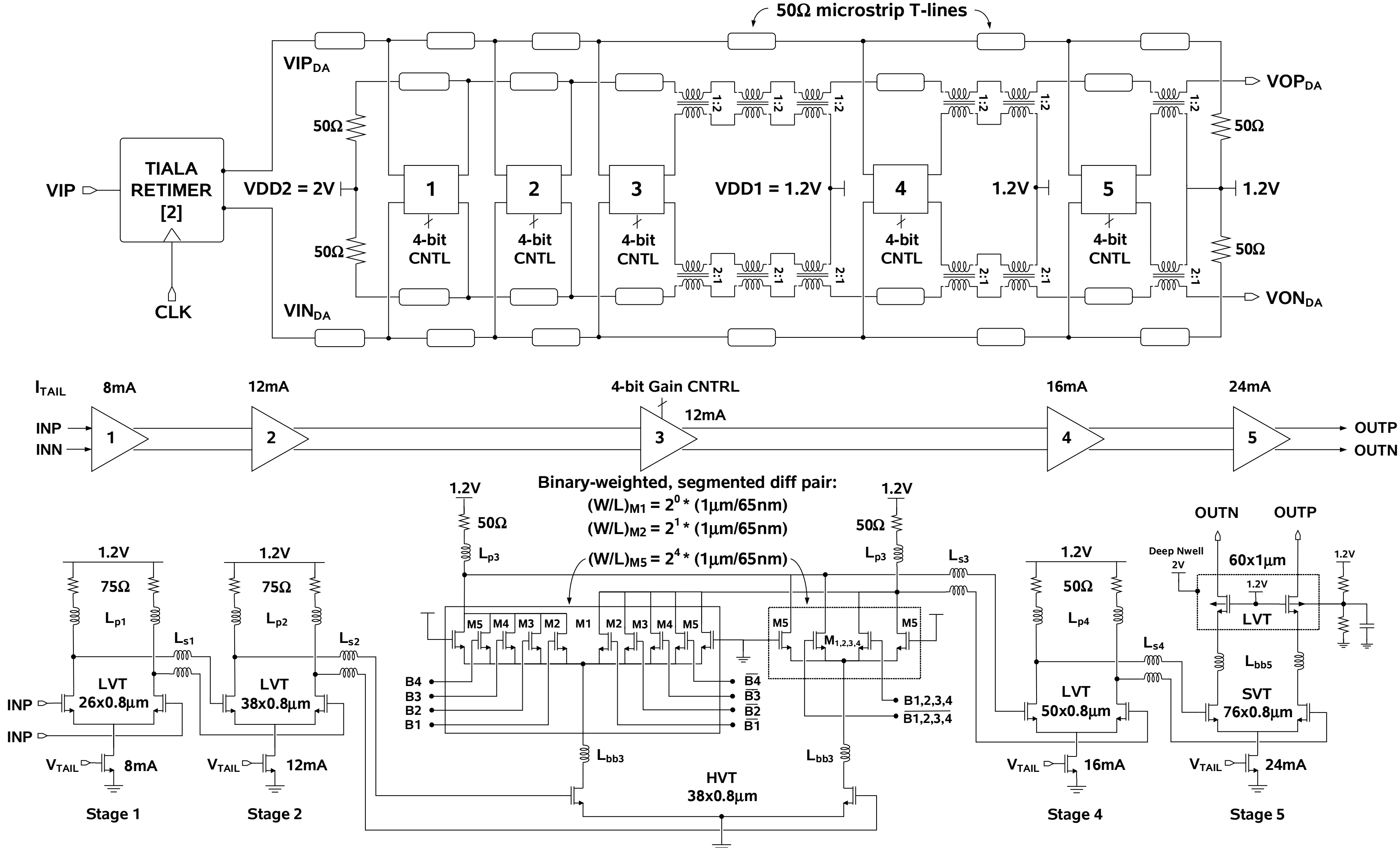
S-parameter Measurements vs. Simulations: 10dB of Amplitude Control



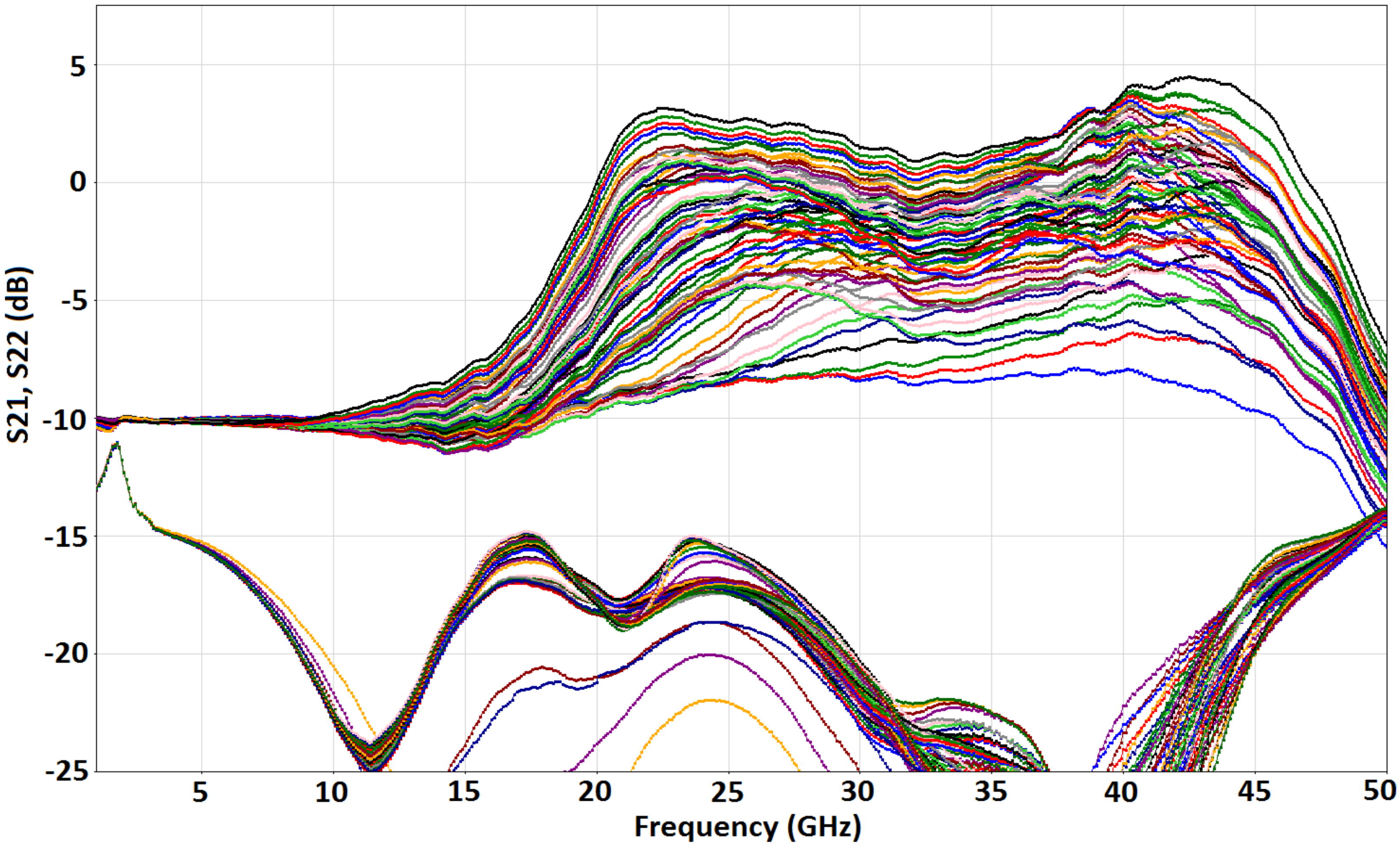
S-Parameter Measurements vs. Simulations: 25 dB of Pre-Emphasis Control



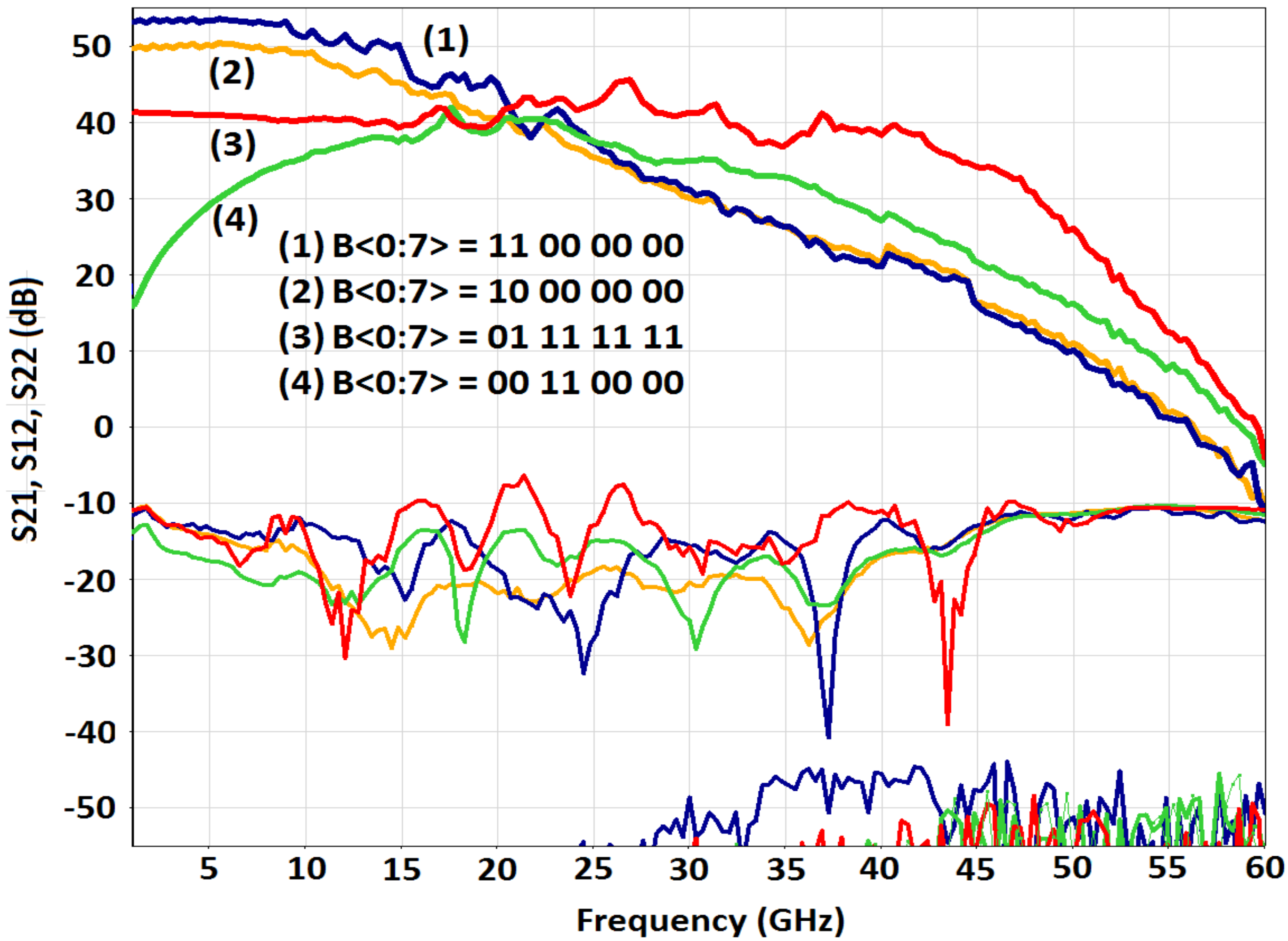
2.4Vpp, 60-Gb/s DAC-Driver in 65-nm CMOS
(R. Aroca, et al, CSICS-10)



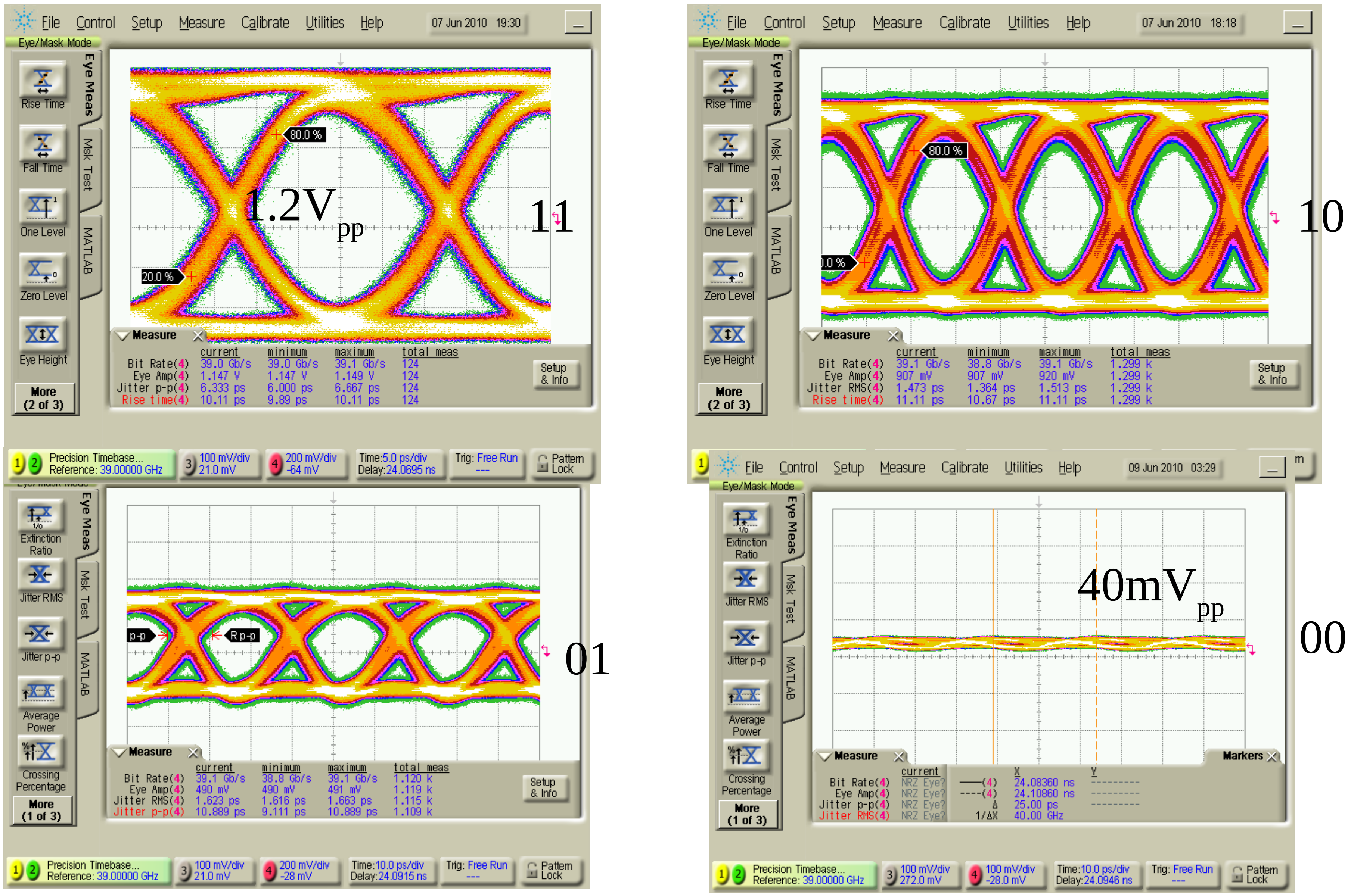
DA-only S-param meas.: all peaking states



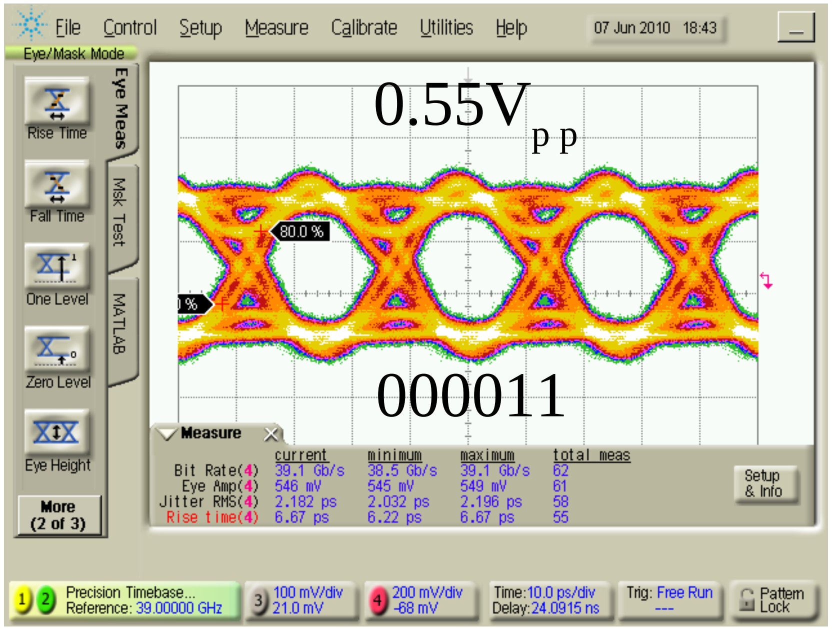
Full driver S-param measurements

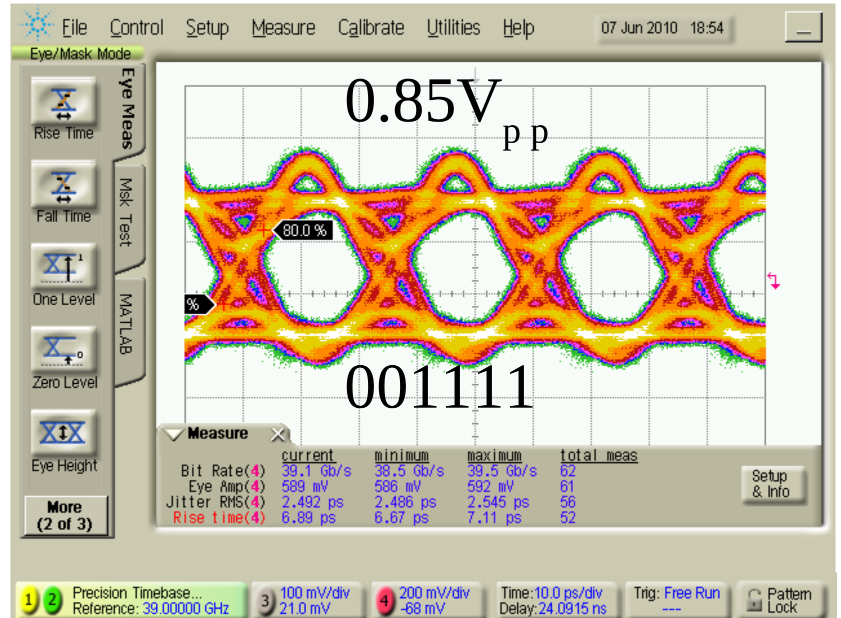


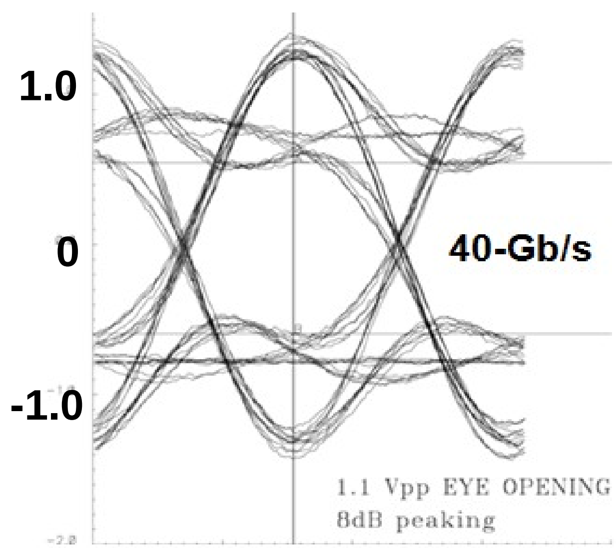
40-Gb/s eyes with ampl. cntr. DR = 30 dB

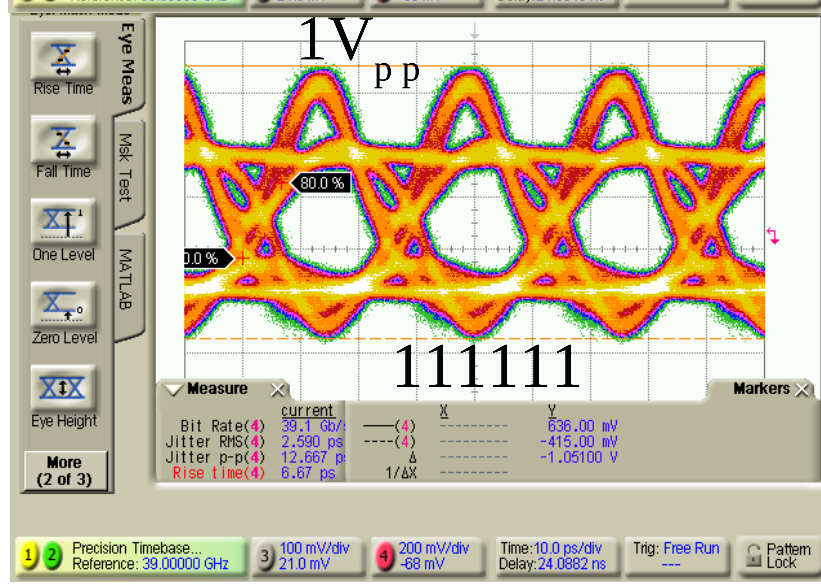


40-Gb/s eyes with peaking control: 8 dB

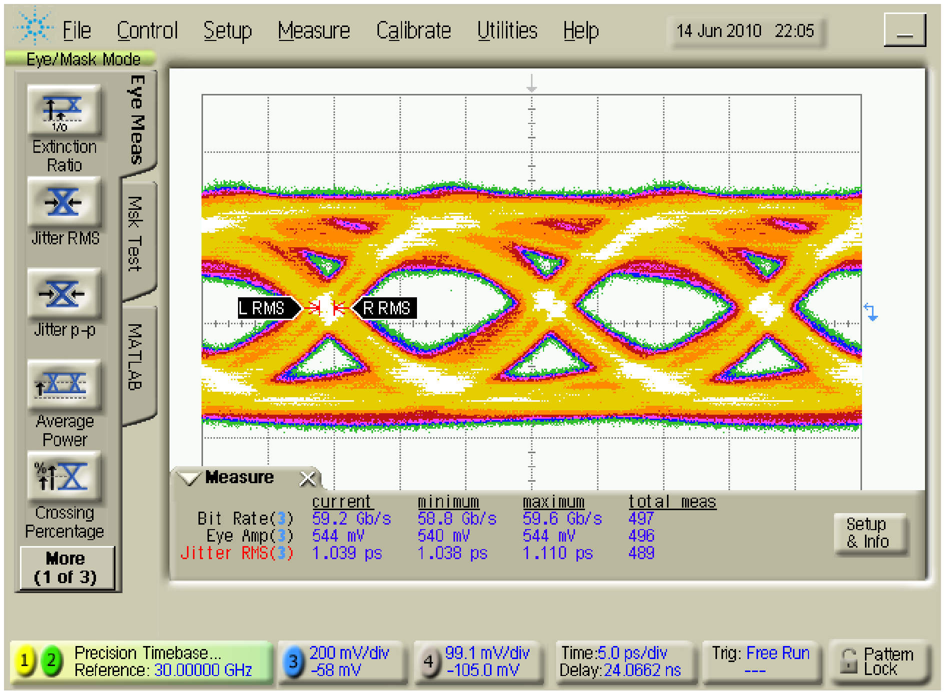


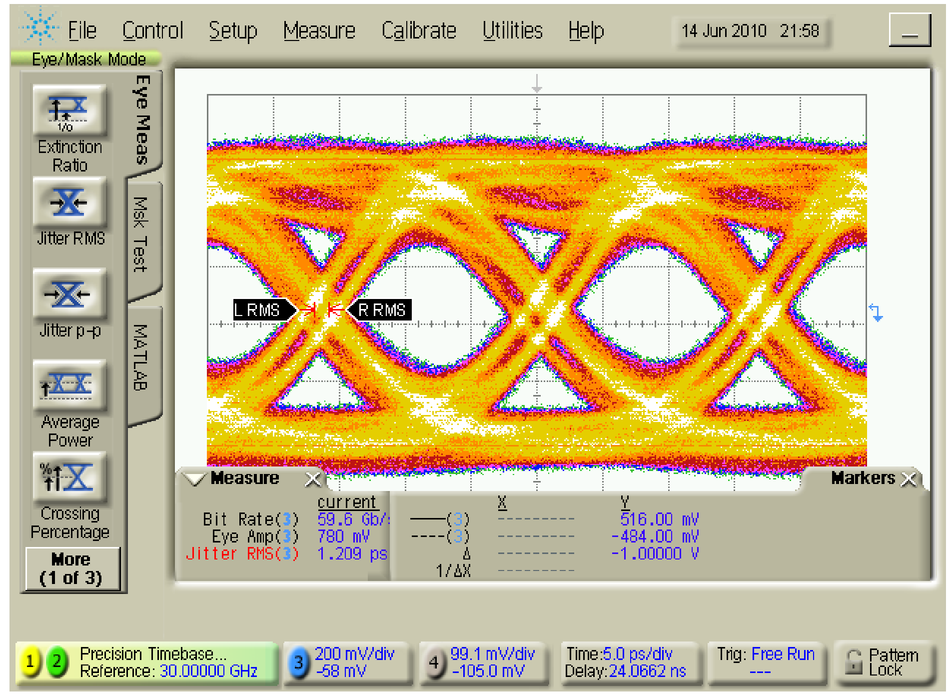






60-Gb/s Eyes with 500mVpp and 800mVpp swing per side





56-Gb/s DAC in 65-nm p-MOS CML
(Ciena ISSCC 2011)

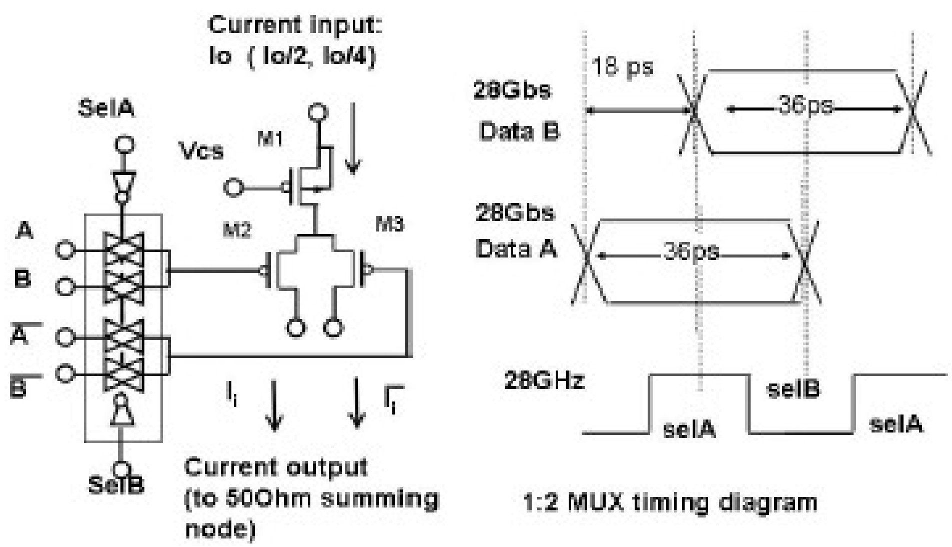


Figure 10.8.3: Unit current steering cell with 2:1 MUX.

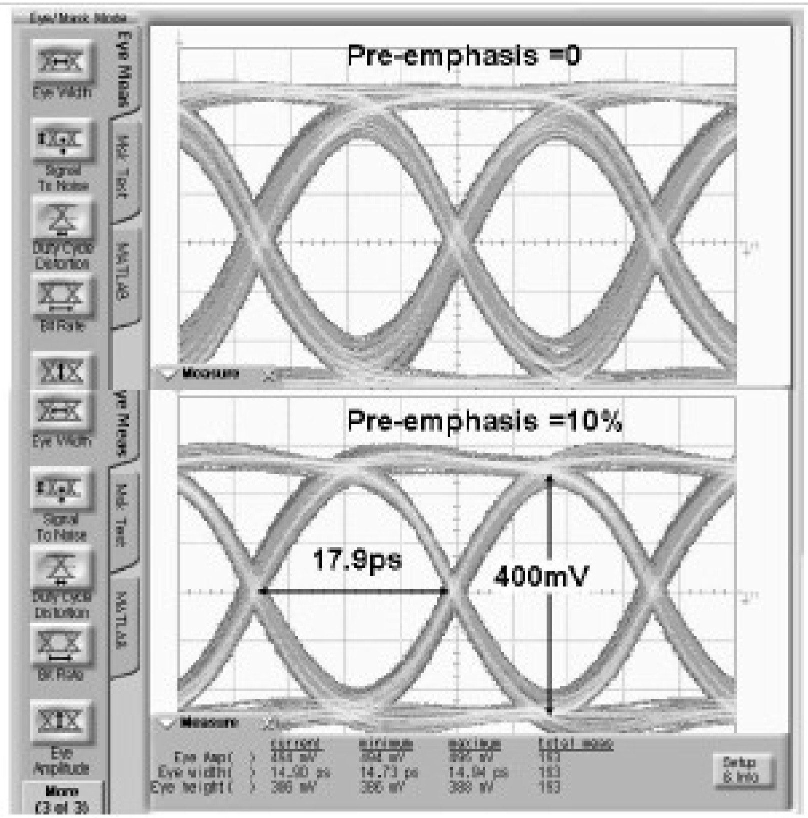


Figure 10.8.5: 56Gb/s 256b PRBS eye with 0% (top) and 10% (bottom) pre-emphasis @28GHz.

Back-up

Design example: 40 Gb/s, 2V SiGe HBT driver

- 2V over 25 Ω load results in 80 mA tail current.
- I_{MOD}= 80 mA, A_E= 80mA/9mA = 9 μm^2, L_E = 45 μm
- g_m = 1.6 S, R_b=6.7 Ω
- C_π = 1.05 pF, C_{cs} = 50 fF, C_μ = 99 fF
- Use emitter degeneration (R_E=12.5 Ω) such that A_v= -2 (previous stage needs 1V swing!)
- $\tau = R_b[C_\pi/(1+g_m R_E) + 3\,C_\mu] + 25\,(C_{cs} + C_\mu + C_{PAD})$

Design example: 40-Gb/s, 2V SiGe HBT driver

- τ = 6.7x(1.05p /21+ 0.297p) + 25x 0.199ps
- τ = 2.3ps + 5ps = 8.3ps
- Assuming emitter followers to reduce source impedance BW_{3dB} = 19 GHz (not adequate)
- Inductive peaking not possible: current is too large and SRF becomes too low
- Use distributed amp with 5 stages, each with 16 mA tail

Design example: 40-Gb/s, 2Vswing SiGe HBT driver

- Gain per stage is still 2
- g_m = 0.32 S, R_b=33.5 Ω
- C_π = 201 fF, C_{cs} = 10 fF, C_μ = 20 fF
- The input/output lines can be loaded by a unit capacitance of 100 fF
- $L = C Z_o^2$ = 250 pH
- $BW_{3dB} = 1/[\pi(LC)^{1/2}]$ = 63 GHz ... but will be limited by frequency at which transistor MAG = 6 dB (A_v = 2)