Schedule

The following table gives the course schedule for Stanford EE273 taught during Autumn Quarter 1998. Each row summarizes the contents of one lecture. Also listed are the reading assignments that should be completed before each lecture and homework assignments that reinforce the lecture material.

Lecture	Date	Topic	Reading	Homework
1	23 Sep	Introduction to Digital Systems Engineering: Overview of signaling, power distribution, timing, and noise issues. Technology trends in digital systems.	1	HW1: 1-1, 1-5, 1-9
2	28 Sep	Wires: Electrical models of wires. Lossless transmission line model. Termination and reflections. The Telegrapher's equation. TDR demonstration.	3.1 through 3.3.3	None
3	30 Sep	More on wires: Lossy transmission lines. Skin effect resistance and dielectric absorption. Multidrop buses. Balanced lines. Common and differential mode analysis.	3.3.4 through 3.5.2	HW2: 3-2, 3-6, 3-7, 3-16 (SPICE all problems)
4	05 Oct	Wire Wrapup: modeling and analysis of wires. Use of the TDR.	3.6 and 3.7	None
5	07 Oct	Noise: Overview of noise sources. Power supply noise. Crosstalk - capacitive lines - coupled transmission lines - even and odd mode deriviation - signal return crosstalk.	6.1 through 6.3	HW3: 6-3, 6-6, 6-7, 6-13, 6-16
6	12 Oct	More on noise: intersymbol interference, alpha particles, thermal and shot noise, parameter variations. Managing noise. Noise budgets and BER.	6.4 through 6.6	None
7	14 Oct	Signaling: A quick comparison. Transmission modes, receiver operation - references and noise cancellation, termination methods. Differential signaling.	7.1 and 7.3	HW4: 7-2, 7-7, 7-8
8	19 Oct	More Signaling: Signaling over capacitive lines. Signaling over inductive lines. Signal encoding.	7.4 and 7.5	None
9	21 Oct	Advanced Signaling. Simultaneous bidirectional signaling. Driving lossy RC lines. Equalization for lossy LRC lines. DC balanced codes.	8.1 through 8.4	None
Midterm	26 Oct	Midterm in the evening, location TBD, no class on this day	None	None
10	28 Oct	Timing: Signals, values, and events. Clock domains. Timing uncertainty: skew and jitter. Synchronous timing and pipeline timing conventions.	9.1 through 9.5	HW5: Crosstalk to RC lines, 8-2, 9-2, 9-3
11	02 Nov	Closed-loop timing: Measuring and canceling skew. A simple timing loop. Timing loop components. Bundled closed-loop timing. Per-line closed-loop timing.	9.6.1 through 9.6.5	None
12	04 Nov	Clock distribution: off-chip distribution: clock trees, phase-locked distribution, salphasic distribution. On-chip distribution: trees, meshes, jitter calculations.	9.7	HW6: 9-6 (SPICE it), clock dist problem w/ spice
13	09 Nov	The synchronization problem: why synchronize, metastability and synchronization failure, calculating failure probability, common synchronizer pitfalls, synchronization hierarchy.	10.1 and 10.2	None
14	11 Nov	Synchronizer design: brute-force synchronizer; mesochronous syncrhonizers: two-register synchronizer, FIFO synchronizer; plesiochronous synchronization, dealing with data-rate mismatch, arbitrary periodic synchronization, the clock predictor.	10.3	Project assigned
15	16 Nov	Asynchronous design: signaling conventions, stoppable clocks, trajectory-map synthesis.	10.4	None

16	18 Nov	Off-Chip Power Distribution: the power distribution problem, local loads and signal loads, a typical distribution network. Bypass capacitors. Regulators: shunt regulators, series regulators, switching regulators.	5.1, 5.2, and 5.5	None
17	23 Nov	On-Chip Power distribution: current-profile of digital functions, IR drops, fraction of metal coverage, deliberate and symbiotic bypass capacitance, local regulation.	5.3	None
18	25 Nov	Slack	None	None
19	30 Nov	Project presentations	None	project due
20	02 Dec	Project presentations	None	project due
Final	10 Dec	8:30AM-10:30AM	None	None