Problems for Chapter 14 of 'Ultra Low Power Bioelectronics'

Problem 14.1

Subthreshold MOS current-mode circuits are typically less accurate than those using bipolar transistors. One reason is that the linear range of a subthreshold MOSFET, which is given by ϕ_t/κ is not constant. It varies from device to device as κ changes with the operating point and source-to-bulk voltage of the transistor. This problem uses the simplest current-mode circuit, a current mirror, to illustrate the effects of variations in κ.

Suppose you need a current mirror that has a large input-to-output current gain, and that the gain must remain constant over a range of input currents. You might try the source-shifting technique shown in Figure P14.1. Let's examine this circuit's behavior. Assume the transistors are the same size, operate in subthreshold, and are saturated.

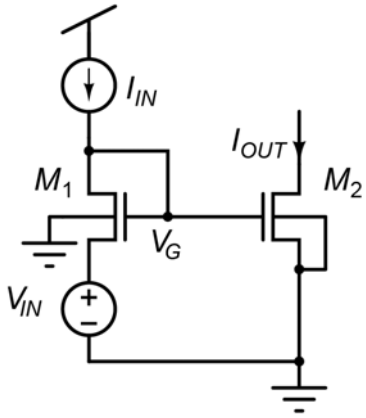

Figure P14.1: A source-shifted current-mirror circuit.

a) First assume that the κ of the two transistors is identical, i.e., $\kappa_{in} = \kappa_{out} = \kappa$. Identify the translinear loop in the circuit and use the static translinear principle to find the dc current gain I_{OUT} / I_{IN}. Does the gain depend on I_{IN} or κ?

b) Let us now remove the assumption made in part a). Write down the source-referenced large-signal current equations for both transistors. Do not assume that the two transistors have the same value of κ.

c) Find the threshold voltage of the input transistor as a function of V_{IN}. Linearize the expression. State clearly the conditions under which the linearization is valid.

d) Use the equations developed in parts c) and d) to show that the current gain is given by

$$\frac{I_{OUT}}{I_{IN}} = \left(\frac{I_{IN}}{I_{T0}}\right)^{(\kappa_{out}-\kappa_{in})/\kappa_{in}} e^{V_{IN}/\phi_t}$$

where I_{T0} is the threshold current for the input transistor, i.e., the current at which the gate-to-source voltage is equal to the threshold voltage.

e) Write down expressions for κ_{in} and κ_{out} in terms of V_{IN} and process parameters. Simplify these expressions to show that

$$\frac{\left(\kappa_{out}-\kappa_{in}\right)}{\kappa_{in}} \approx -\left(1-\kappa_{out}\right)\frac{V_{IN}}{2\phi_0}$$

where ϕ_0 is the inversion potential of the channel. Under what conditions is the approximation in the above equation valid?

f) Combine the results from parts d) and e) and plot the current gain as a function of I_{IN} for various values of V_{IN}. You may assume the following parameter values: $\gamma = 0.6\ \text{V}^{1/2}$, $\phi_0 = 1$ V, $I_0 = 1\ \mu$A.

g) Estimate the significance of the fact that $\kappa_{\text{out}} \neq \kappa_{\text{in}}$ by plotting the percentage change in gain that can be attributed to this effect. For what values of I_{IN} and V_{IN} is the effect significant, if any?

Problem 14.2

Consider the circuit shown in Figure P14.2. Assume that all the transistors are identical, have no Early effect, and the bipolar transistors have infinite current gain (β).

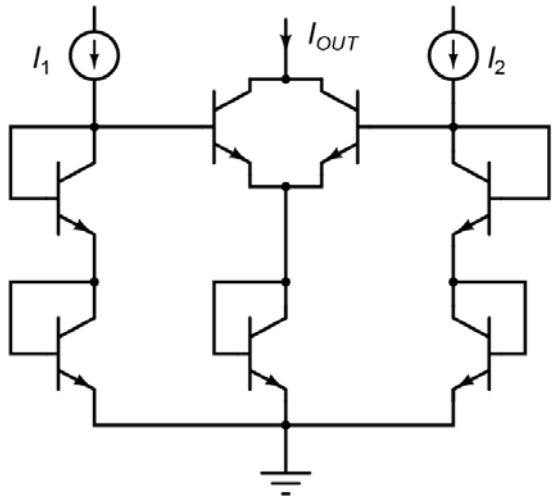

Figure P14.2: A current-mode circuit

a) Identify the translinear loops present within this circuit.

b) Use the static translinear principle to find the dc output current I_{OUT} in terms of the input currents $I_1$and I_2.

c) Draw a generalized version of this circuit that can handle any number of input currents.

Problem 14.3

Consider the circuit shown in Figure P14.3. Assume that all the transistors are identical, and have no Early effect. Also assume that I_B, $I_{IN,1}$, $I_{IN,2}$, ..., $I_{IN,N}$ are ideal current sources.

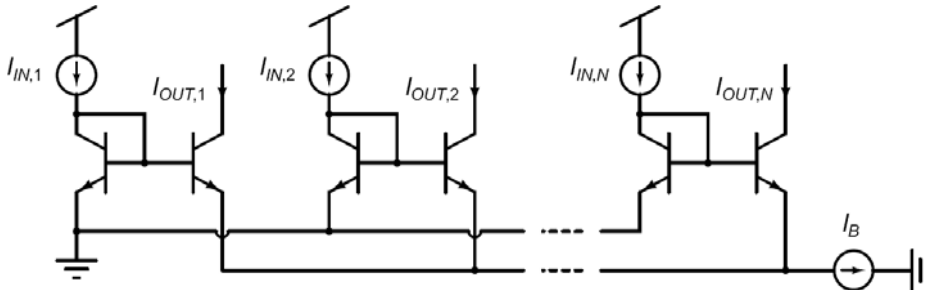

Figure P14.3: A current-mode circuit

a) Identify the translinear loops present within this circuit assuming that the I_B current source operates with very low voltage across it and that all transistors are in saturation.

b) Use the static translinear principle to find the dc output currents $I_{OUT,i}$ in terms of the input currents, where $1 \le i \le N$.

Problem 14.4

Consider the circuit shown in Figure P14.4. Assume that all the transistors are identical, have no Early effect, and have infinite current gain. Also assume that all current sources are ideal.

a) Identify the translinear loops present within this circuit.

b) Split up the input currents into common-mode and differential components, as follows:

$$i_{A1} = I_A + i_a / 2, \quad i_{A2} = I_A - i_a / 2$$
$$i_{B1} = I_B + i_b / 2, \quad i_{B2} = I_B - i_b / 2$$

Now use the static translinear principle to find the transfer function between the differential output current $i_{OUT} = i_{OUT1} - i_{OUT2}$ and the differential input currents I_a and I_b.

c) What are the allowable magnitudes and signs of the differential input currents? [Hint: think about the conditions that must be satisfied in order for the analysis in part b) to be valid.]

d) What are the functions of the diode-connected transistors? What function does the overall circuit perform?

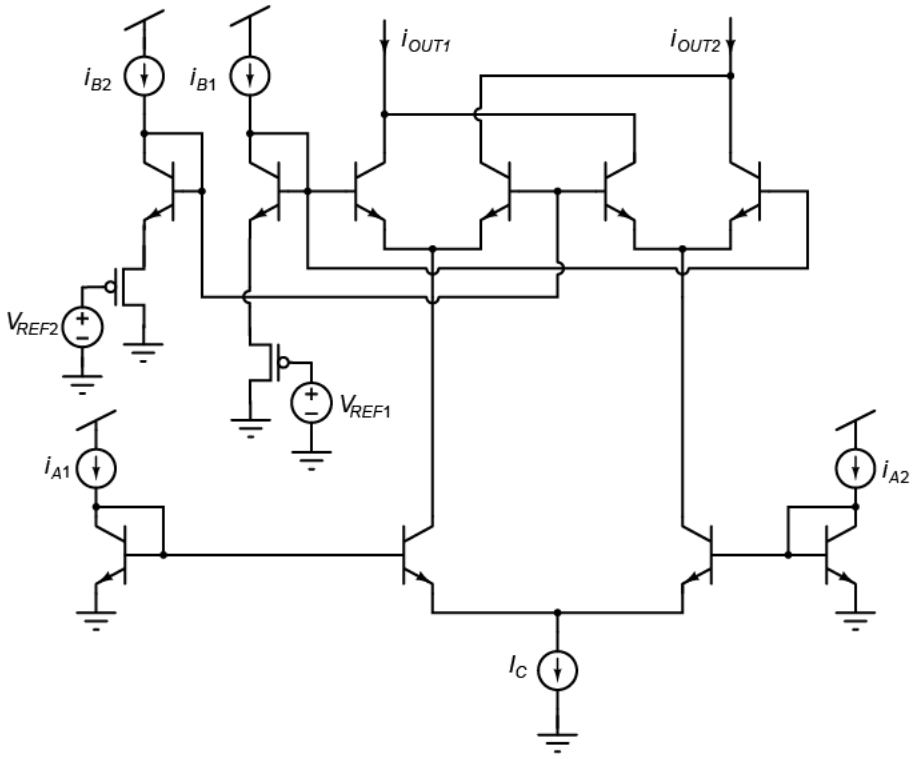

Figure P14.4: A current-mode circuit.

Problem 14.5

Consider the current-mode low-pass filter circuit shown in Figure 14.9. Assume that you want to use this circuit to create a filter with DC gain A_{DC} = 10 and corner frequency of f_c = 1 kHz. Assume that all transistors have infinite Early voltage and infinite dc current gain.

a) Because of layout and device parasitics, you find that the drain of Q_3 has a parasitic capacitance C_B = 10 fF to ground. What is the minimum value of output capacitance C that will guarantee that the parasitic pole caused by C_B is at least two decades higher than the corner frequency of the filter?

b) You decide to use the minimum allowable value of C, determined in part a), for your design. What values of I_A and I_B must now be used to get the right dc gain and cutoff frequency?

c) What is the maximum allowable parasitic capacitance C_C that can be present between V_C and ground in order to ensure that the local feedback loop consisting of Q_3 and M_1 will be over-damped? You may find the two-pole closed-loop τ and Q rules useful (Section 9.4 and Figure 11.12).

Problem 14.6

Consider the modified winner-take-all circuit shown in Figure P14.6.

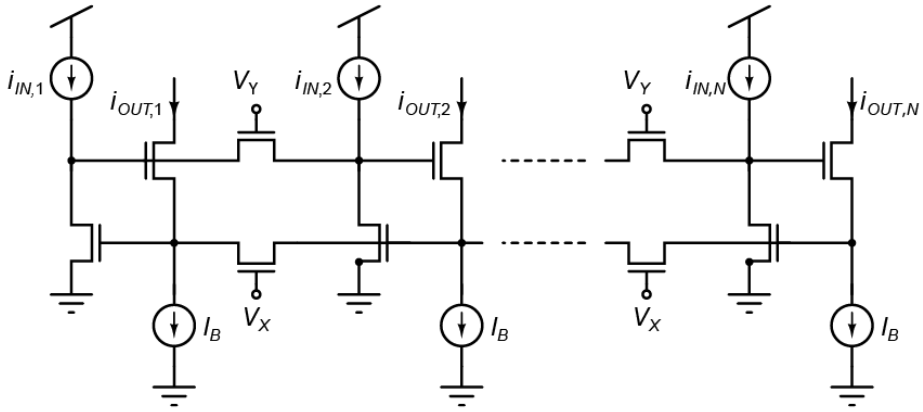

Figure P14.6: A modified winner-take-all circuit

a) Explain intuitively the function of the transistors with gate voltages V_X and V_Y [Hint: these transistors can be viewed as voltage-controlled resistors.].
b) **The following questions require the use of a circuit simulator such as SPICE**. Implement a version of this circuit with $N = 16$ stages. Initially, set $V_X = V_{DD}$ and $V_Y = 0$. Set i_{IN} to a random input vector, simulate the circuit and explain its behavior. Repeat your simulation for various input vectors.
c) Gradually increase V_Y and explain the behavior of the circuit.
d) Set $V_Y = 0$, gradually decrease V_X and explain the behavior of the circuit.
e) What are the effects of combining the conditions simulated in parts c) and d), i.e., simultaneously varying V_X and V_Y? Do the effects of the two voltages combine linearly?
f) Propose two practical applications for this circuit.

Problem 14.7

Consider the current-mode circuit shown in Figure P14.7. You may assume that I_B and I_P are constant current sources, and that $i_{IN,,i}$ and $i_{OUT,,i}$ are input and output currents, respectively, with $1 \le i \le N$.

a) Explain intuitively, without any mathematics, the function of this circuit.
b) Assume that all the input currents are initially equal at i_{IN}. Now let the i-th current change by a small amount Δi_{in} . Calculate the resultant changes in the output currents of all channels. Justify any assumptions that you make.
c) **The following question requires the use of a circuit simulator such as SPICE.** Implement a version of this circuit with $N = 4$ stages, and perform dc simulations to verify that it behaves as expected.
d) Show how a ring of two cortex-inspired networks like those of Figure 14.22 (b) can implement a similar function to that implemented by Figure P14.6, if appropriate weights are used.

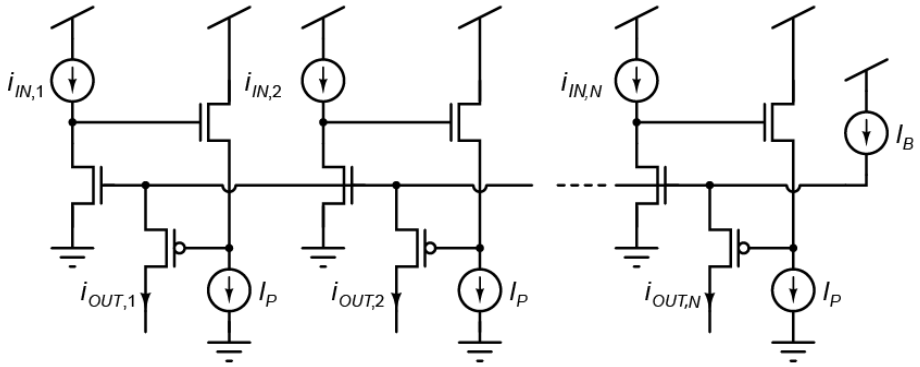

Figure P14.7: A current-mode circuit

Problem 14.8

Consider the current-mode low-pass filter circuit shown in Figure 14.9. This circuit requires, in addition to the normal power supply voltages, an additional DC voltage, labeled V_{CONST} in the figure, to function. Such voltage sources are required in many other current-mode circuits as well.

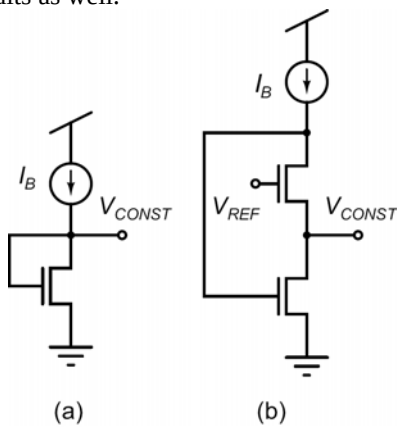

Figure P14.8: Biasing schemes for biasing current-mode circuits

a) Explain the necessity for V_{CONST}. Why can't the emitter of transistor Q_1 simply be shorted to ground? What value of V_{CONST} should be used?
b) Are there any requirements on the output impedance of the voltage source V_{CONST}? Explain.
c) Figure P14.8 shows two circuits for generating V_{CONST}. Calculate the output impedance of both circuits. Which one would you prefer for this application, and why?
d) Assume that parasitic capacitances are present at each node of the circuit shown in Figure P14.8 (b). Draw a feedback block diagram that represents its small-signal behavior. What conditions must be satisfied for the circuit to be stable? Explain any assumptions that you make.
e) What is the maximum current that can be sourced or sunk by the circuits shown in Figure P14.8? Does your answer to this question modify any of the conclusions you reached in part c)?

Problem 14.9

This question requires the use of a circuit simulator such as SPICE. Consider the current-mode low-pass filter circuit shown in Figure 14.15 (a).

a) Implement the filter circuit shown in the figure in a standard CMOS process such that it has a dc gain of 1 and a 3 dB cutoff frequency of 1 kHz. Explain the purpose of any modifications that you make to the circuit. [Hint: in a typical n-well process, consider replacing all NPN transistors with PMOS transistors.]

b) Perform small-signal ac simulations to verify the functionality of your circuit.

c) Assume that the input current amplitude is limited to a maximum of 50 nA, and bias the circuit in class-A mode.

d) Find the power spectral density of the output current noise, and plot the output *SNR* as a function of the input signal amplitude. Explain any assumptions that you make.

e) Use transient simulations to feed sinusoidal currents of various amplitudes and frequencies into your circuit. Estimate and plot the total harmonic distortion (THD) at the output in each case. You may want to use the following set of frequencies: $\{0.2\omega_c, \omega_c, 5\omega_c\}$, where ω_c is the 3-dB cutoff frequency of the filter.

f) What is the dynamic range of operation of your filter? Explain any assumptions that you make.

g) Now assume that the circuit is biased in adaptive class-A mode. For the purposes of this question, you do not need to build the envelope detector required to actually implement such a scheme. Simply set an appropriate input dc bias current "by hand'' for each input signal amplitude used in your simulations.

h) Repeat parts d), e), and f) for this biasing scheme.

i) Is there a maximum output *SNR* in the adaptive class-A case? Use its value to estimate the equivalent number of shot-noise sources within the log-domain core of the filter.

Problem 14.10

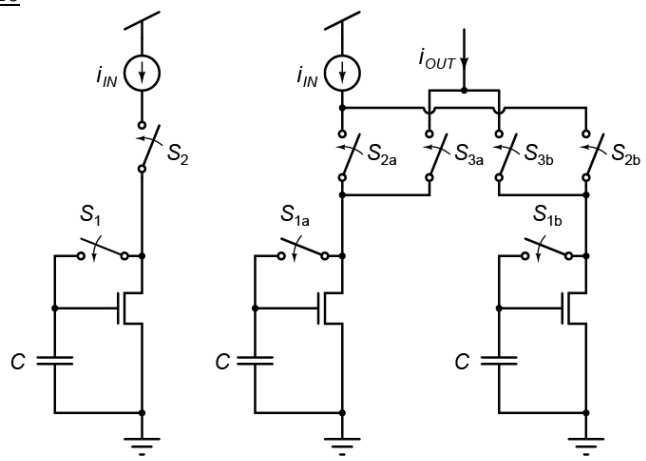

Figure P14.10: Two switched-current circuits

Current mirrors are commonly used for copying currents within current-mode circuits. Unfortunately, their accuracy is limited by device mismatch. Several schemes have been proposed for eliminating this problem. Consider the circuits shown in Figure P14.10. The switches are controlled by clock phases, which are generated using other circuitry (not shown).

a) How would you improve the accuracy of a standard current mirror circuit? Are there trade-offs between speed and accuracy? Are there special requirements for current mirrors used within current-mode circuits?

b) The circuit in Figure P14.10 (a) is known as a switched-current cell. It is used to copy the input current i_{IN} to a load (not shown). Draw a diagram containing the switching waveforms required for the circuit to function properly.

c) Explain why the accuracy of this circuit is not affected by the mismatch properties of the transistor or the possible nonlinearity of capacitor C.

d) What are the main sources of copying error in this circuit? Propose schemes to alleviate their effects.

e) Unlike a normal current mirror, a single switched-current cell cannot deliver current continuously to its load. The combination of two cells shown in Figure P14.10 (b) is known as a dynamic mirror. It is designed to provide continuous output current. Explain intuitively how this circuit works, and draw a diagram containing the switching waveforms required for the circuit to function properly.