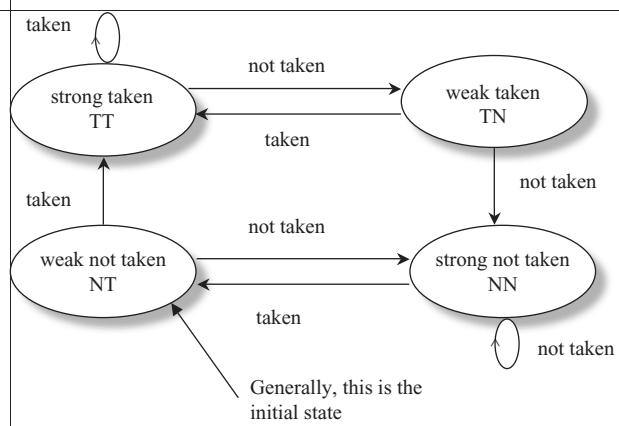


Convert Art

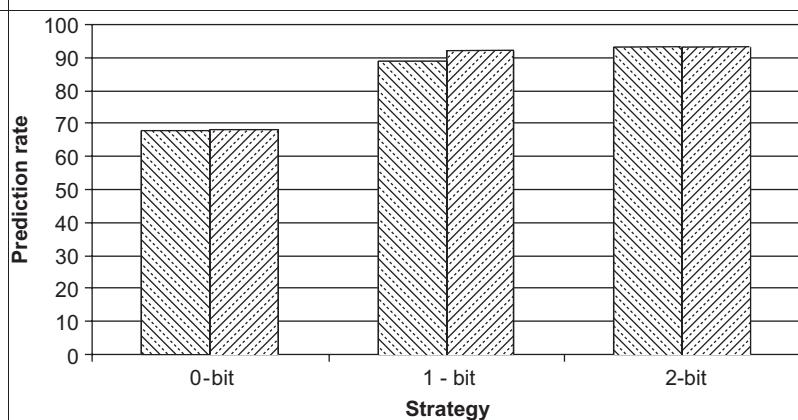
Figure 04-02.

5



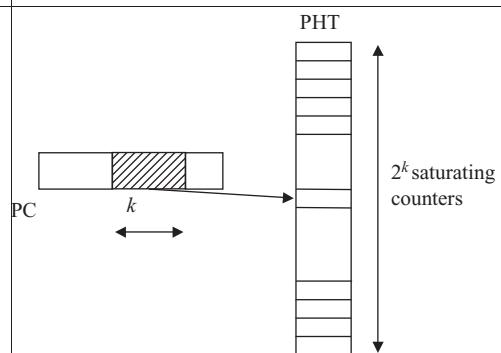
Convert Art

Figure 04-03.



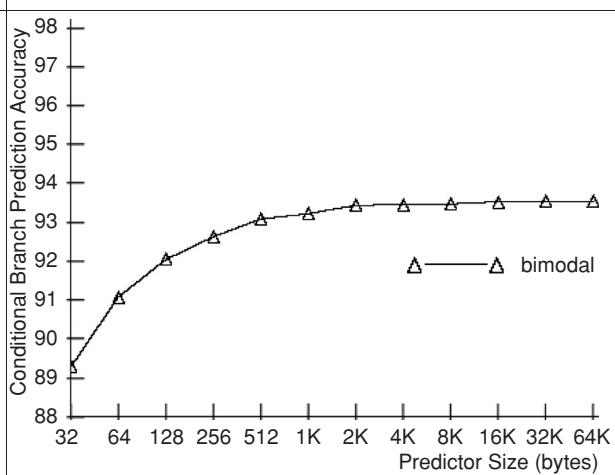
Convert Art

Figure 04-04.



Convert Art

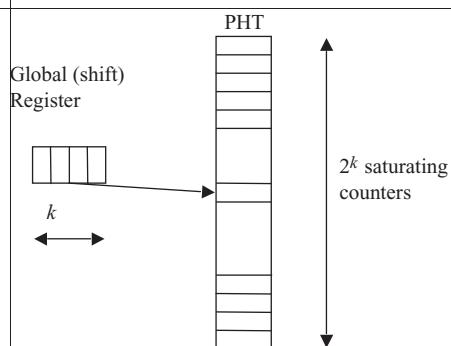
Figure 04-05.



Relabal Art

Figure 04-06.

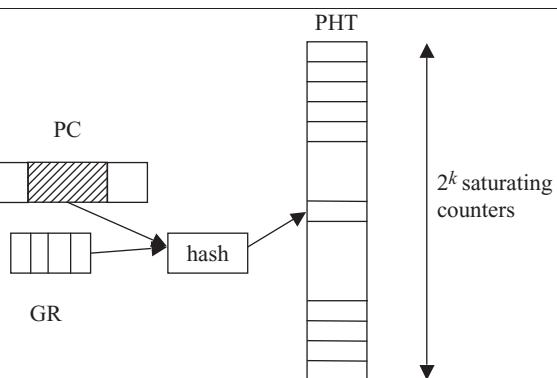
13



Convert Art

Figure 04-07.

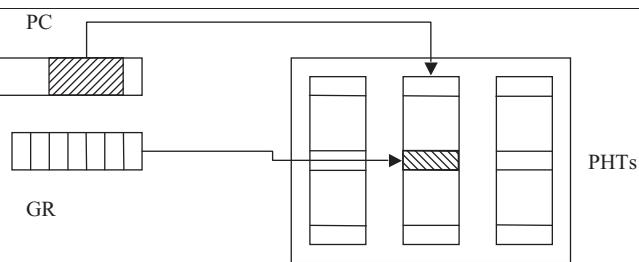
15



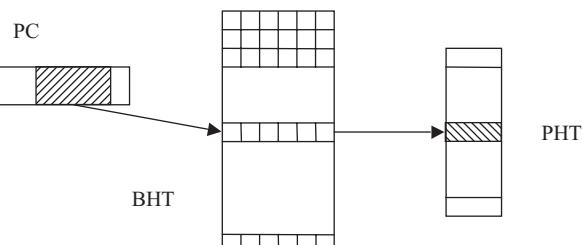
Convert Art

Figure 04-08.

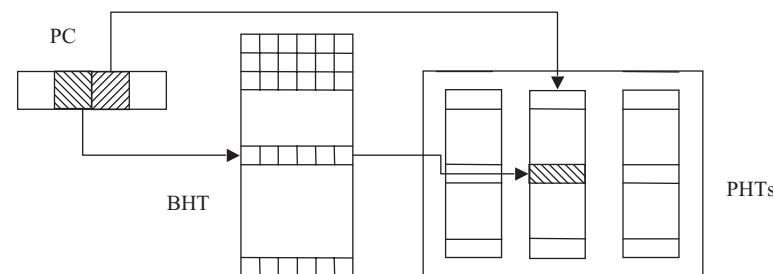
17



(a) 1 Global register, several PHTs (Global-set). Selected bits of the PC point to a PHT; the GR points to a row of the PHTs



(b) Table of local history registers (BHT) and one PHT (Set-global). Selected bits of the PC point to a local history register which in turns points to a saturating counter in the PHT.

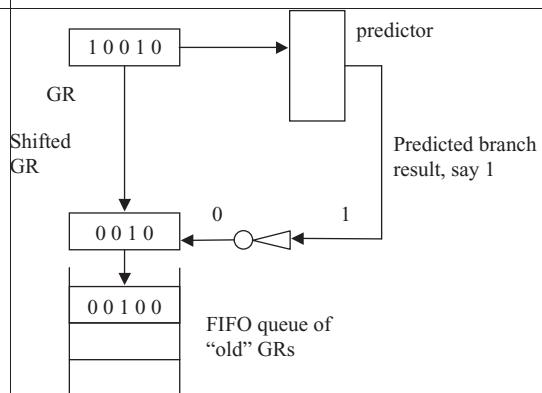


(c) Table of local history registers (BHT) and several PHTs (Set-set). Selected bits of the PC point to a local history register which in turns points to a row in the PHTs. Other bits of the PC select the PHT.

Convert Art

Figure 04-09.

19



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Figure 04-10.

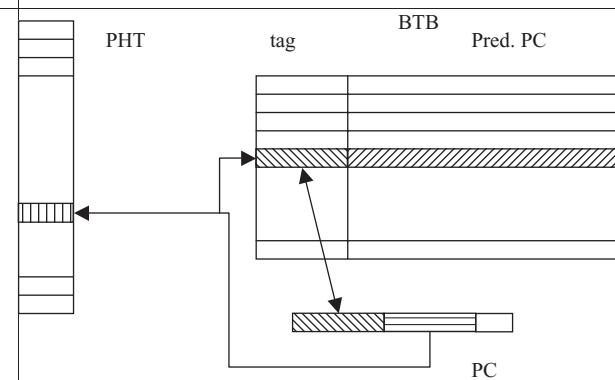
21

Tag (cache-like)	Target instruction address or I-cache line target address, i.e., next predicted PC	Pred

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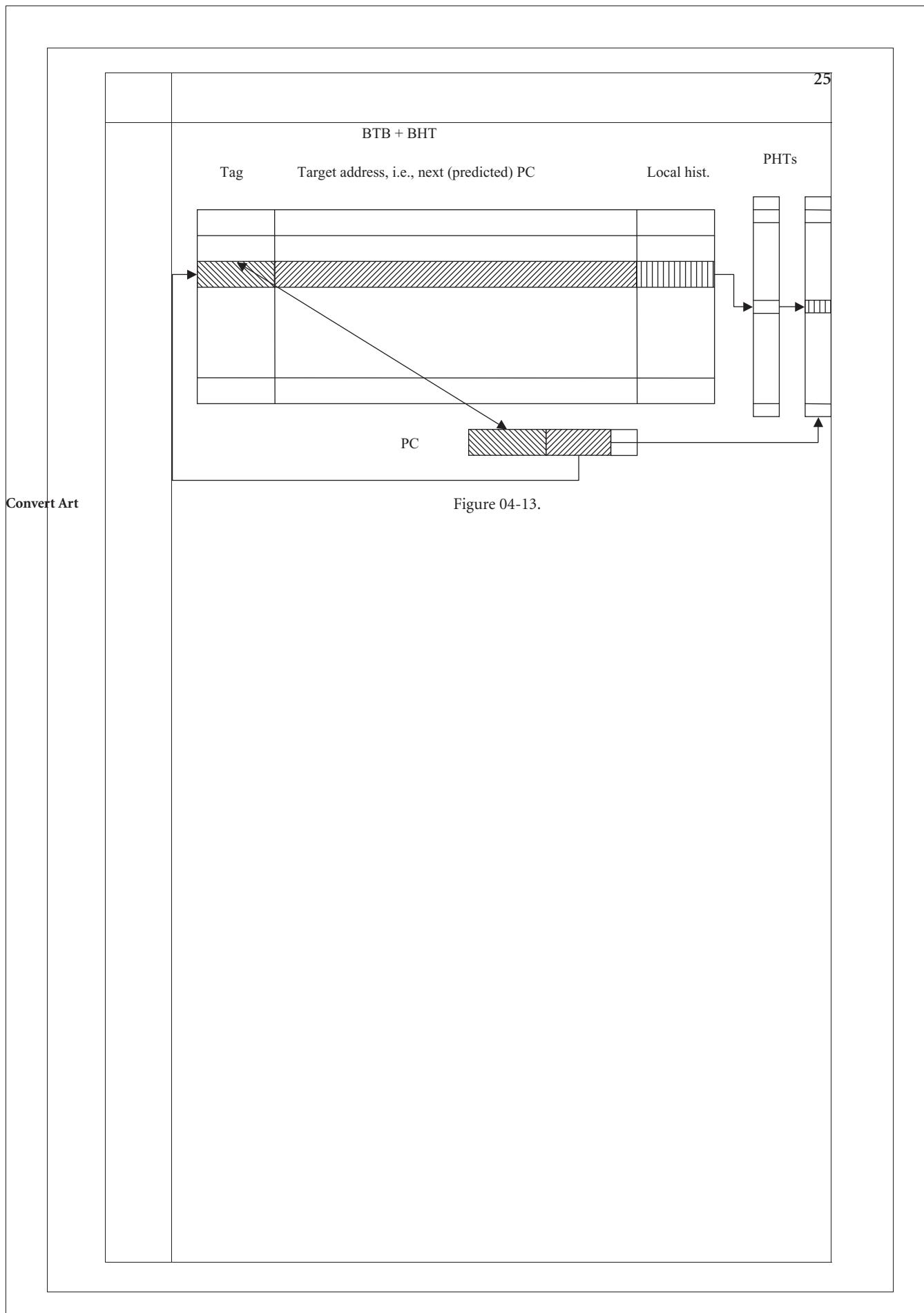
Figure 04-11.

23

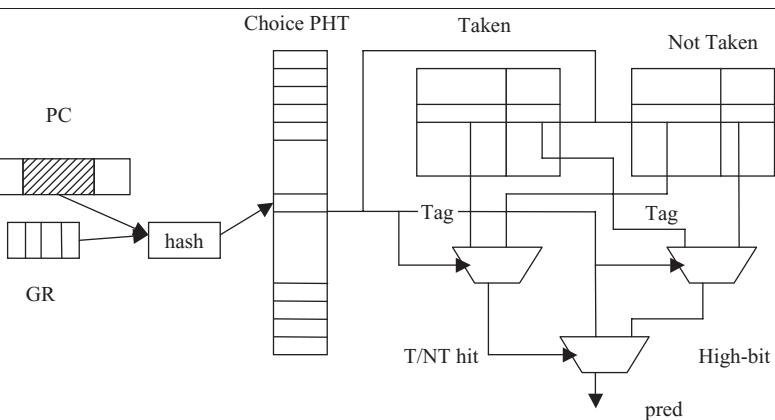


Convert Art

Figure 04-12.



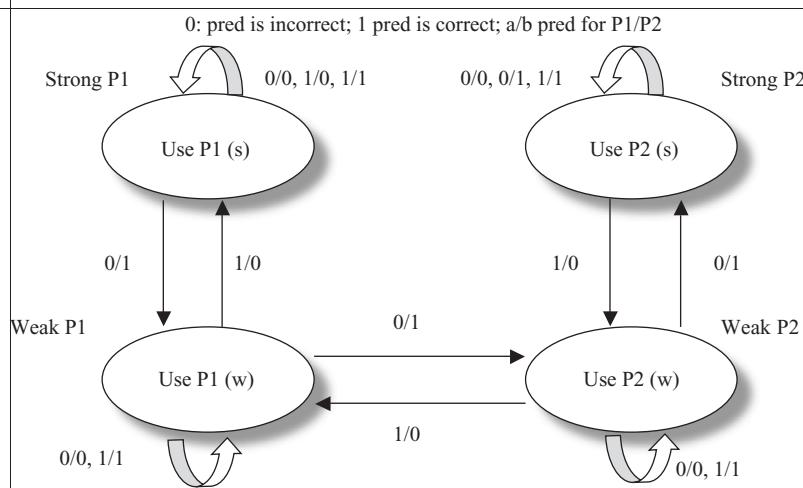
27



Convert Art

Figure 04-14.

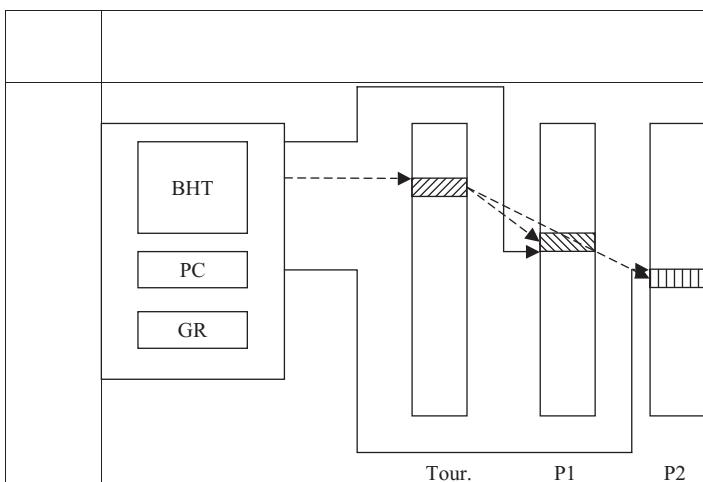
29



Convert Art

Figure 04-15.

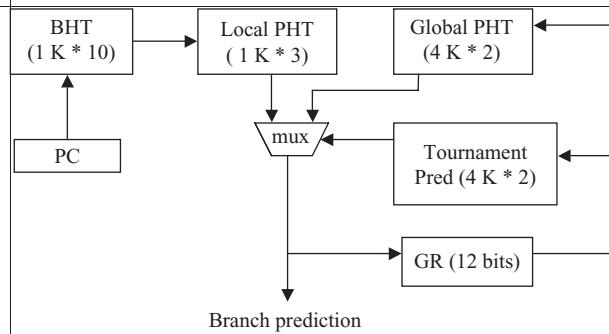
31



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Figure 04-16.

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Convert Art

Figure 04-17.

35

Tag	Inst <sub>0</sub>	Inst <sub>1</sub>	...	Inst <sub>m-1</sub>	Pos	Ind	Dis	Way
-----	-------------------	-------------------	-----	---------------------	-----	-----	-----	-----

 $m$  instructions

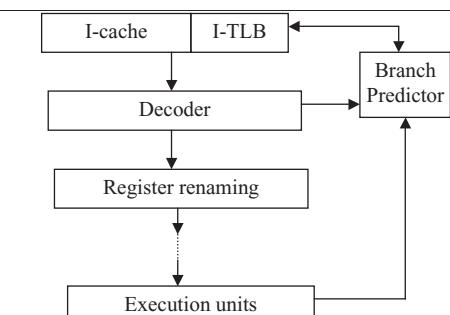
Id. of target address

Will be repeated  $k = l/m$  times where  $l$  is the I-cache line size

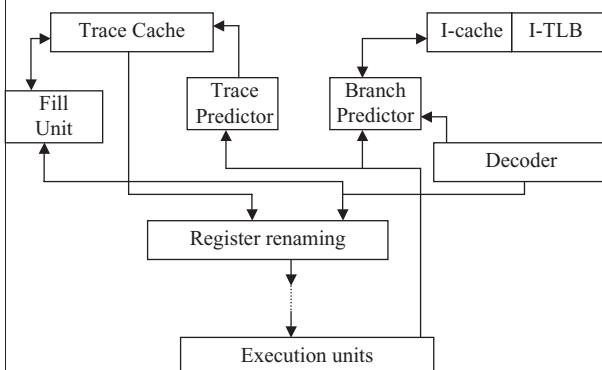
Convert Art

Figure 04-18.

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(a) Instruction Fetch Unit using an I-cache

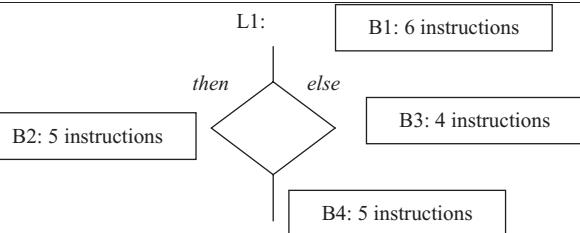


(b) Instruction Fetch Unit using a Trace cache

Convert Art

Figure 04-19.

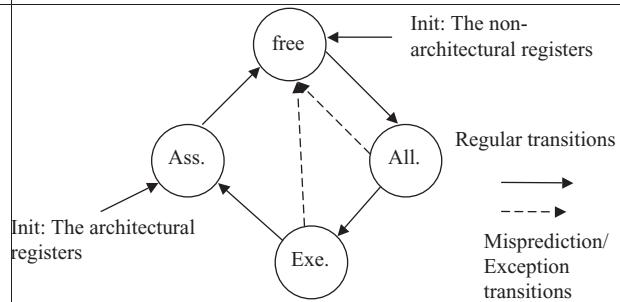
39



Convert Art

Figure 04-20.

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Convert Art

Figure 04-21.