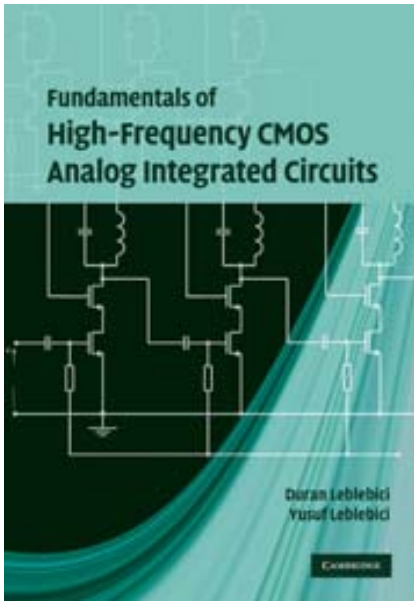

Fundamentals of High-Frequency CMOS Analog Integrated Circuits

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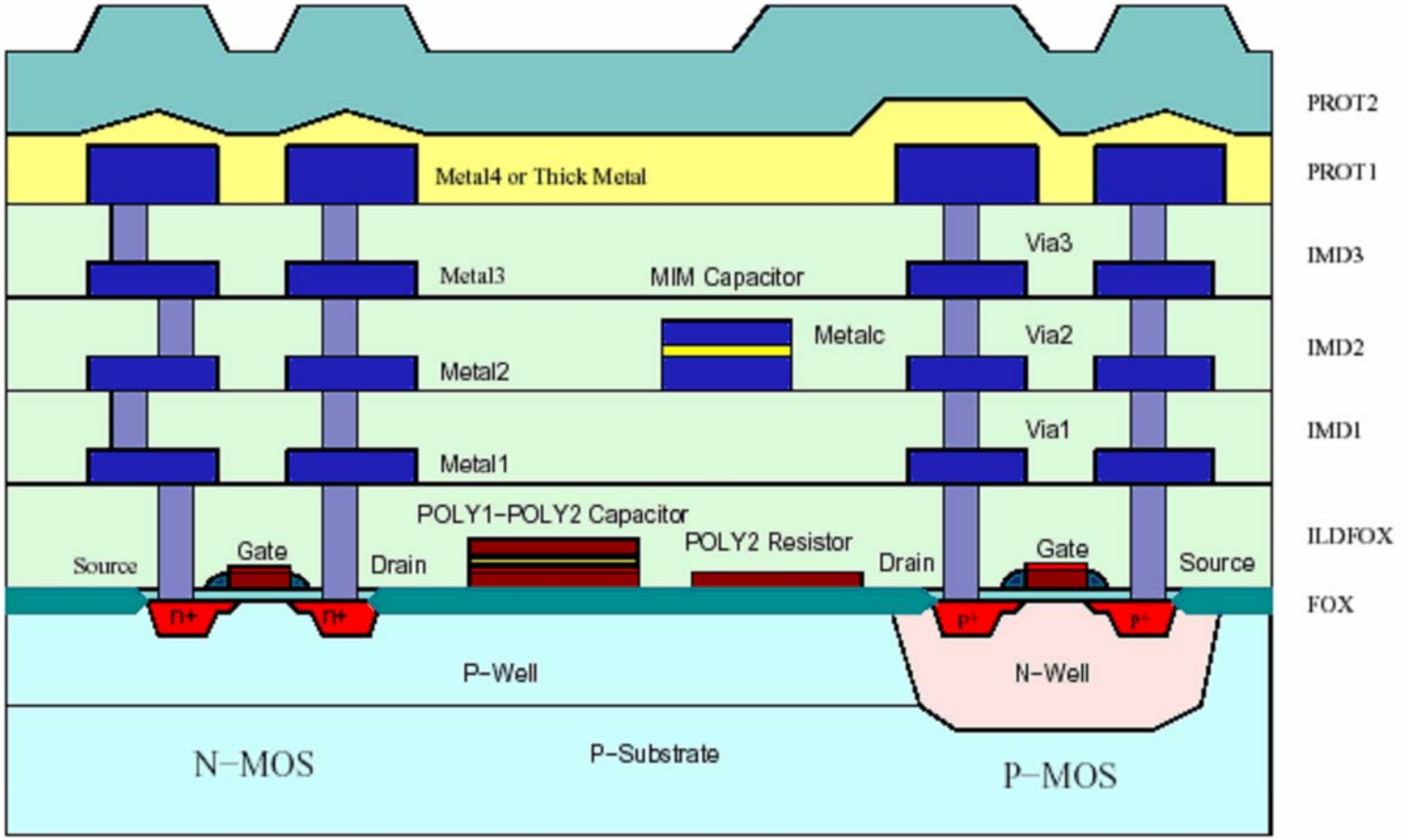
Yusuf Leblebici

Chapter 1

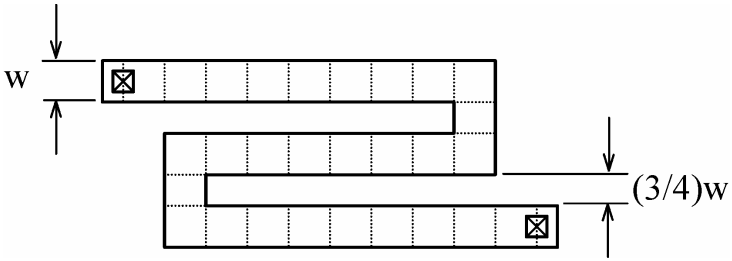
Components of Analog CMOS Integrated Circuits (Passive Components)

Passive on-chip components:



Cross-section of a typical CMOS - IC (AMS035)

Resistors:



$$R \cong R_{sh}(N_{sq} + 0.6 \times N_{corner}) + (2 \times R_{contact})$$

R_{sh} : Sheet resistance of the conductive thin layer in ohm/square

Sheet resistances are process and material dependent. Typical values:

- Gate poly-Si: R_{sh}= 5...10 Ω/□
- High resistivity poly: R_{sh}= 1...2 kΩ/□
- Metal (Al) films: R_{sh}= 50...100 mΩ/□
- Doped Si regions
  - S and D regions: R_{sh}= 50...100 Ω/□
  - Well regions: R_{sh}= 1...2 kΩ/□

Absolute tolerances: ≈ 20%
Relative tolerances: Smaller, depend on the dimensions.
Contact resistances: Depend on the technology and size.

Typical (max) values for AMS 035, A= 0.4 μm × 0.4 μm

- Metal - poly: 2 (10) Ω/contact
- Metal - n type S/D: 30(100) Ω/contact
- Metal - p type S/D: 60(150) Ω/contact

(N parallel contacts decrease the resistance N times, and increase the reliability !)

Capacitors:

- Passive (fixed) capacitors
- Varactors

Passive capacitors:

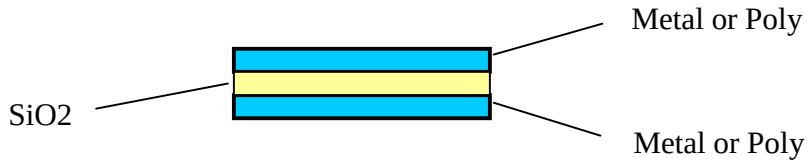
a) Poly 1 - poly 2 capacitors

b) Metal - metal (MIM) capacitors

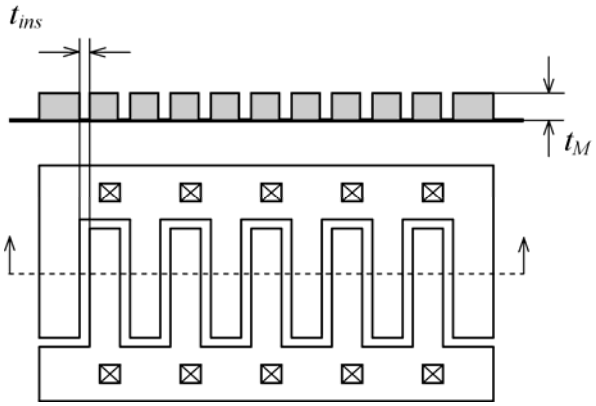
Insulator: SiO_2 , $C = \dfrac{34.5}{t_{ox}\left[\text{nm}\right]}\ \left[\text{fF}\right]$

(Edge-effects for small geometries !)

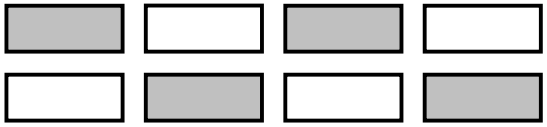
Planar capacitor:



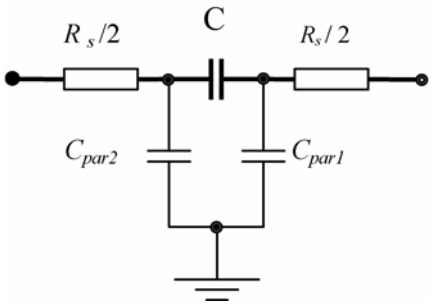
Finger capacitor:



Two layer finger structure:



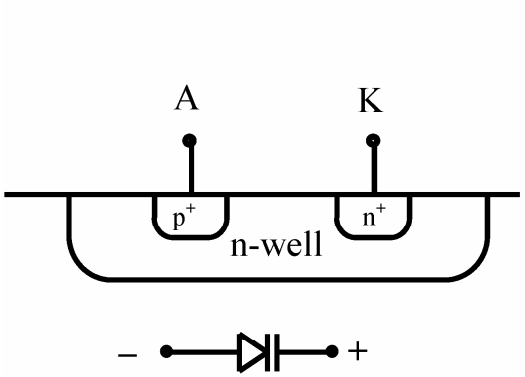
Parasitics:

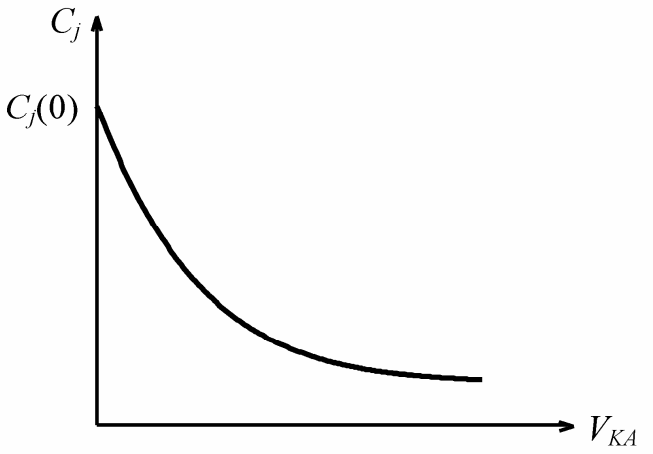


Varactors:

a) p-n junction varactor

$$C_j(V) = C_j(0)\left(1 - \frac{V}{\Phi_B}\right)^{-m}$$





$\Phi_B =$ PB $= 0.65....0.75$ [V]

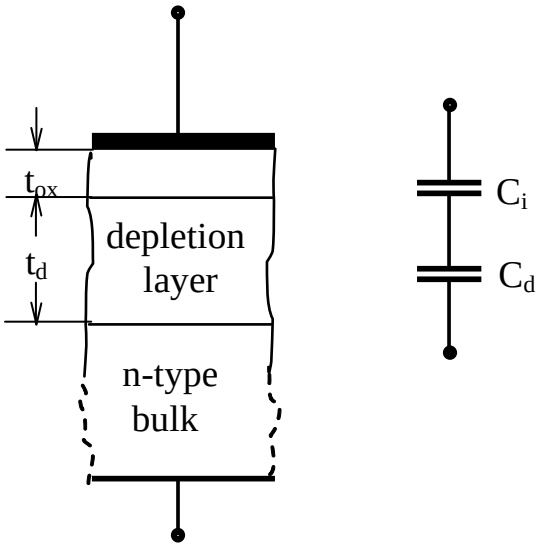
$m = (1/3)....(1/2)$

Tuning range:

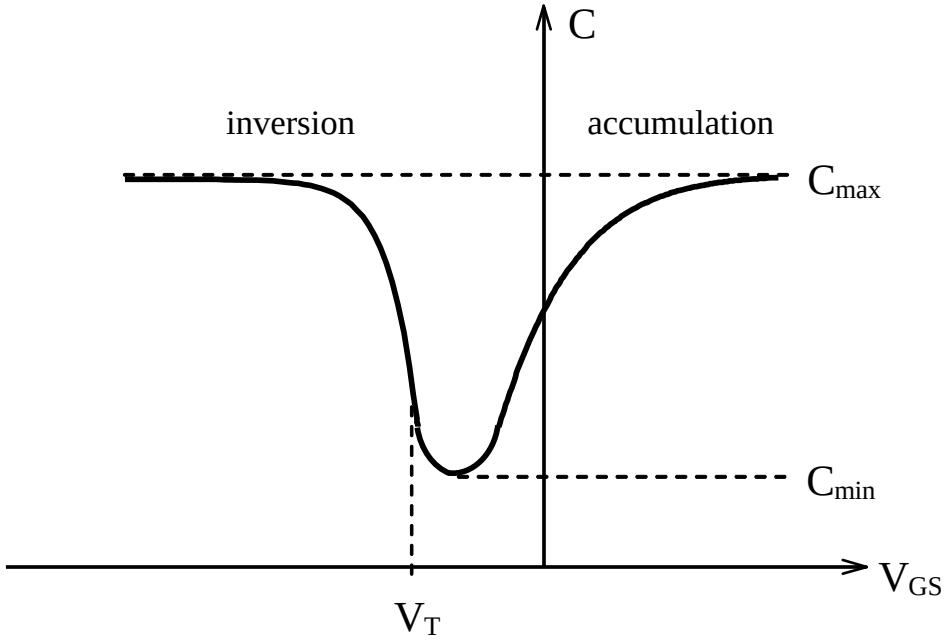
$$\gamma = (C_{\max} - C_{\min}) / (C_{\max} + C_{\min})$$

b) MOS varactors:

Capacity-voltage characteristic of a MOS capacitor

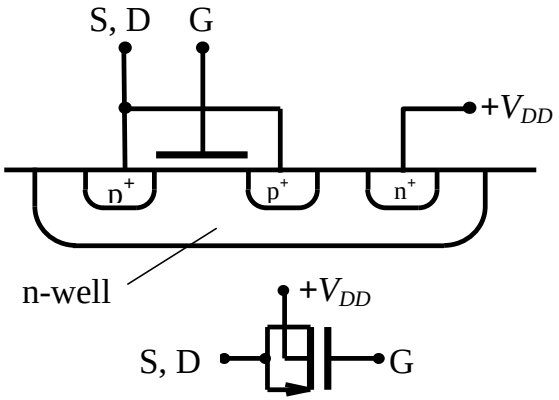


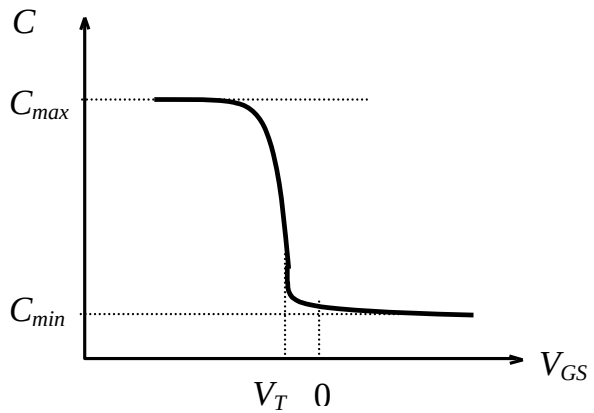
(a)



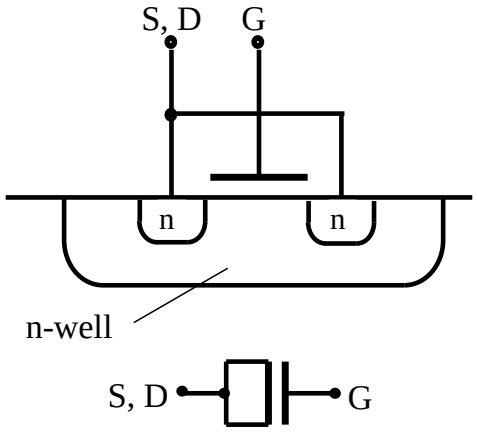
(b)

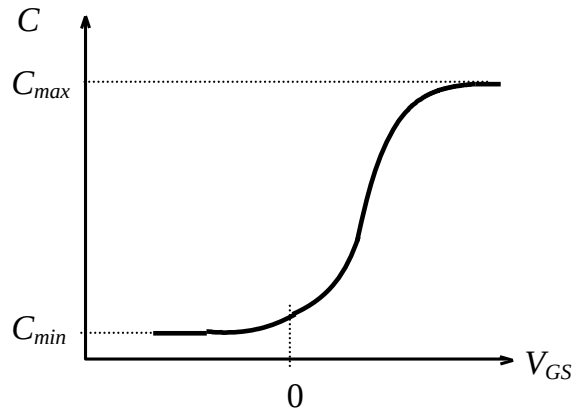
- Inversion type MOS varactor





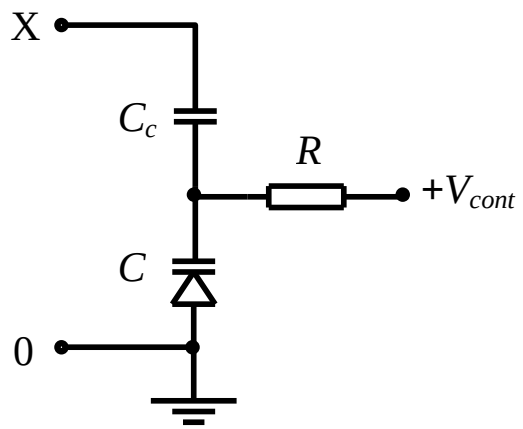
- Accumulation type MOS varactor



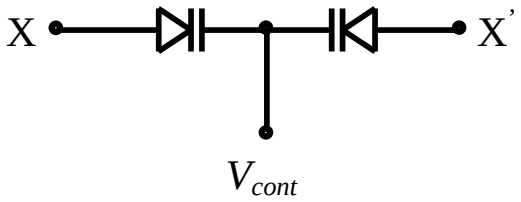


Biasing of varactors:

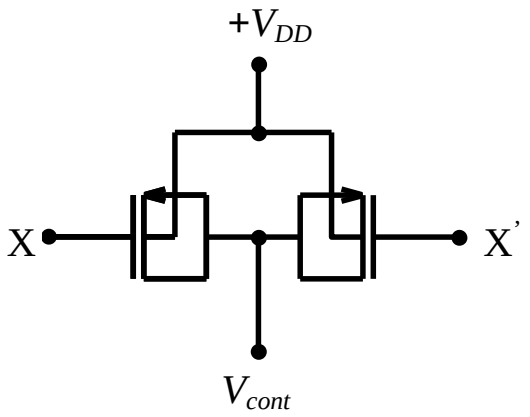
One end grounded p-n varactor



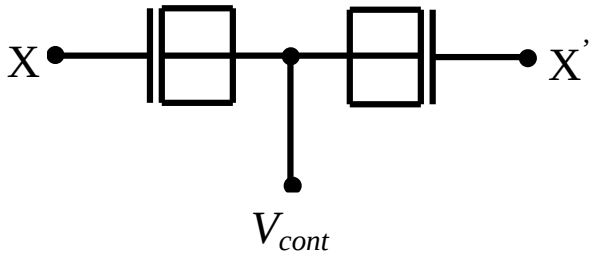
Symmetrical (floating) p-n varactor



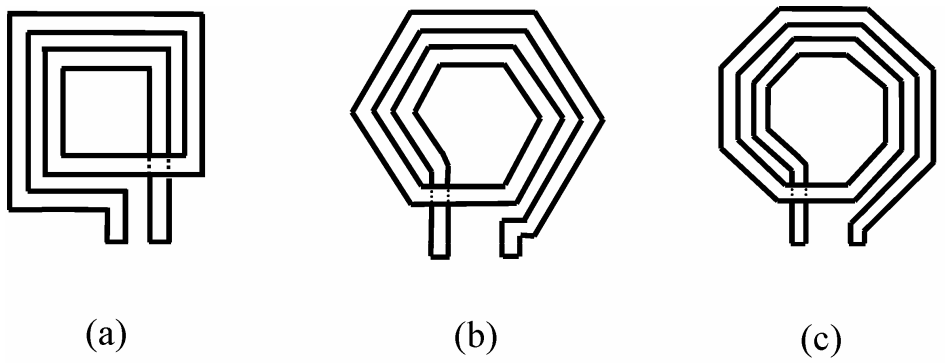
Inversion type symmetrical MOS varactor



Accumulation type symmetrical MOS varactor



Inductors:



(a) (b) (c)

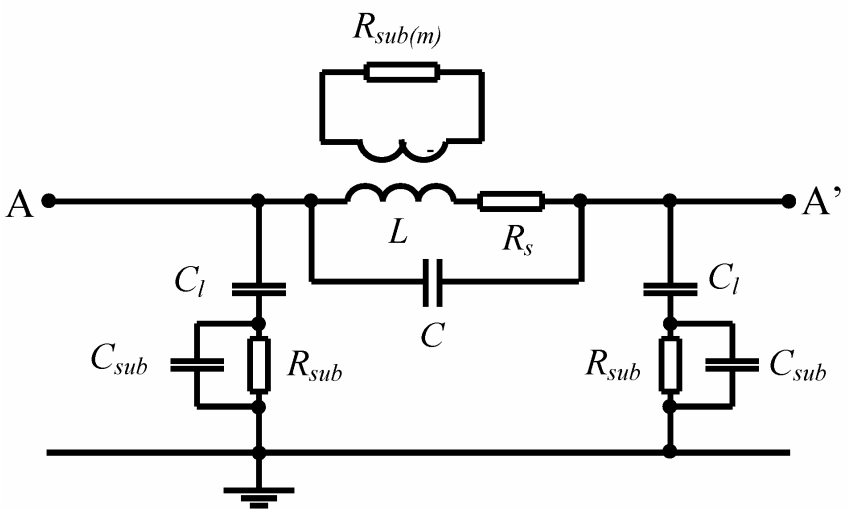
Form	K_1	K_2
Square	2.34	2.75
Hexagon.	2.33	3.82
Octagon.	2.25	3.55

Modified Wheeler formula:

$$L = K_1 \mu_0 \frac{n^2 d_{avg}}{1 + K_2 \rho}$$

$$d_{avg} = \frac{d_{out} + d_{in}}{2} \qquad \rho = \frac{(d_{out} - d_{in})}{(d_{out} + d_{in})}$$

Equivalent circuit of an on-chip inductor:



R_s : Resistance of the metal stripe (skin-effect included)

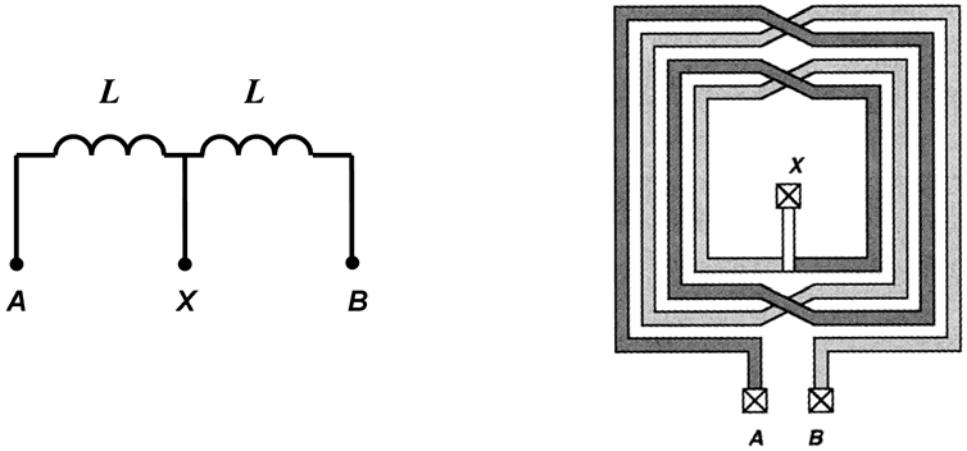
C : Parasitic capacitance between terminals

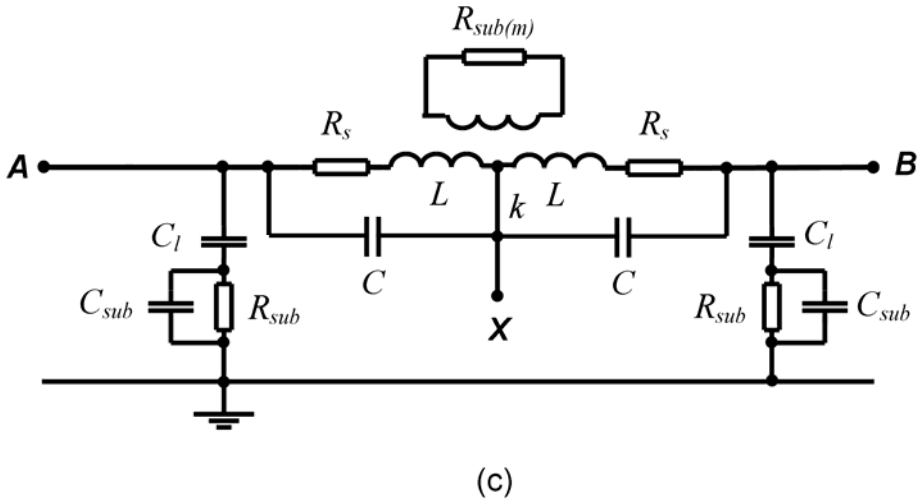
C_1 : Capacitors representing the distributed strip-to-substrate capacitance

R_{sub} : Series resistance of the terminal-substrate capacitor

$R_{sub(m)}$: Resistance representing the losses owing to the magnetically induced currents in the substrate

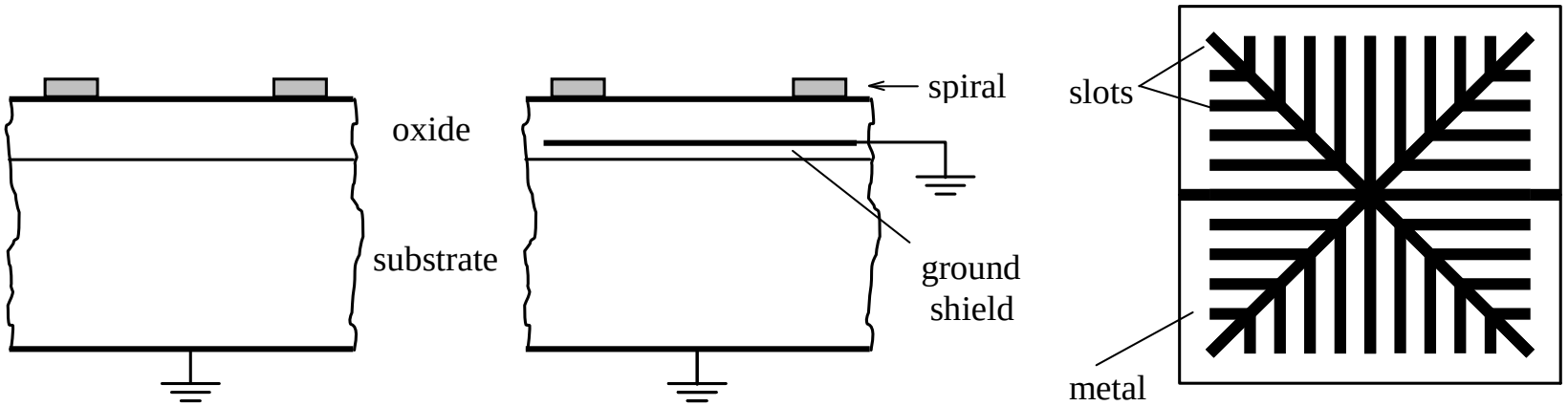
The symmetrical (center-tapped) on-chip inductor:



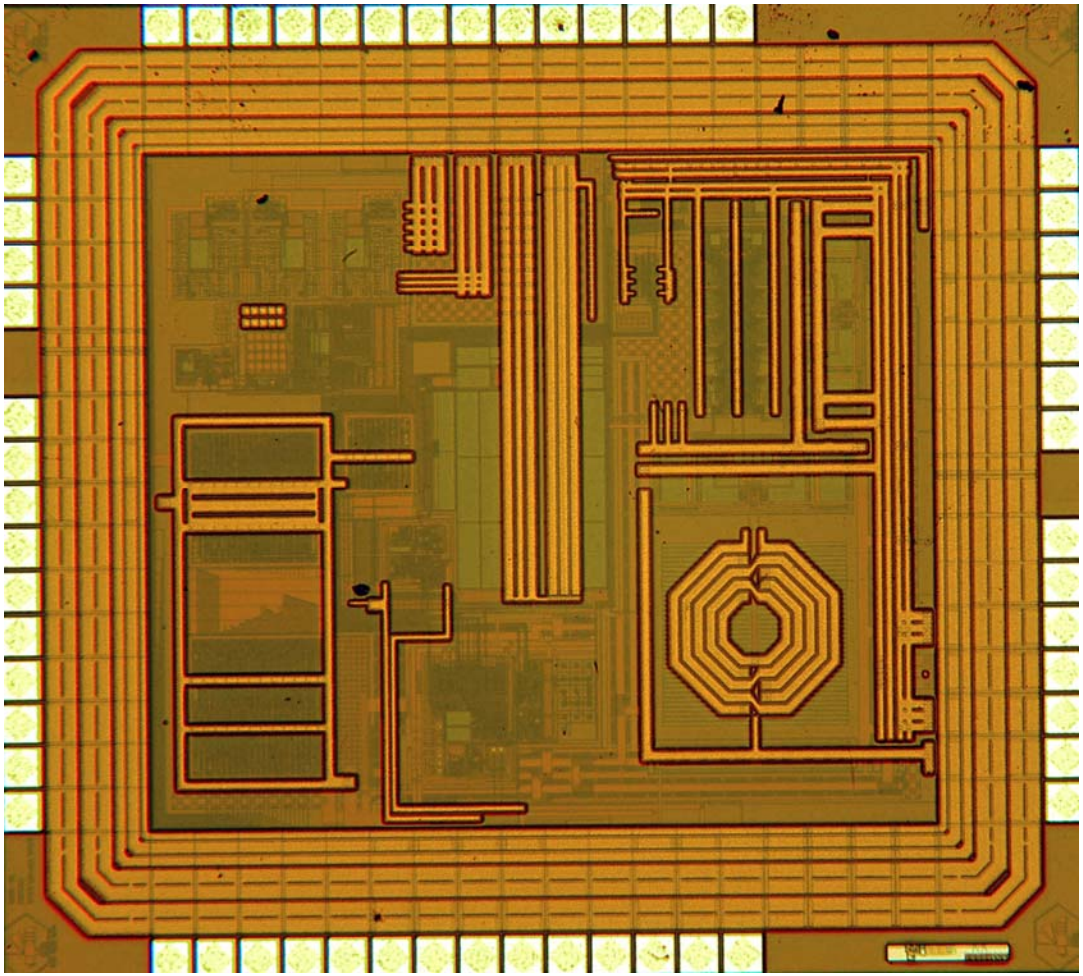


$$L_{AB} = 2L(1+k)$$

Ground-shield to decrease the losses owing to R_{sub}

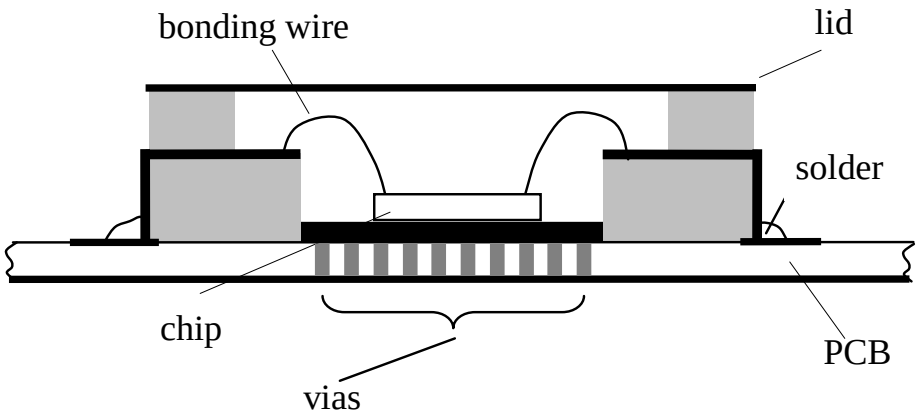


Package related problems



A typical RF-IC chip

Cross-section of a typical RF-IC package

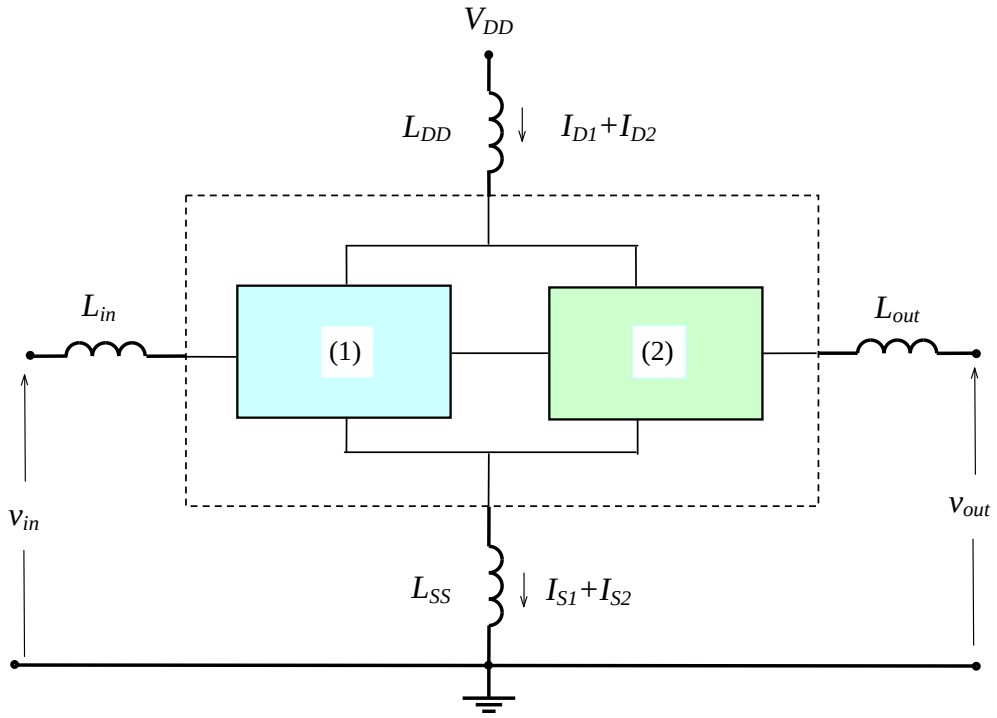


Bonding wires (Al or Au)

Typical diameter 25 μm

Parasitic inductance: ≈ 1 nH/mm

To parallel the bonding wires or use ribbon instead of wire reduces the inductance.



Negative effects of bonding wire inductances:

L_{in} , L_{out} : Resonance with C_{in} and C_{out}

L_{SS} : Feedback from output to input and noise injection

L_{DD} : Change of V_{DD} (can be reduced with an on chip by-pass capacitor)

(Since in differential circuits I_S and I_D do not contain any signal component, L_{SS} and L_{DD} related problems are minimized!)

I/O PADS

- Pad types
  - V_{DD} / GND
  - Output
  - Input
  - Bidirectional
  - Analog

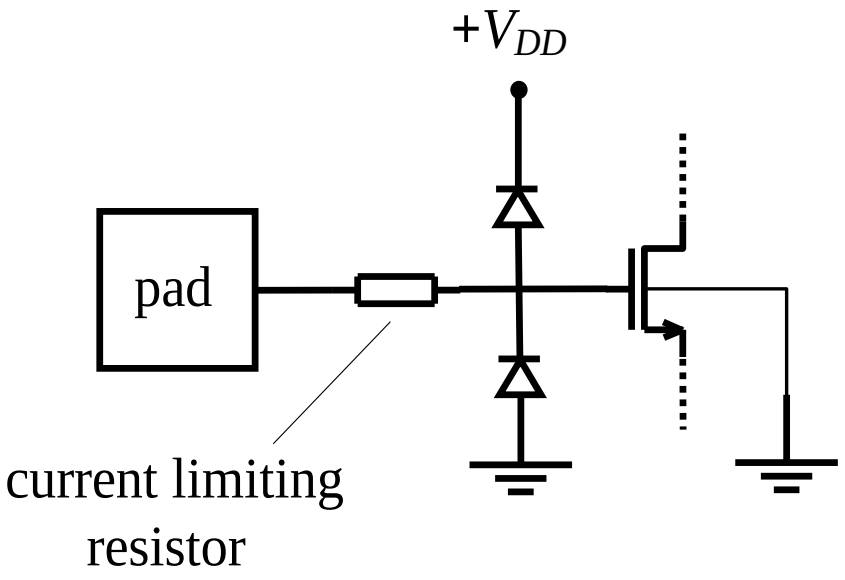
Analog pads pass analog voltages directly in or out of chip

- No buffering
- Protection circuits must not distort voltages

ESD Protection

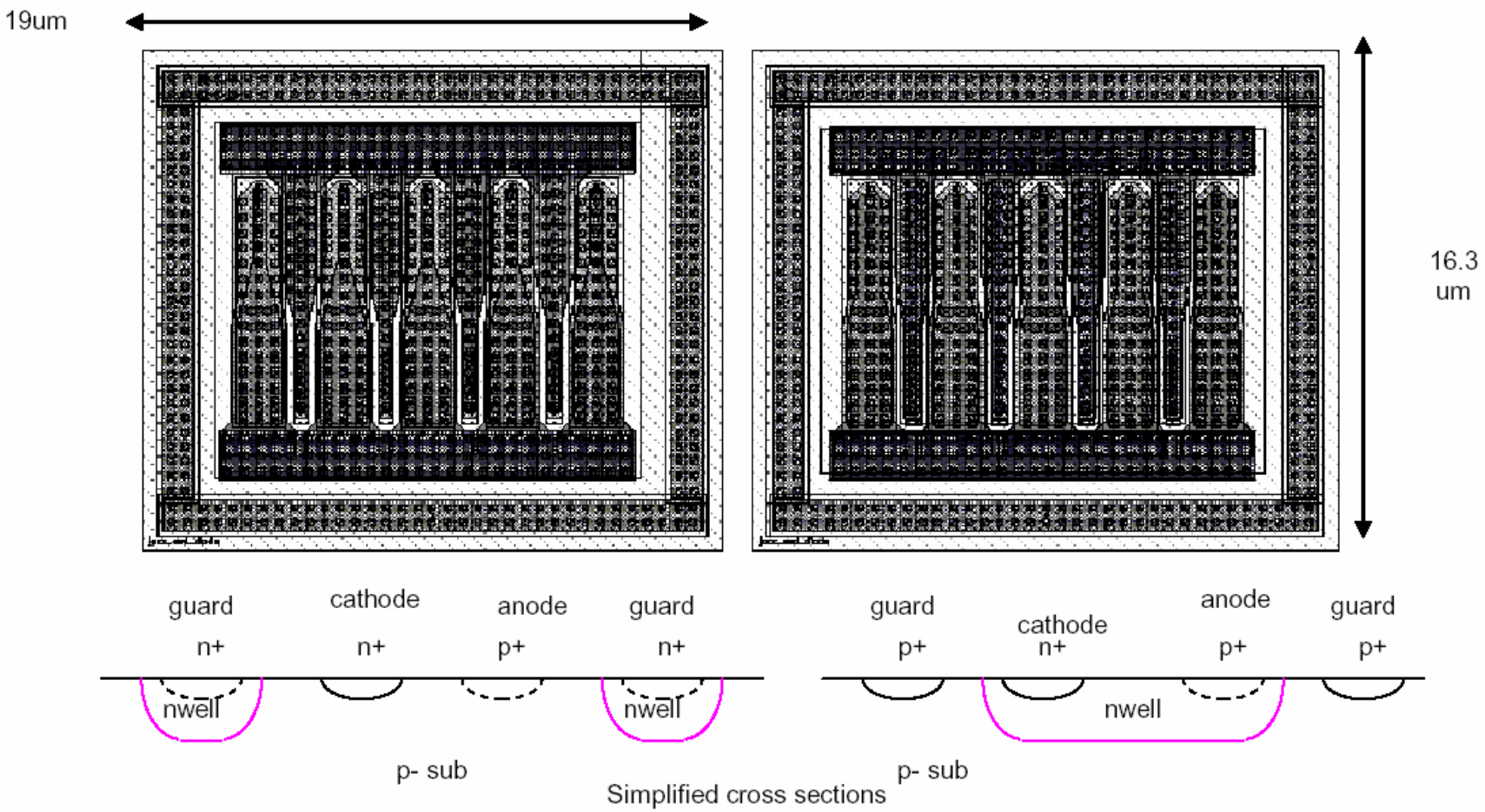
- Static electricity builds up on human body
  - Shock delivered to a chip can puncture thin gates
  - Must dissipate this energy in protection circuits before it reaches the gates

The basic ESD protection circuit with a current limiting resistor and diode clamps



Typical large-area ESD protection diode structures

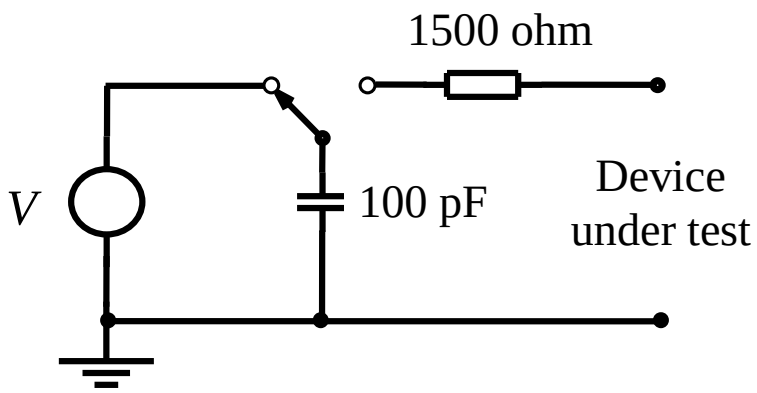
- High current carrying and power dissipation capability
- Parasitic capacitance: as low as possible



Simplified cross sections

- ESD testing

Human body model to simulate the ESD hazard when a person touches to a device.



V typically 1000 V DC