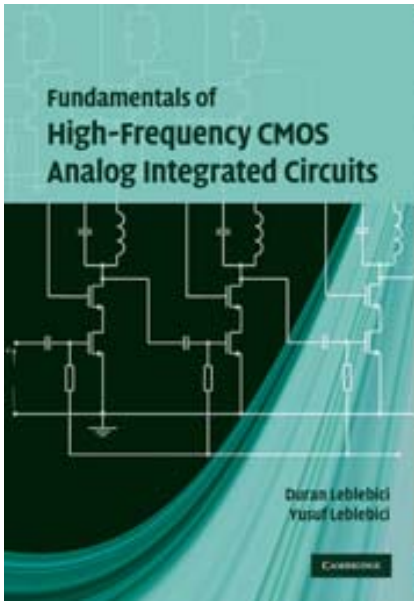

Fundamentals of High-Frequency CMOS Analog Integrated Circuits

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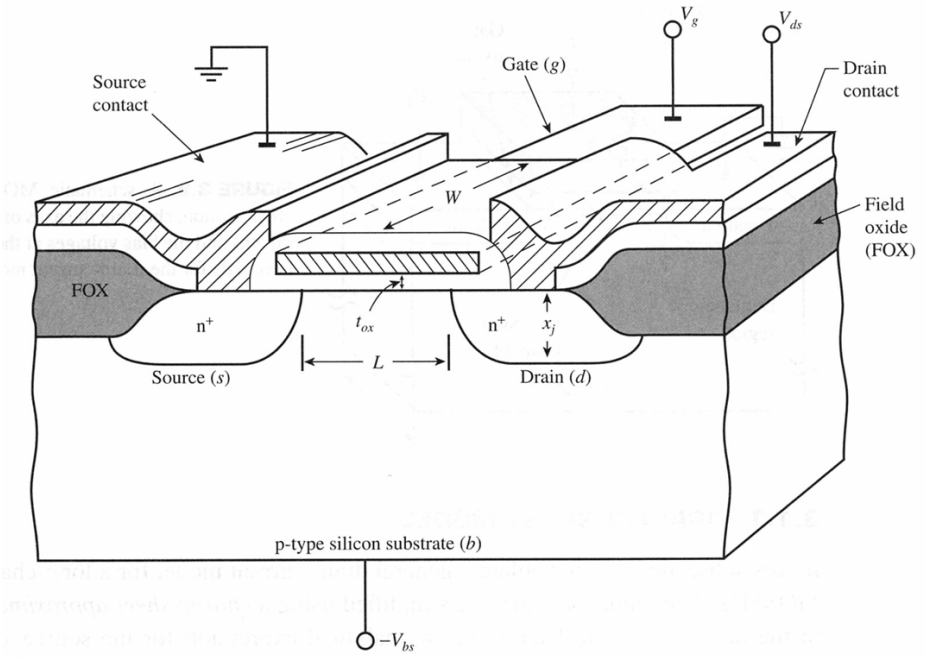
Yusuf Leblebici

Chapter 1

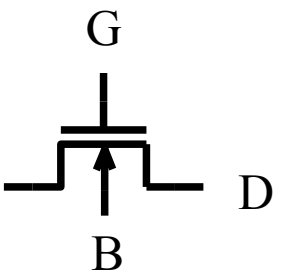
Components of Analog CMOS Integrated Circuits (MOS Transistor)

MOS TRANSISTOR

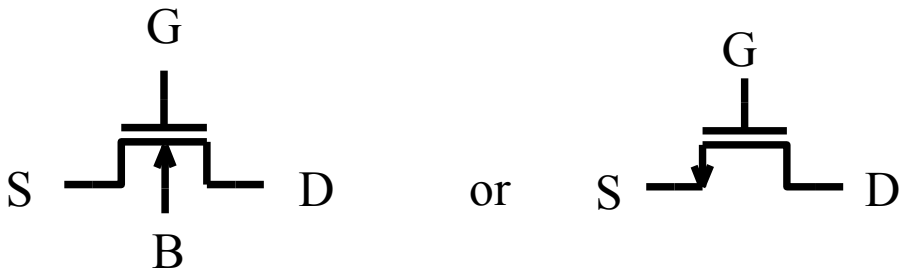
Structure of an NMOS transistor



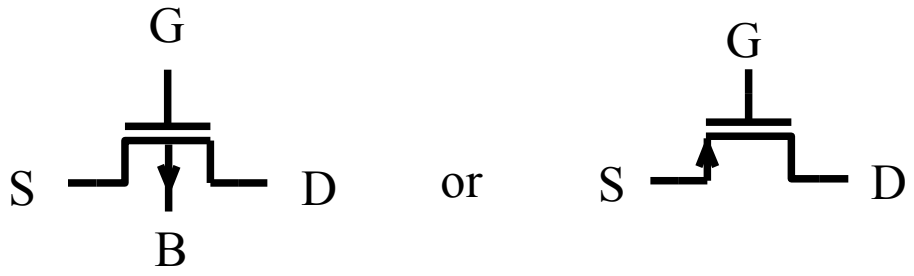
Symbol:



Symbols for NMOS transistor:



Symbols for PMOS transistor:



Parameters of the most basic model of a MOS transistor

-the threshold voltage of the transistor, $V_T \quad [\mathrm{V}]$

-the mobility of electrons (or holes), $\mu \left[\mathrm{cm}^2 / \mathrm{V.s}\right]$

-the gate capacitance per unit area, $C_{ox} \left[\mathrm{F} / \mathrm{cm}^2\right]$

-the aspect ratio of the transistor, (W / L)

-the gate-length modulation coefficient, $\lambda \left[\mathrm{V}^{-1}\right]$

- The threshold voltage, V_T is the gate-source voltage that is assumed the drain current starts to flow.

- A gate-source voltage equal to V_T inverts the channel region to a carrier density equal to the carrier density of the bulk.

- The gate voltages higher than V_T correspond to the strong inversion.

- The gate voltages smaller than V_T correspond to the weak inversion (or sub-threshold).

- The mechanisms governing the current flow are completely different for strong inversion and weak inversion.

The threshold voltage

$$V_T = \Phi_{MS} - \frac{Q_{tot}}{C_{ox}} - \frac{Q_s}{C_{ox}} - 2\Phi_F - q\frac{D_I}{C_{ox}}$$

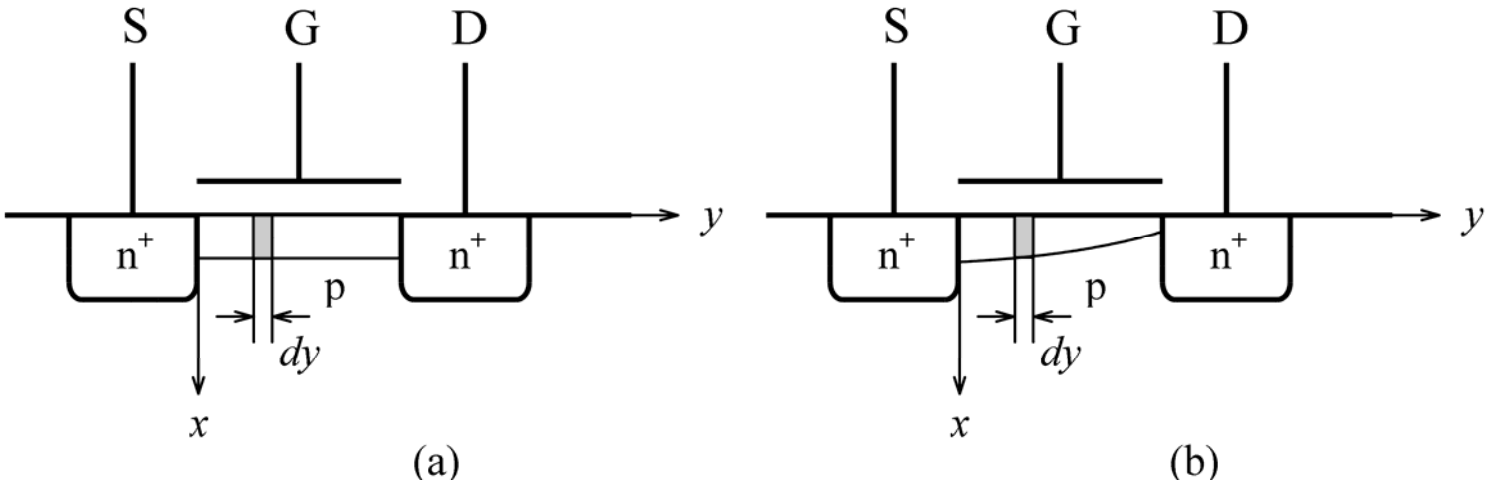
- Φ_{MS} : Gate-substrate work function difference $\left[\text{V}\right]$
- Q_s : Depletion charge density $\left[\text{coulomb} / \text{cm}^2\right]$
- Q_{tot} : Total oxide charge density $\left[\text{coulomb/cm}^2\right]$
- Φ_F : Fermi potential of the substrate $\left[\text{V}\right]$
- D_I : Threshold adjustment implant dose $\left[\text{cm}^{-2}\right]$

For analog CMOS: $V_T \succ 0$ for NMOS

$V_T \prec 0$ for PMOS

Voltage-current relations of a MOS transistor

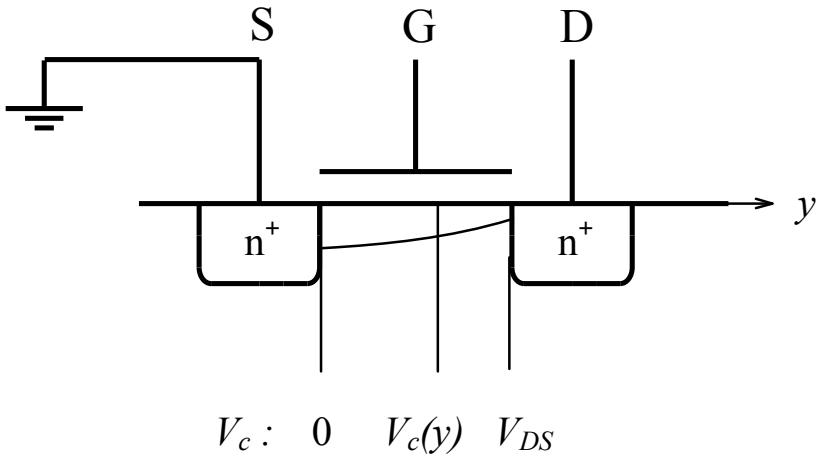
(Based on realistic inversion channel profile)



Inversion channel profiles of an NMOS transistor:

(a) For $V_{GS} \succ V_T$ and $V_{DS} = 0$

(b) For $V_{GS} \succ V_T$ and $V_{DS} \succ 0$



$$V_{eff}(0) = (V_{GS}\text{-}V_T)$$
$$V_{eff}(y) = (V_{GS}\text{-}V_c)\text{-}V_T$$
$$V_{eff}(L) = (V_{GS}\text{-}V_{DS})\text{-}V_T$$

Inversion charge density : $Q_i(y) = -C_{ox} \times V_{eff}(y)$ [coulomb/cm^2]

(Note that C_{ox} is in farad/cm^2)

Inversion charge in a $(W \times dy)$ channel element:

$$d\bar{Q}_i(y) = -C_{ox}W[(V_{GS} - V_T) - V_c(y)]dy \quad \text{[coulomb]}$$

The drain current: $I_D = \dfrac{d\bar{Q}_i(y)}{dt} = \dfrac{d\bar{Q}_i(y)}{dy / v(y)}$ (constant along the channel!)

$$v(y) = \mu_n E(y) = -\mu_n \frac{dV_c(y)}{dy}$$

$$I_D = \mu_n C_{ox} W[(V_{GS} - V_T) - V_c(y)] \frac{dV_c(y)}{dy}$$

$$\frac{I_D}{\mu_n C_{ox} W} dy = [(V_{GS} - V_T) - V_c(y)] dV_c(y)$$

After integration from 0 to y:

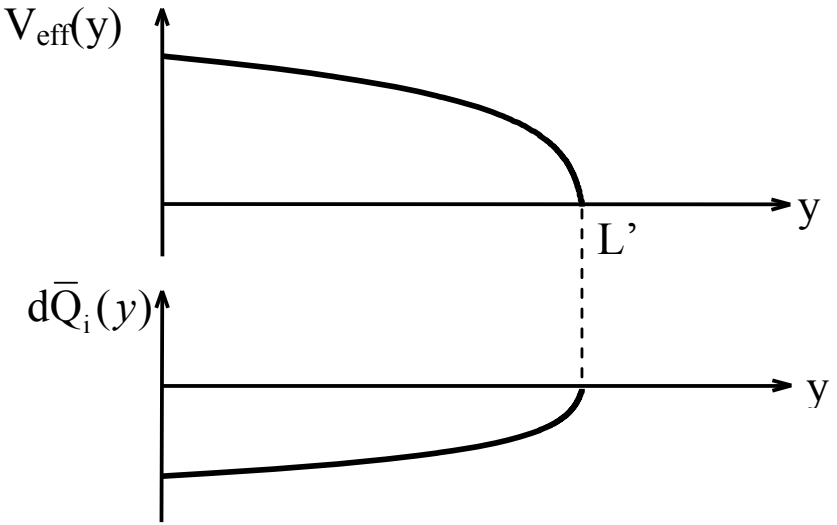
$$\frac{I_D}{\mu_n C_{ox} W} y = (V_{GS} - V_T) V_c(y) - \frac{1}{2} V_c^2(y)$$

$$V_c(y) = (V_{GS} - V_T) \mp \sqrt{(V_{GS} - V_T)^2 - \frac{2I_D}{\mu_n C_{ox} W} y}$$

Variation of the effective channel voltage as a function of y :

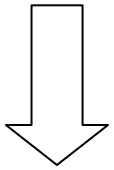
$$V_{eff}(y) = (V_{GS} - V_T) - V_c(y) = (V_{GS} - V_T)\sqrt{1 - \frac{2I_D}{\mu_n C_{ox} W (V_{GS} - V_T)^2}\, y}$$

$$V_{eff}(0) = (V_{GS} - V_T) \quad \Rightarrow \quad V_{eff}(L') = 0 \; ; \quad L' = \frac{\mu_n C_{ox} W (V_{GS} - V_T)^2}{2I_D}$$



Special cases:

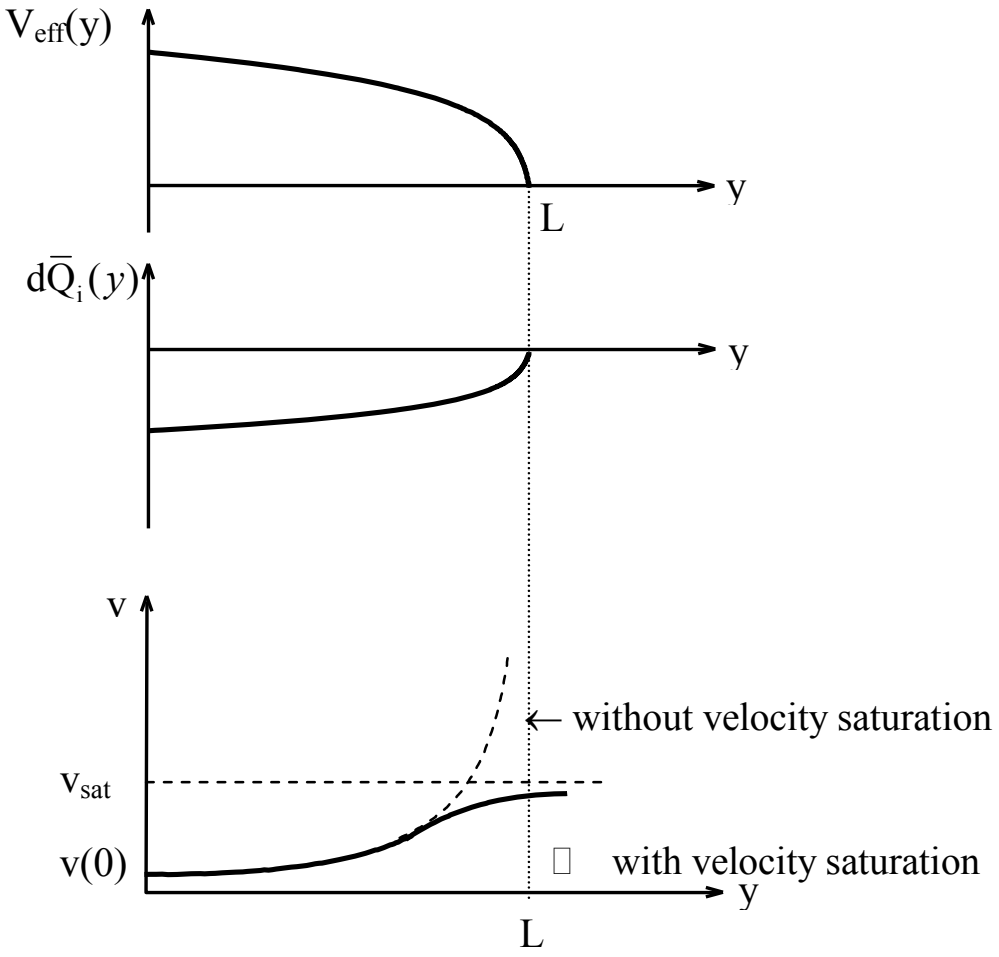
a) $L = L'$; $V_{eff}(L) = 0$, $V_c(L) = V_{DS} = (V_{GS} - V_T)$



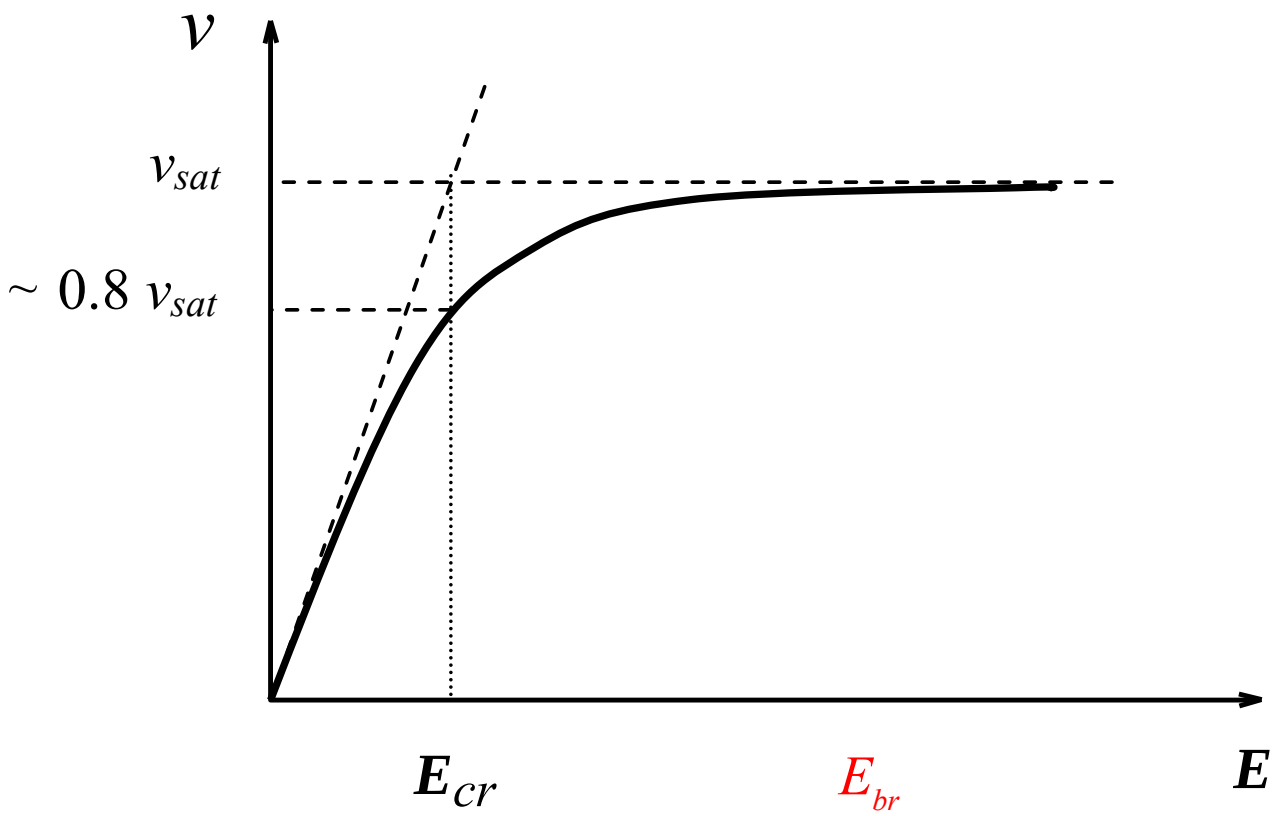
$$I_D = I_{Dsat} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_T)^2$$

(The drain current corresponding to the on – set of saturation)

At the on-set of the saturation, variations of the effective channel voltage, inversion layer charge density and the velocity of electrons along the channel



The velocity saturation of charge carriers



$$E \square \; E_{cr} \quad ; \quad \mu = \frac{dv}{dE} \cong \frac{v_{sat}}{E_{cr}}$$

Remark: The field strength must not exceed the break-down field strength $E_{br} \cong 3 \times 10^5$ V/cm, to maintain the integrity of the crystal.

b) $L \prec L'$; $V_c(L) = V_{DS} \prec (V_{GS} - V_T)$

$$\Downarrow$$

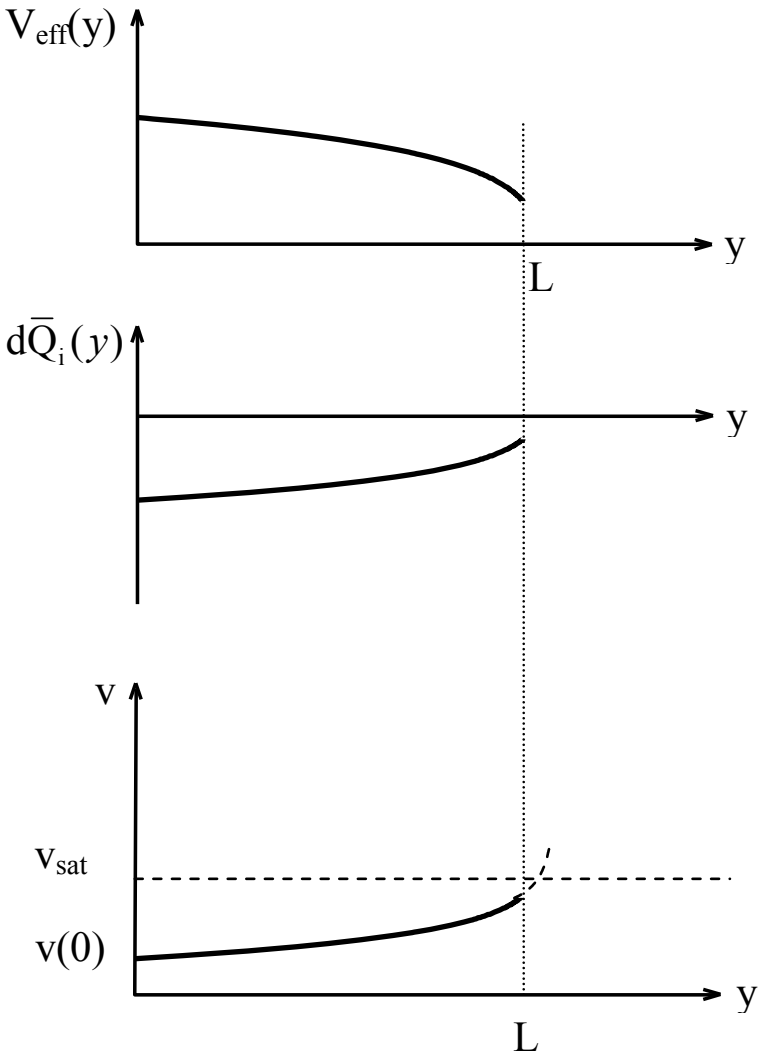
$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

(The drain current in the resistive -or linear- region)

V_{DS} □ $(V_{GS} - V_T)$ $\Longrightarrow$ $I_D \cong \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)V_{DS}$

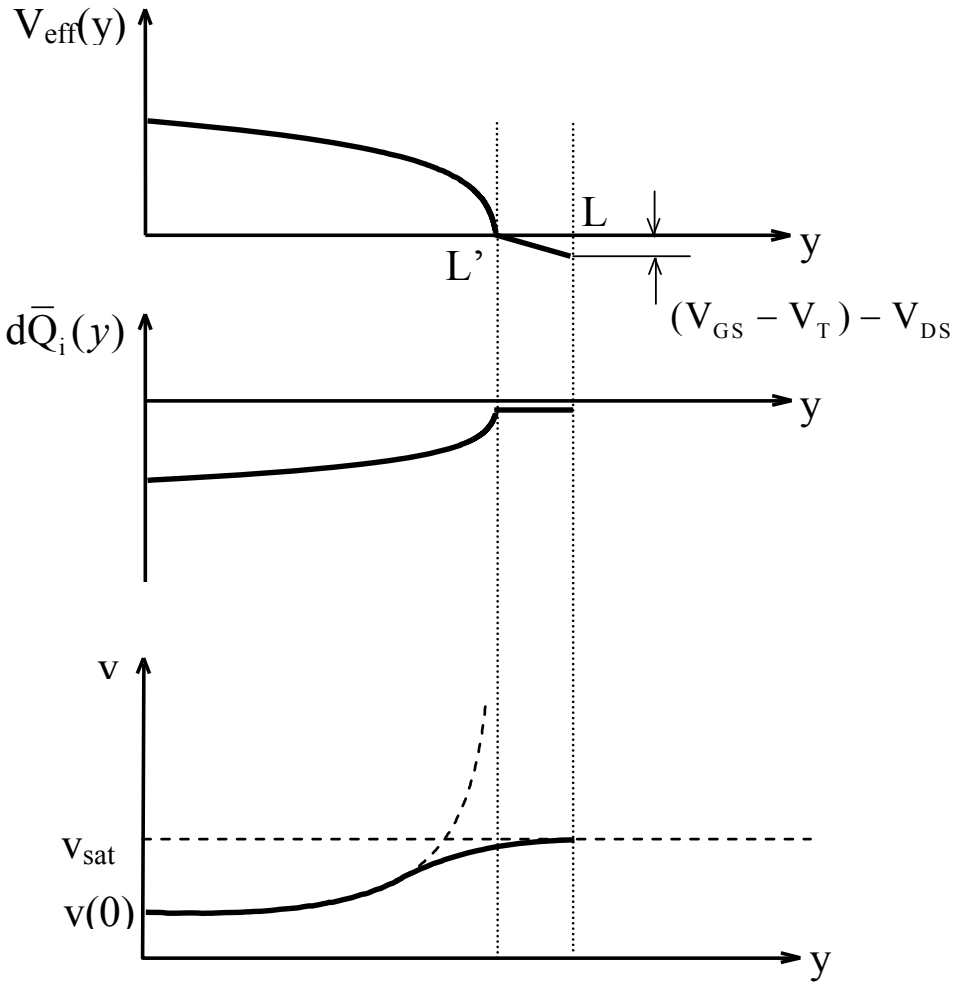
(The drain current at the beginning of the resistive region)

In the resistive region, variations of the effective channel voltage, inversion layer charge density and the velocity of electrons along the channel



In the saturation region, variations of the effective channel voltage, inversion layer charge density and the velocity of electrons along the channel

c) $L \succ L'$; $V_c(L) = V_{DS} \succ (V_{GS} - V_T)$



$$\Delta L = (L - L') = \frac{(V_{GS} - V_T) - V_{DS}}{E_{sat}}$$

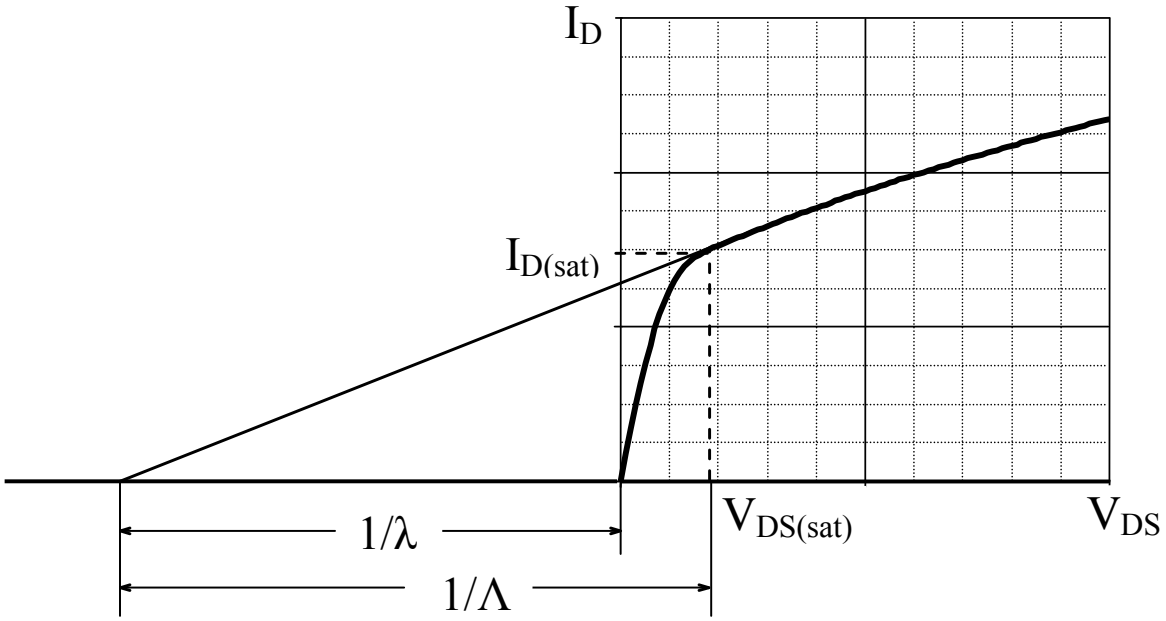
$$I_{Dsat} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_T)^2$$

$$\frac{dI_D}{dV_{DS}} = \frac{dI_D}{dL} \times \frac{dL}{dV_{DS}} = \left(-I_D \frac{1}{L}\right) \times \left(-\frac{1}{E_{sat}}\right) = \lambda I_D \quad ; \quad \lambda = \frac{1}{L E_{sat}}$$

$$I_D = I_{Dsat} + g_{ds}(V_{DS} - V_{DS(sat)}) = I_{Dsat} + g_{ds}[V_{DS} - (V_{GS} - V_T)]$$

$$I_D = I_{Dsat}\frac{1}{1 - \lambda[V_{DS} - (V_{GS} - V_T)]} \cong I_{Dsat}\{1 + \lambda[V_{DS} - (V_{GS} - V_T)]\}$$

(Drain current in the saturation region)

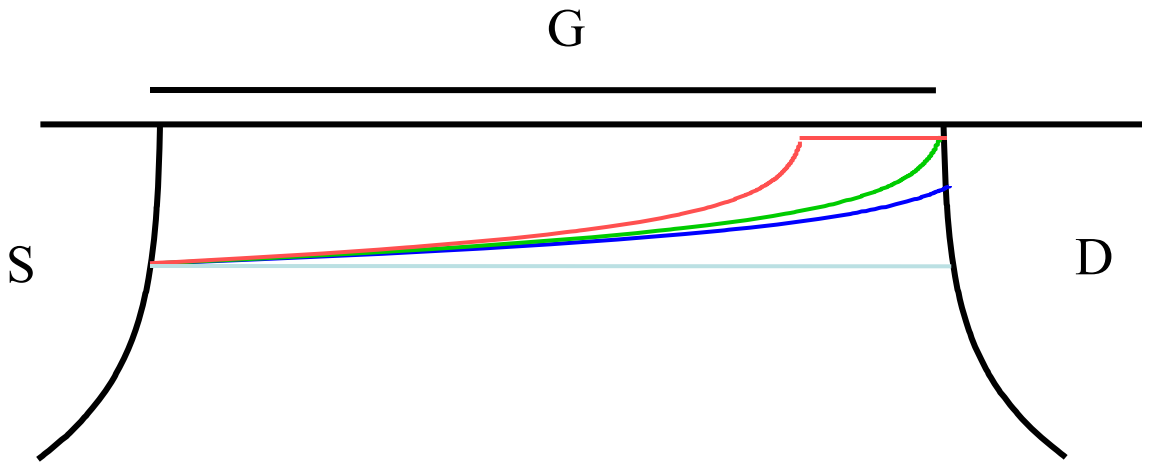


$$I_D = I_{Dsat}\frac{1+\lambda V_{DS}}{1+\lambda(V_{GS}-V_T)}$$

(The drain current in the saturation region in terms of the λ parameter)

$$V_{DS} \square (V_{GS}-V_T) \quad \Rightarrow \quad I_D = I_{Dsat}(1+\lambda V_{DS})$$

Summary:



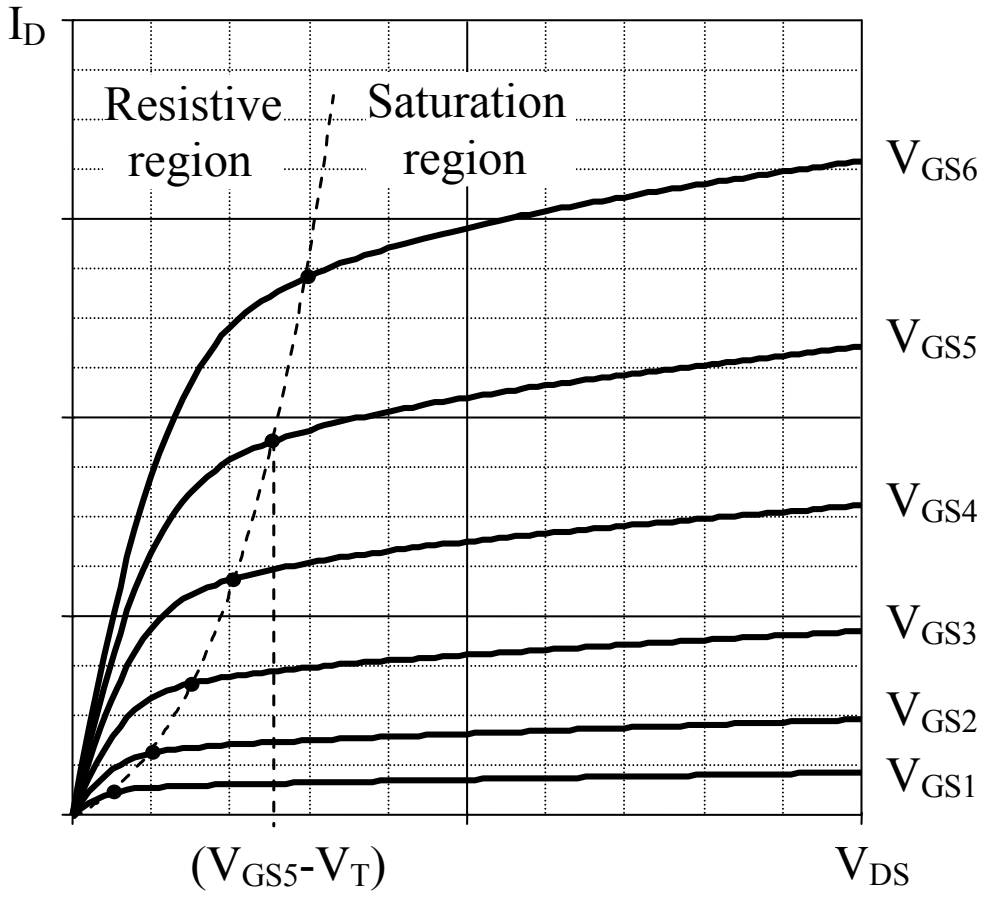
$$I_D \cong \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)V_{DS} \quad \text{for} \quad V_{DS} \ll (V_{GS} - V_T)$$

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right] \quad \text{for} \quad V_{DS} \prec (V_{GS} - V_T)$$

$$I_D = I_{Dsat} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)^2 \quad \text{for} \quad V_{DS} = (V_{GS} - V_T)$$

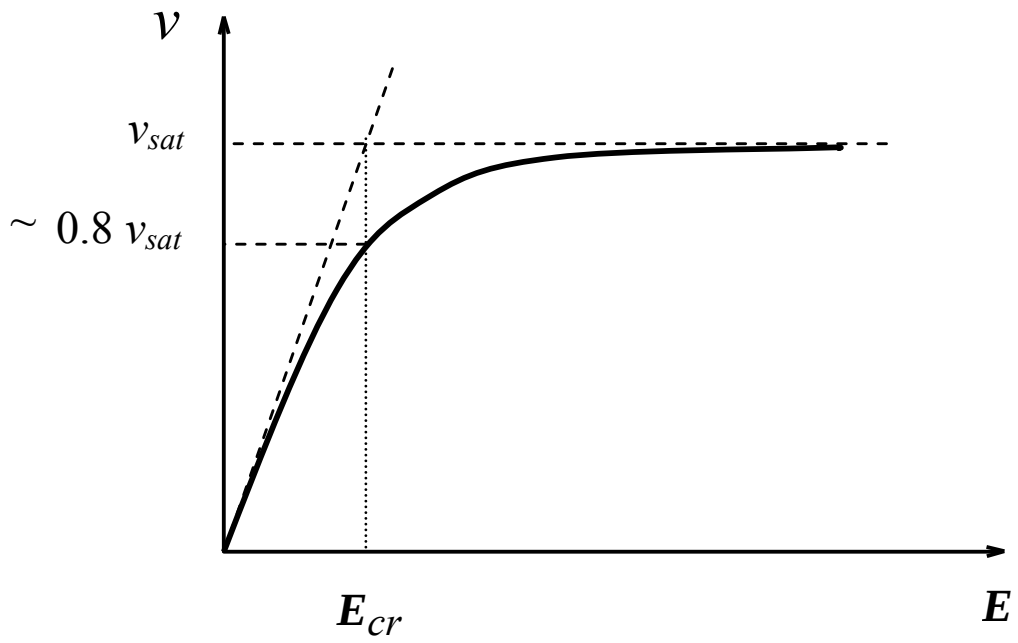
$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)^2 \frac{1 + \lambda V_{DS}}{1 + \lambda(V_{GS} - V_T)} \quad \text{for} \quad V_{DS} \succ (V_{GS} - V_T)$$

The output characteristics of a NMOS transistor



Voltage-current relations of a MOS transistor

operating in the velocity saturation region



Saturation velocities of carriers:

	In the bulk silicon	In the inversion layer
For electrons:	$v_{sat} \approx 10^7$ cm/s	$v_{sat} \approx 6.5\times10^6$ cm/s
For holes:	$v_{sat} \approx 8\times10^6$ cm/s	$v_{sat} \approx 5.8\times10^6$ cm/s

Assumptions:

- Velocity saturation along the channel,
- Inversion charge density is constant along the channel.

$$\bar{Q}_i = WLC_{ox}(V_{GS} - V_T)$$

$$I_D = \frac{\bar{Q}_i}{t} = \frac{\bar{Q}_i}{(L / v_{sat})}$$

$$I_D = WC_{ox}(V_{GS} - V_T)v_{sat}$$

More realistic: $I_D = kWC_{ox}(V_{GS} - V_T)v_{sat}$, $k \cong 0.8$

(Drain current under velocity saturation)

On-set of the velocity saturation regime

$$I_D = WC_{ox}(V_{GS} - V_T)v_{sat} \Rightarrow I_D = WC_{ox}(V_{GS} - V_T)(\mu_n E_{crit(n)})$$

At the on-set of the velocity saturation:

$$E_{(crit-n)} = \frac{V_{DS(v-sat)}}{L} = \frac{v_{sat}}{\mu_n}$$

$$\Downarrow$$

$$V_{DS(v-sat)} = \frac{L\,v_{sat}}{\mu_n}$$

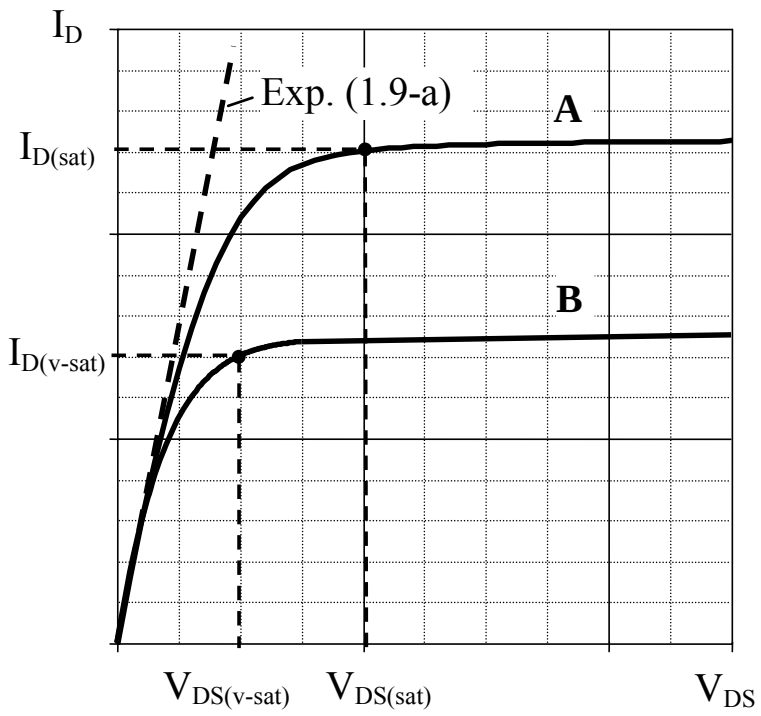
1st Condition for velocity saturation:

$$V_{DS(sat)} \succ \frac{L\,v_{sat}}{\mu_n}$$

Comparison of the normal saturation and velocity saturation voltages:

$$\text{For } E \gg E_{crit(n)} \;;\; v = \mu_n \frac{V_{DS}}{L} \;\Rightarrow\; I_D = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)V_{DS}$$

(same as the drain current of a non-velocity saturated transistor in the resistive region)



$$V_{DS(v-sat)} \prec V_{DS(sat)} \;,$$

$$V_{DS(v-sat)} \prec (V_{GS} - V_T)$$

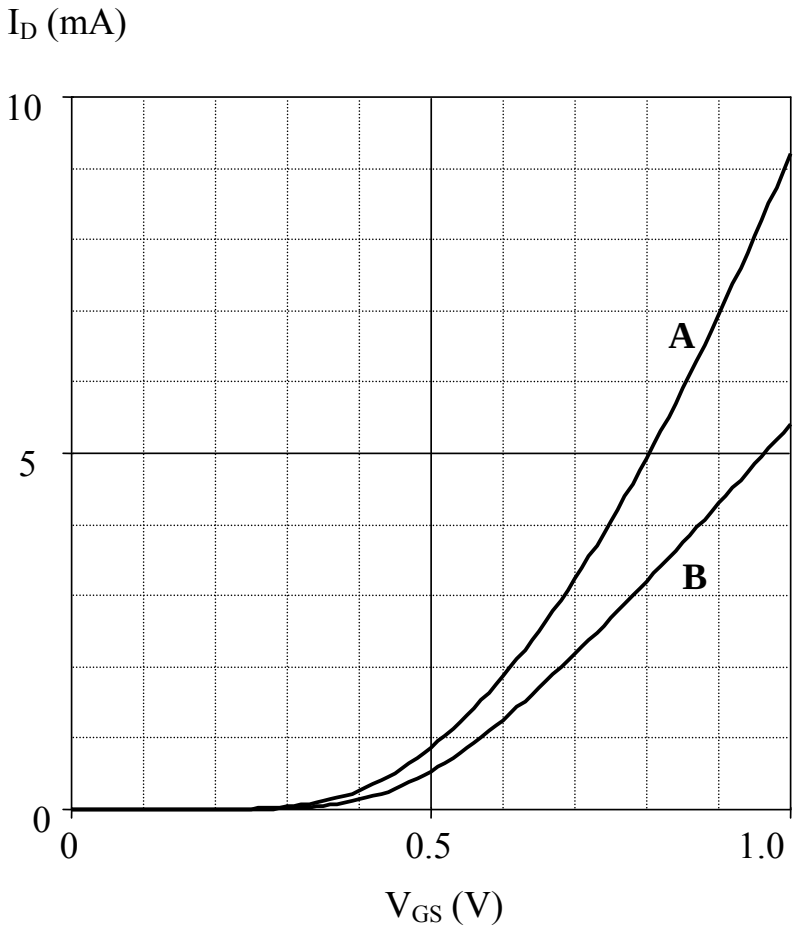
$$\frac{Lv_{sat}}{\mu_n} \prec (V_{GS} - V_T)$$

$$\Downarrow$$

$$L \prec \frac{\mu_n (V_{GS} - V_T)}{v_{sat}}$$

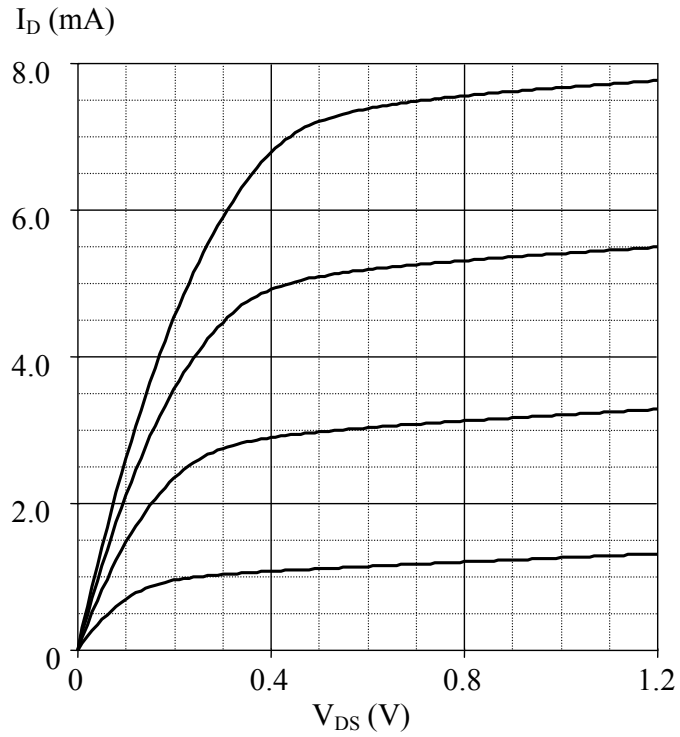
(2. Condition for velocity saturation)

Comparison of $I_D = f(V_{GS})$ curves of non-velocity saturated, and velocity saturated transistors

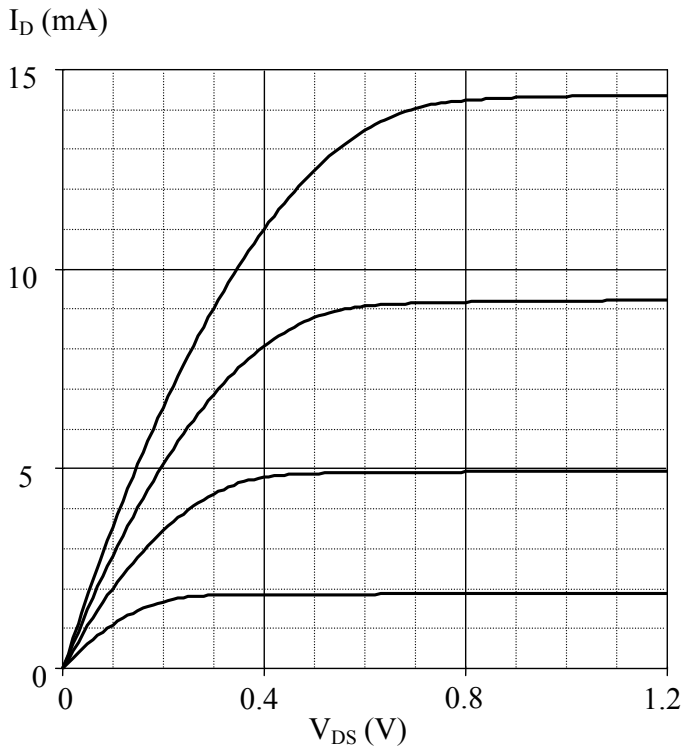


(A) 130μm/1.3μm transistor, (B) 13μm/0.13μm transistor

Comparison of $I_D = f(V_{GS})$ curves of non-velocity saturated, and velocity saturated transistors



13μm/0.13μm transistor



130μm/1.3μm transistor

The transconductance (g_m) in saturation region:

- For a non-velocity saturated transistor:

$$g_m = \frac{dI_D}{dV_{GS}} = \mu C_{ox} \frac{W}{L}(V_{GS} - V_T) = \sqrt{2\mu C_{ox} \frac{W}{L} I_D}$$

- For a velocity saturated transistor:

$$g_m = \frac{dI_D}{dV_{GS}} = kWC_{ox}v_{sat}$$ (bias independent!)

Model parameters and secondary effects

- Mobility

  - Smaller in the inversion channel compared to the bulk silicon,
  - Depends on the process techniques.

Examples:

AMS035: $\mu_{n0} = 476\ \text{cm}^2 / \text{V.s}, \quad \mu_{p0} = 137\ \text{cm}^2 / \text{V.s}$

TMSC025: $\mu_{n0} = 300\ \text{cm}^2 / \text{V.s}, \quad \mu_{p0} = 78\ \text{cm}^2 / \text{V.s}$

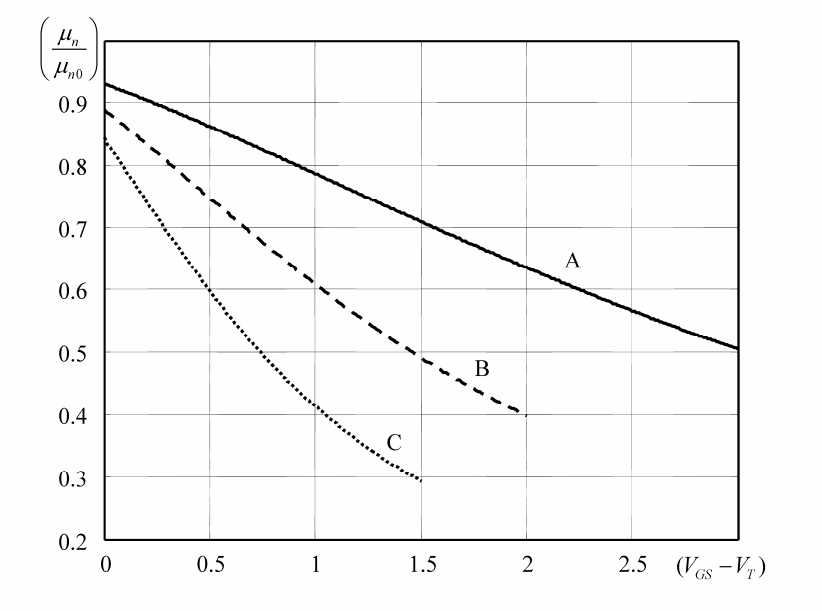
UMC018: $\mu_{n0} = 267\ \text{cm}^2 / \text{V.s}, \quad \mu_{p0} = 118\ \text{cm}^2 / \text{V.s}$

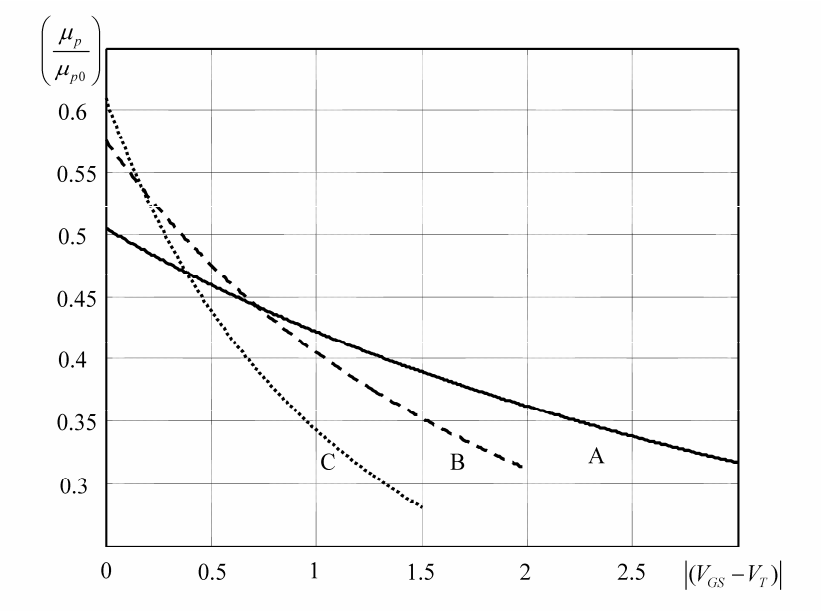
ST013: $\mu_{n0} = 312\ \text{cm}^2 / \text{V.s}, \quad \mu_{p0} = 54\ \text{cm}^2 / \text{V.s}$

- Decreases with temperature: $\mu(T) = \mu(T_{nom})\left(\frac{T}{T_{nom}}\right)^{BEX}$, $BEX \approx -1.5$

- Decreases with the transversal electric field strength:

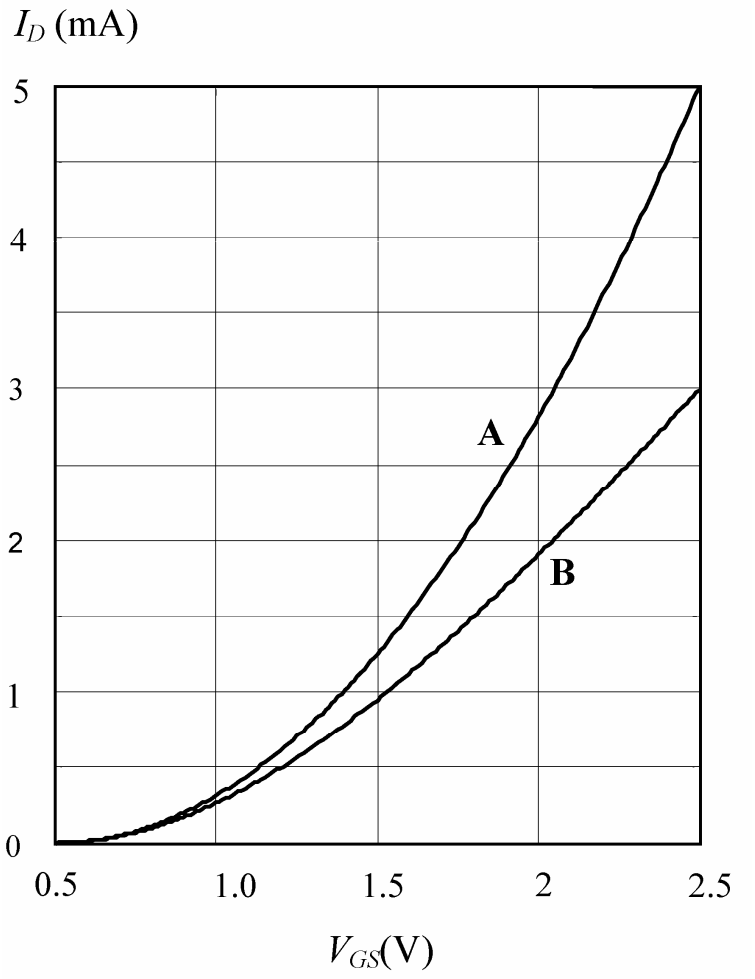
$$\mu_n = \frac{\mu_{no}}{1+\left(\frac{V_{GS}+V_T}{0.54\times T_{ox}}\right)^{1.85}} , \qquad \mu_p = \frac{\mu_{po}}{1+\left(\frac{V_{GS}+1.5\times V_T}{0.338\times T_{ox}}\right)}$$





(A) $T_{ox} = 7.5$ nm, (B) $T_{ox} = 4$ nm, (C) $T_{ox} = 2.3$ nm,

Effects of the mobility degradation on I_D and g_m



$\mu_{n0} = 500 \text{ cm}^2 / \text{Vs}$

$T_{ox} = 5 \text{ nm}$

$V_T = 0.5 \text{ V}$

$W / L = 10$

(A) degradation neglected

(B) degradation included

Oxide capacitance

$$C_{ox} = \frac{\varepsilon_0 \varepsilon_{ox}}{T_{ox}} \quad , \quad (\varepsilon_0 = 8.85 \times 10^{-14} \text{ F/cm}, \ \varepsilon_{ox} = 3.9)$$

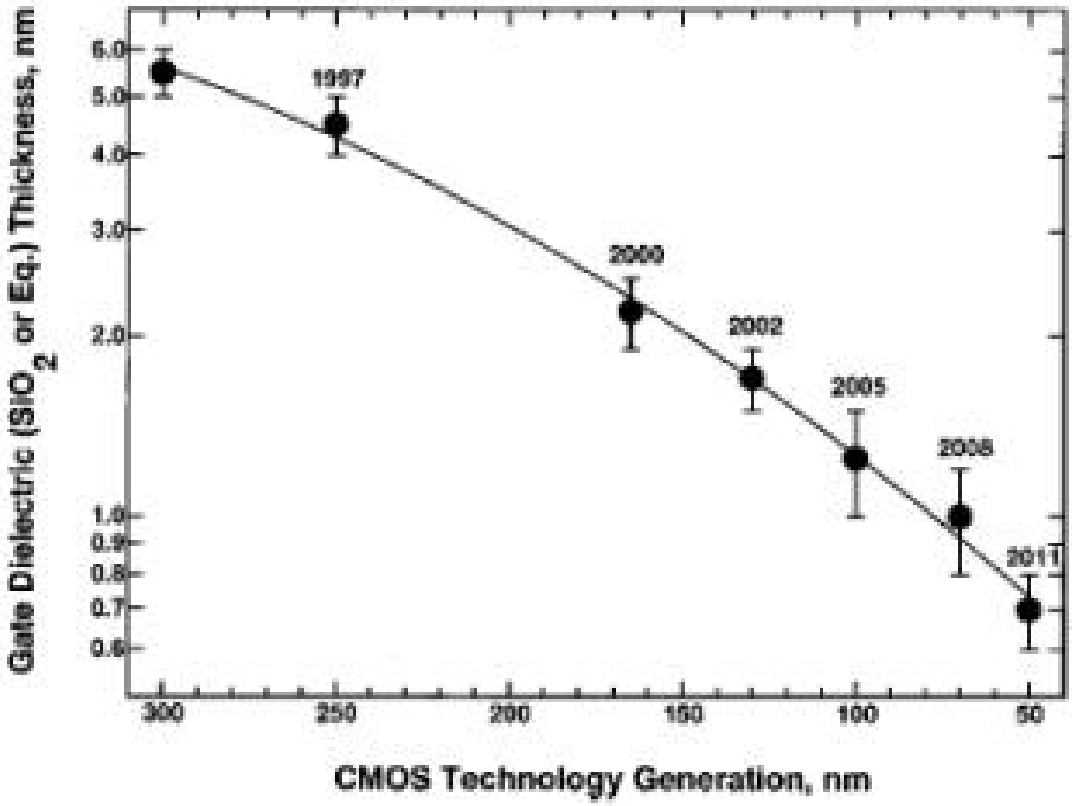
$$C_{ox} = \frac{34.5}{T_{ox}\,[\text{nm}]} \times 10^{-7} \ \left[\text{F/cm}^2\right]$$

Breakdown voltage of SiO_2 : ≈ 10 MV / cm

$\Downarrow$

≈ 1V / nm

Oxide thickness vs. minimum feature size (nm)



Examples

Technology	Tox (nm)	V_{DD} (V)
AMS 035	7.6	3.3
IHP 025	5.8	2.5
AMS 018	4.5	1.8
Lfoundry 015	3.3	1.8
UMC 90 nm	2.2	1.2
SMIC	2.3	1.2

- The threshold voltage, V_T

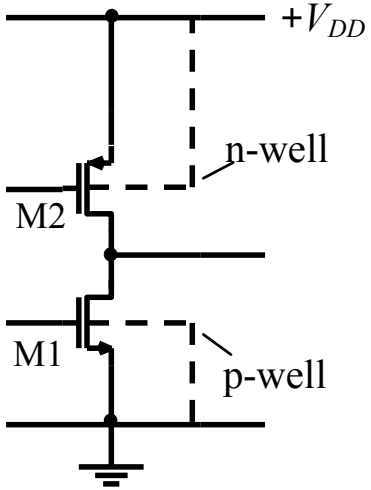
- The threshold voltage for a certain technology is given for a transistor
  - having L and W considerably larger than the minimum dimensions,
  - for no substrate bias ($V_{SB} = 0$)
  - denoted as VTO.

- For a certain technology varies with the length and width of the gate.
  - Decreases for smaller gate lengths,
  - Increases for smaller gate widths.

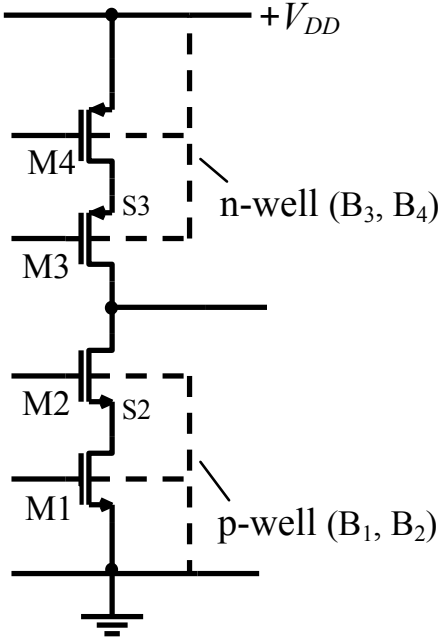
- Technology dependent; magnitude usually in the range of 0.2 to 0.5 V.

- Magnitude increases with the substrate bias.

Effects of the substrate bias ($V_{SB} \neq 0$)



$$V_{SB}(\text{M1}) = 0$$
$$V_{SB}(\text{M2}) = 0$$



$$V_{SB}(\text{M1}) = 0$$
$$V_{SB}(\text{M2}) = 0$$

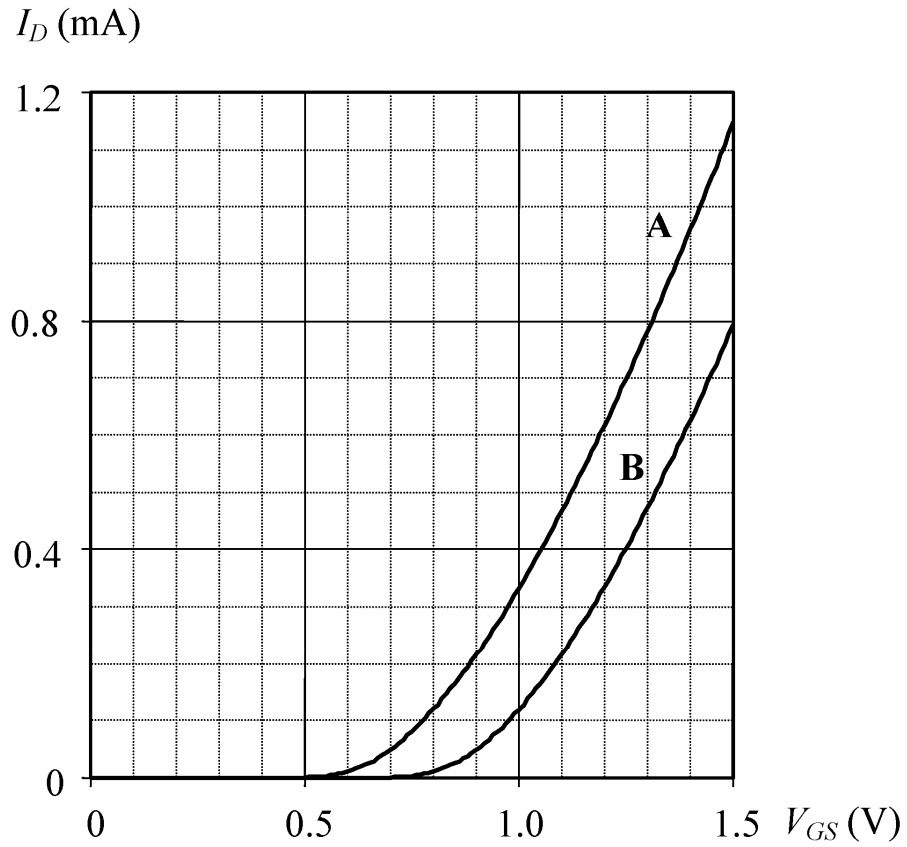
$$V_{SB}(\text{M2}) = V_{DS}(\text{M1})$$
$$V_{SB}(\text{M3}) = V_{DS}(\text{M4})$$

The value of the threshold voltage under substrate bias:

$$V_T = V_{TO} + \gamma\left(\sqrt{\left|-2\Phi_F + V_{SB}\right|} - \sqrt{\left|2\right|\Phi_F}\right)$$

$$\gamma = \frac{\sqrt{2qN_A}}{C_{ox}}$$

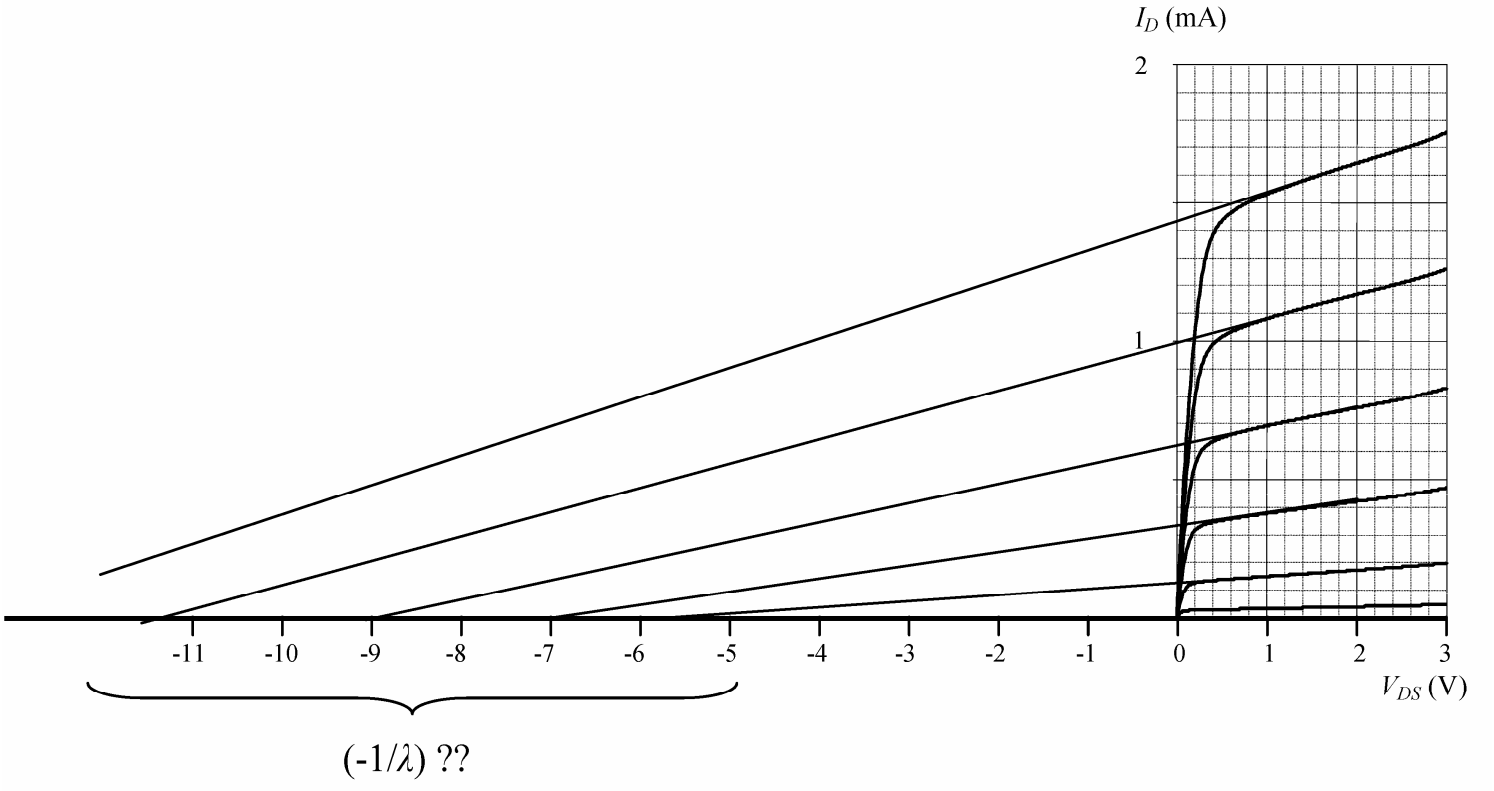
Determination of the threshold voltage under substrate bias (by SPICE simulation)



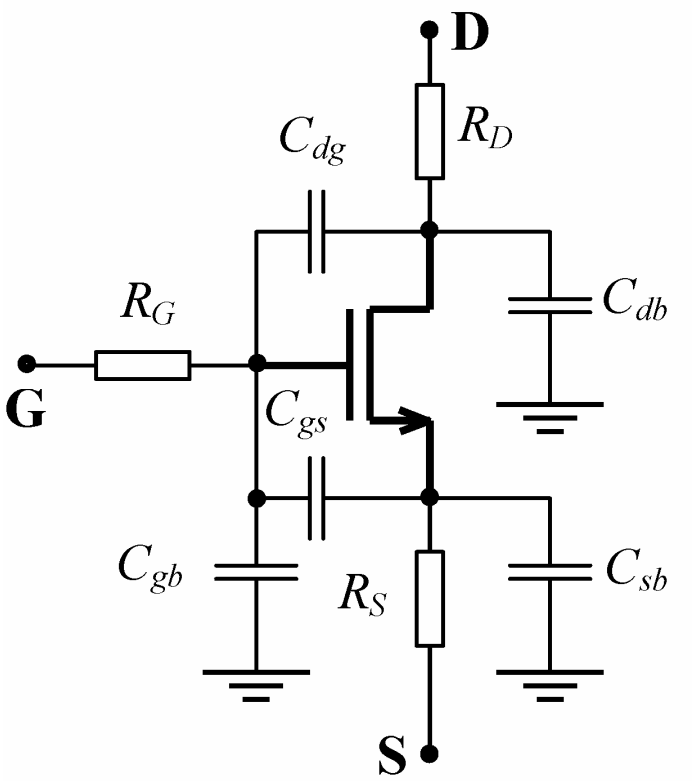
$L = 0.35\ \mu$m, $W = 10\ \mu$m NMOS transistor

(A) $V_{SB} = 0$, (B) $V_{SB} = 1$V

Channel length modulation



Parasitic components of MOS transistors



(and unavoidable parasitic bipolar transistors!)

a) Total gate capacitance:

C_{gs} = Gate electrode-channel cap. (C_g)

+ gate-source overlap cap. (C_{gso})

$$C_g = \frac{d\bar{Q}_i}{dV_{GS}}$$

$$d\bar{Q}_i(y) = -C_{ox}W\left[(V_{GS} - V_T) - V_c(y)\right]dy$$

$$d\bar{Q}_i(y) = -C_{ox}W(V_{GS} - V_T)\sqrt{1 - \frac{2I_D}{\mu_n C_{ox}W(V_{GS} - V_T)^2}\,y}\;\;dy$$

At the on-set of saturation

$$d\bar{Q}_i(y) = -C_{ox}W(V_{GS} - V_T)\sqrt{1 - \frac{y}{L}}\, dy$$

$$\bar{Q}_i = \frac{2}{3}C_{ox}WL(V_{GS} - V_T)$$

$$C_g = \frac{d\bar{Q}_i}{dV_{GS}} = \frac{2}{3}C_{ox}WL$$

For a transistor in velocity saturation;

$$C_g = C_{ox}WL$$

Gate-source overlap capacitance:

$$C_{gso} = (\mathrm{CGSO} \times W)$$

(CGSO usually given in F/m)

Total gate-source capacitance:

for a non-velocity saturated transistor

$$C_{gs} = W\left(\frac{2}{3}C_{ox}L + \mathrm{CGSO}\right) = C_{ox}WL\left(\frac{2}{3} + \frac{\mathrm{CGSO}}{C_{ox}L}\right)$$

for a velocity saturated transistor

$$C_{gs} = W(C_{ox}L + \mathrm{CGSO})$$

Example:

Technology: UMC018, $W = 20\ \mu\text{m}$, $L = 0.18\ \mu\text{m}$

$\text{TOX} = 4\text{E}-9\ [\text{m}]$, $\text{CGSO} = 9.07\text{E}-10\ [\text{F/m}]$

$$C_{ox} = \frac{34.5}{4}\times 10^{-7} = 8.625\times 10^{-7}\ \ [\text{F/cm}^2]$$

$$= 8.625\times 10^{-3}\ \ [\text{F/m}^2]$$

$$C_{gs} = 20\times 10^{-6}\left(\frac{2}{3}8.625\times 10^{-3}\times 0.18\times 10^{-6} + 9.07\times 10^{-10}\right)$$

$$= 20\times 10^{-6}(1.035\times 10^{-9} + 0.907\times 10^{-9})$$

$$= 38.84\times 10^{-15}\ \text{F} = 38.84\ \text{fF}$$

Drain-gate capacitance:

$$C_{dg} = (\text{CDGO}) \times W\,[\text{m}] \quad [\text{farad}]$$

Gate-substrate capacitance:

$$C_{gb} = (\text{CDBO}) \times L\,[\text{m}] \quad [\text{farad}]$$

Source - substrate (or well) and drain - substrate (or well) junction capacitances:

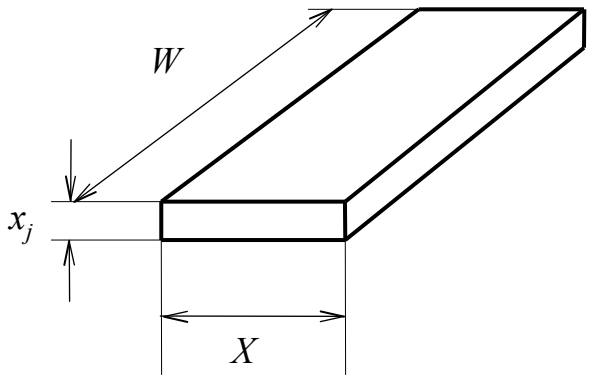
- Junction capacitances depend on the material, structure and the applied polarisation voltage:

$$C_j(V) = C_j(0)\left(1 - \frac{V}{\phi_B}\right)^{-m}$$

- They have two components, different in nature:

- The bottom capacitance, $C_j = \mathrm{CJ}\left[\mathrm{F/m^2}\right] \times (W \times X)$

- The side-wall capacitances, $C_{jsw} = \mathrm{CJSW}\left[\mathrm{F/m}\right] \times 2(W + X)$



Bottom junction capacitance per unit area:

$$\mathrm{CJ}(V) = \mathrm{CJ}\left(1 - \frac{V}{\mathrm{PB}}\right)^{-\mathrm{MJ}}$$

Side-wall junction capacitance per unit length:

$$\mathrm{CJSW}(V) = \mathrm{CJSW}\left(1 - \frac{V}{\mathrm{PB}}\right)^{-\mathrm{MJSW}}$$

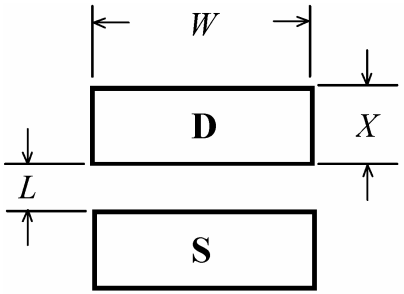
(both in terms of BSIM3 parameters)

Example:

Technology: AMS035

NMOS transistor: $W = 20\ \mu\text{m},\ L = 0.35\ \mu\text{m},\ X = 0.85\ \mu\text{m}$

$$V_{SB} = 0,\ V_{DB} = 1\ \text{V}$$



CJ	9.4 e-4
CJSW	2.5 e-10
MJ	3.4e-1
MJSW	2.3 e-1
PB	6.9 e-1

S (or D) bottom junction area:

$$A = X \times W = (0.85 \times 10^{-6}) \times (20 \times 10^{-6}) = 17 \times 10^{-12}\ \left[\text{m}^2\right]$$

S (or D) side-wall junction length:

$$L_{SW} = 2(X + W) = 2 \times (0.85 \times 10^{-6} + 20 \times 10^{-6}) = 41.7 \times 10^{-6}\ \left[\text{m}\right]$$

The bottom junction zero bias capacitance:

$$C_j(0) = (\mathrm{CJ}) \times A = \left(9.4 \times 10^{-4}\right)\left(17 \times 10^{-12}\right) = 159.8 \times 10^{-16}\,[\mathrm{F}] = 15.98\,[\mathrm{fF}]$$

The total side – wall capacitance:

$$C_{jsw}(0) = (\mathrm{CJSW}) \times L_{SW} = \left(2.5 \times 10^{-10}\right) \times \left(41.7 \times 10^{-6}\right) = 10.425\,[\mathrm{fF}]$$

The total zero bias junction capacitance:

$$C_{jT}(0) = C_j(0) + C_{jsw}(0) = 26.4\,[\mathrm{fF}]$$

(that is equal to C_{sb} since $V_{SB} = 0$)

The bias dependent factor for the bottom capacitance for 1V reverse bias:

$$\left(1-\frac{(-1)}{0.69}\right)^{-0.34}=0.737$$

The bottom junction capacitance for 1V reverse bias:

$$C_j(-1) = 15.98\times 0.737 = 11.78\ [\text{fF}]$$

The bias dependent factor for the side – wall capacitance for 1V reverse bias:

$$\left(1-\frac{(-1)}{0.69}\right)^{-0.23}=0.814$$

The side – wall junction capacitance for 1V reverse bias:

$$C_{jsw}(-1) = 10.425\times 0.814 = 8.48\ [\text{fF}]$$

The total junction capacitance for 1V reverse bias:

$$C_{jT}(-1) = 11.78 + 8.48 = 20.26\ [\text{fF}]$$

HF figure of merit (f_T)

(where the magnitude of the current gain drops to 1)

$$i_i = v_{gs}\, sC_{gs}\ , \quad i_o = g_m v_{gs} \quad \Rightarrow \quad |A_i| = \frac{|i_o|}{|i_i|} = \frac{g_m}{C_{gs}} = 1$$

For a non-velocity saturated transistor;

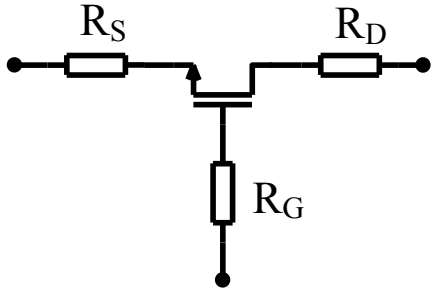
$$f_T = \frac{1}{2\pi} \frac{\mu(V_{GS} - V_T)}{L^2\left(\frac{2}{3} + \frac{\text{CGSO}}{LC_{ox}}\right)}$$

or $$f_T = \frac{1}{2\pi} A \sqrt{\frac{I_D}{W}} \quad \text{where} \quad A = \sqrt{\frac{2\mu}{k_{ol}^2 C_{ox} L^3}}$$ (depends on I_D)

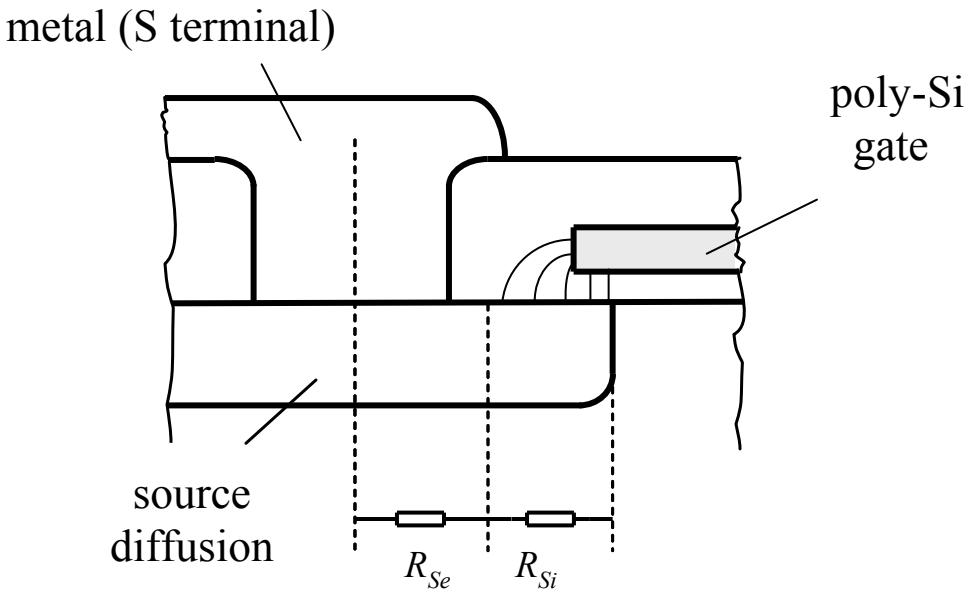
For a velocity saturated transistor;

$$f_T = \frac{1}{2\pi} \frac{kv_{sat}}{L\left(1 + \frac{\text{CGSO}}{LC_{ox}}\right)}$$ (does not depend on I_D)

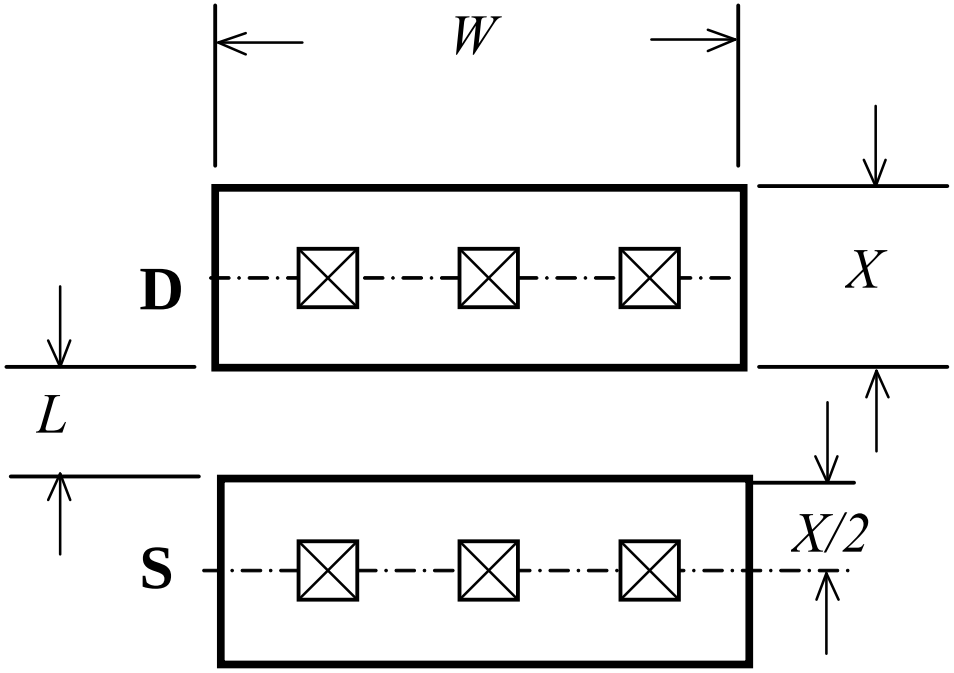
Parasitic resistors:



a) Source (drain) series resistance:



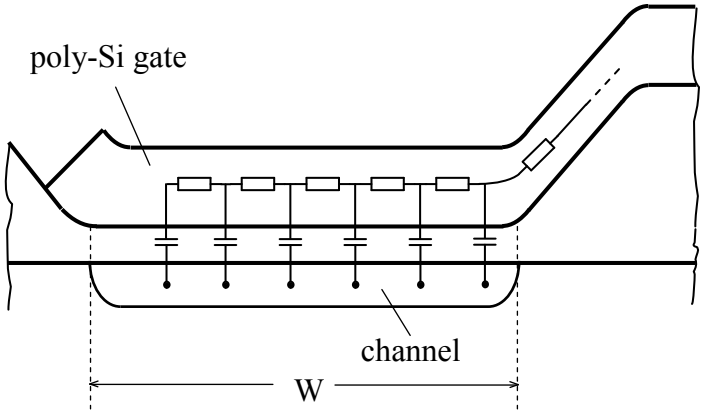
$$R_S = R_{Se} + R_{Si} + R_{contact}$$



$$R_{Si} = \frac{1}{2}\frac{(\text{RDSW})}{W[\mu\text{m}]} \quad \text{(Total res. per 1 micron gate width)}$$

$$R_{Se} = \frac{1}{2}(\text{RSH}) \times (\text{NRS}) \ , \quad (\text{NRS}) = X / W$$

b) Gate series resistance:



Transfer function of a R-C line:

$$A = \frac{v_o}{v_i} = \frac{1}{\cosh\left(l\sqrt{s\,rc}\right)}$$

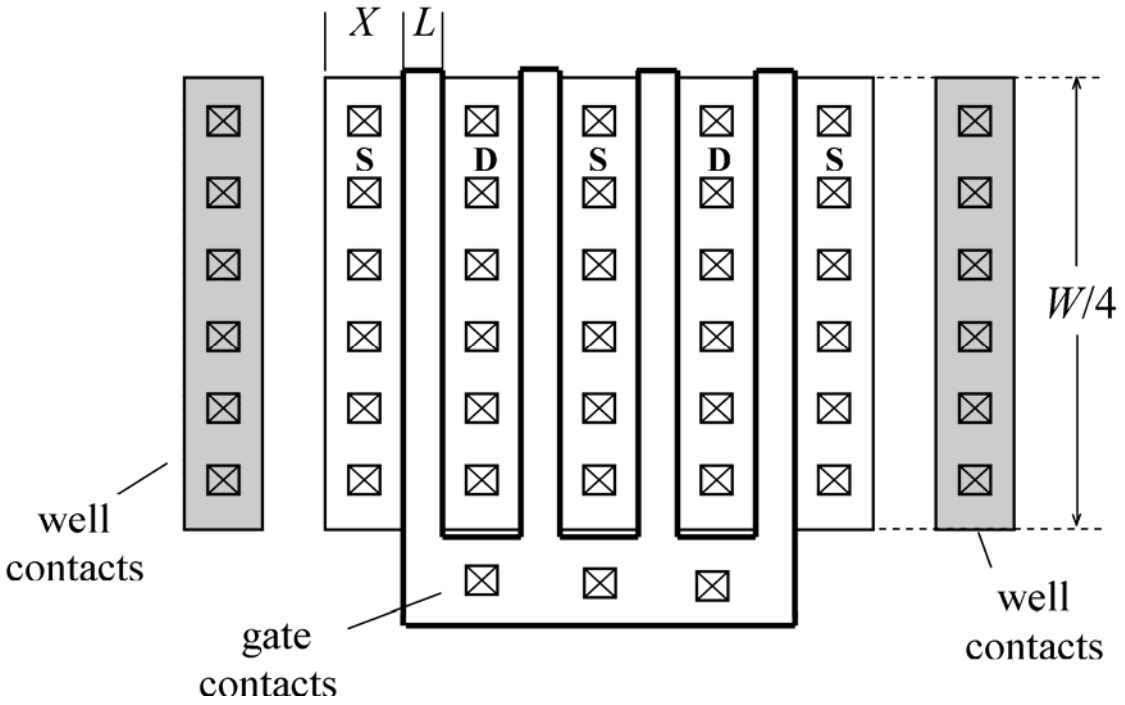
f_c , The frequency where $|A|$ drops 3 dB:

$$\cosh\left(l\sqrt{s_c rc}\right) = \sqrt{2} \;\rightarrow\; \left(l\sqrt{s_c rc}\right) = 0.882 \;\text{ or }\; \left(s_c l^2 rc\right) = 0.78$$

$$R = r \times l = R_{sh}\frac{W}{L}\;,\quad C = C_{ox}WL \;\rightarrow\; s_c = \frac{0.78}{R_{sh}C_{ox}W^2}$$

$$f_c = \frac{0.78}{2\pi \times R_{sh}C_{ox}W^2} = \frac{0.124}{R_{sh}C_{ox}W^2}$$

Finger structure:



- f_c increases with the square of the number of fingers.
- Source and drain parasitic capacitances decrease.