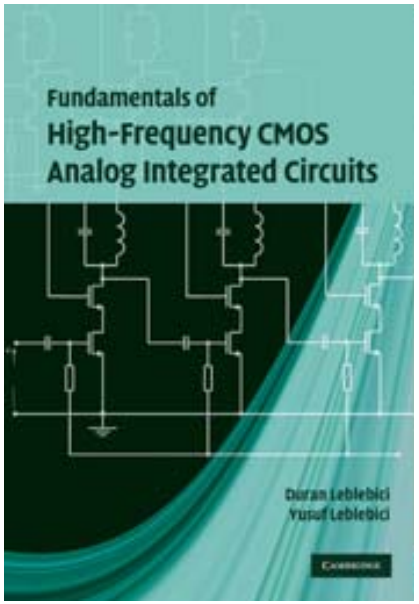


Fundamentals of High-Frequency CMOS Analog Integrated Circuits

Duran Leblebici
Yusuf Leblebici

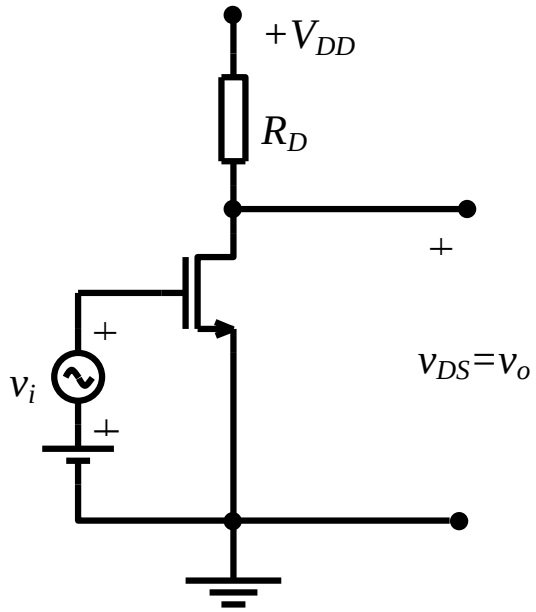
Chapter 2

Basic MOS Amplifiers
(DC and Low Frequency Behavior)

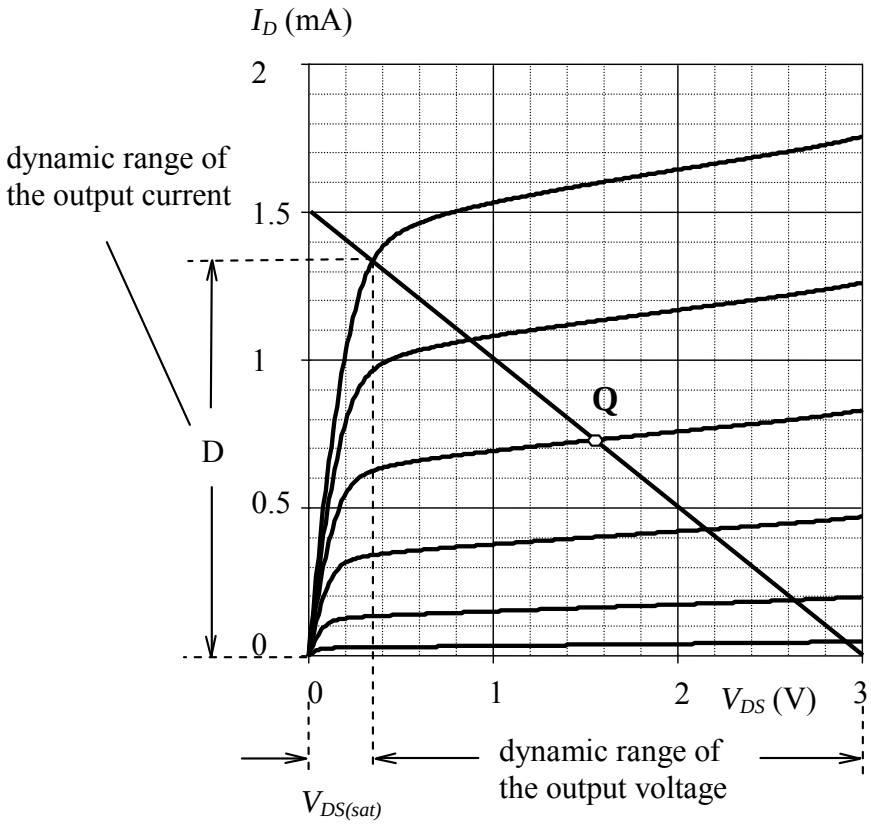
1- Common Source (CS) Amplifier

Main features:

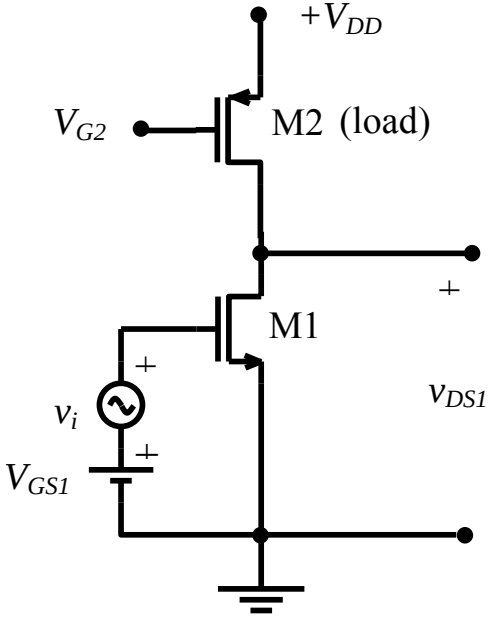
- High input resistance,
- High output resistance,
- High (negative) voltage gain.



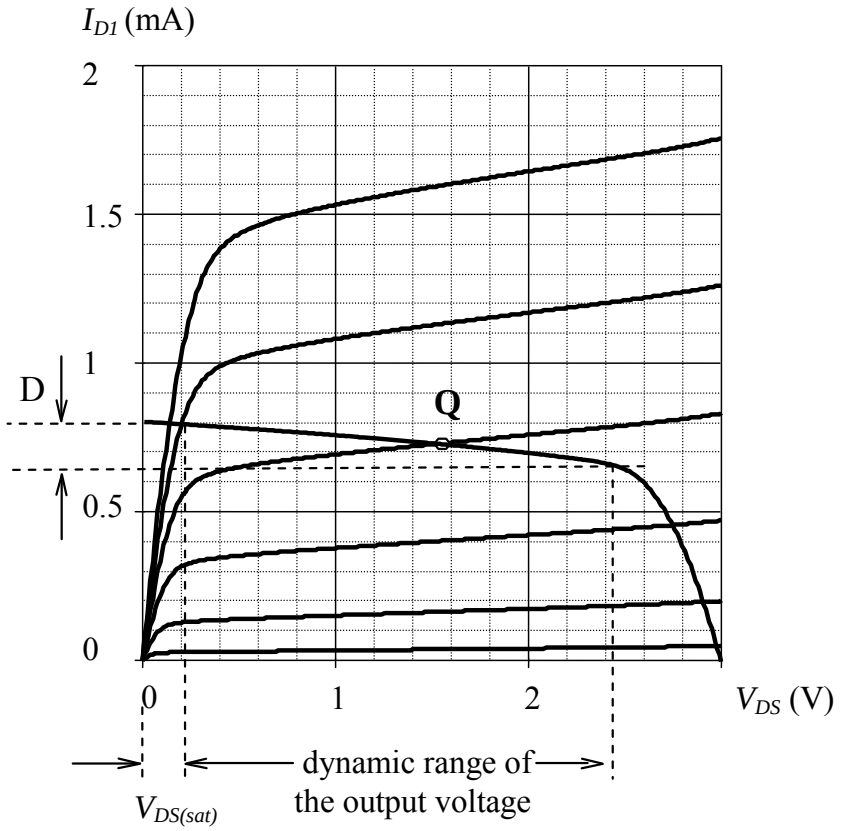
Basic circuit of a resistance loaded common source amplifier.



The load-line and the output current and voltage dynamic ranges



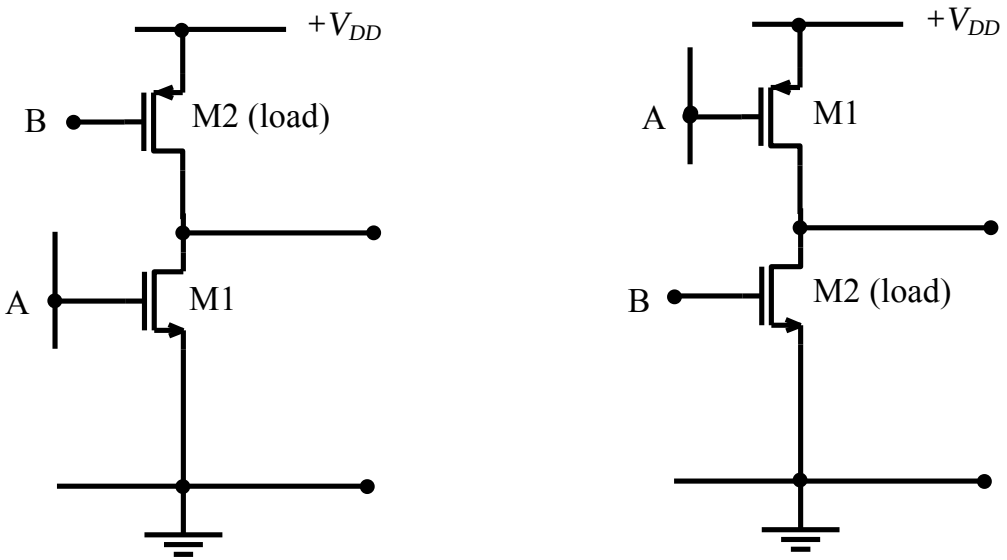
Passive PMOS transistor (DC current source) loaded CS amplifier



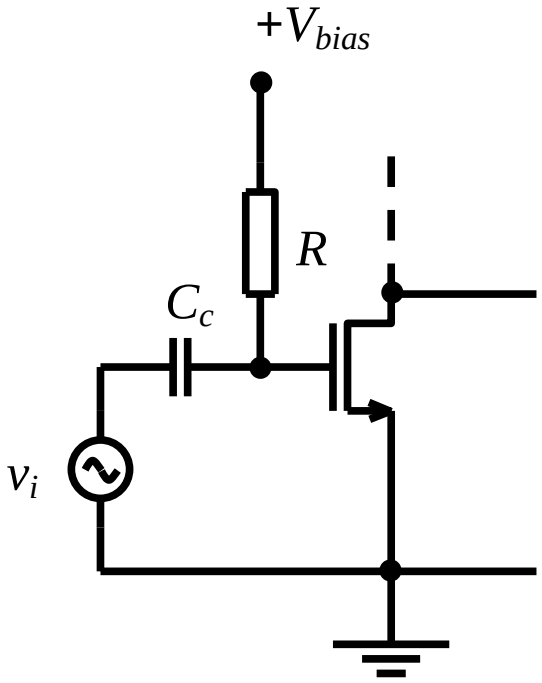
The nonlinear load-line, the output current and voltage dynamic ranges corresponding to the linear region of the load

DC Biasing:

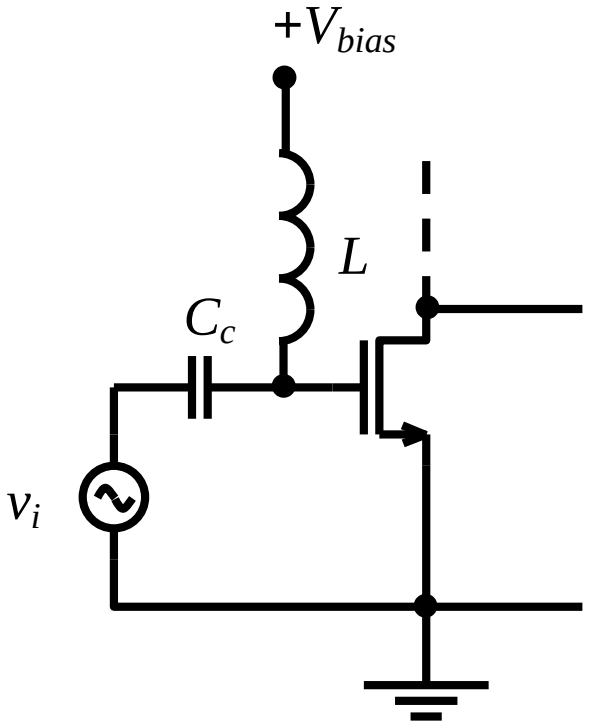
a) Bias the input transistor from the output of the previous stage



b) Biasing suitable for AC coupling to the signal source

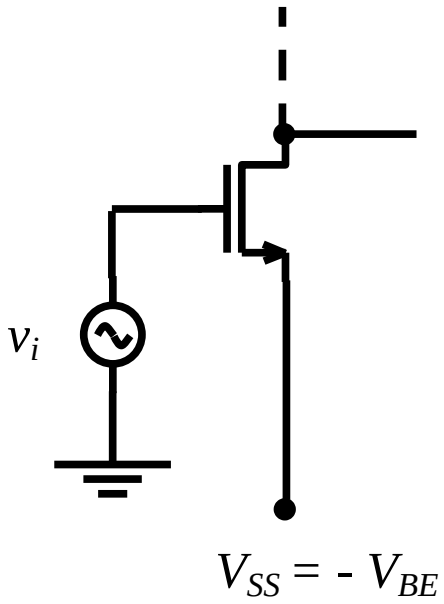


For LF and wide-band applications



For HF low noise applications

c) Biasing suitable for DC coupling to the signal source



(The bias resistor or inductor connected to the input is eliminated)

The linearisation of the current-voltage relation and the small-signal equivalent circuit:

For a non velocity saturated MOS transistor;

$$I_D = \frac{1}{2}\beta(V_{GS} - V_T)^2 \left(\frac{1 + \lambda V_{DS}}{1 + \lambda(V_{GS} - V_T)} \right) \quad \text{where} \quad \beta = \mu C_{ox} \frac{W}{L}$$

The Taylor series around the operating point, with only linear terms;

$$I_D + \Delta I_D \cong I_D + \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{\Delta V_{DS}=0} \times \Delta V_{GS} + \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{\Delta V_{GS}=0} \times \Delta V_{DS}$$

$$\Delta I_D \cong \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{\Delta V_{DS}=0} \times \Delta V_{GS} + \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{\Delta V_{GS}=0} \times \Delta V_{DS}$$

Definitions:

The transconductance: $g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{\Delta V_{DS}=0}$ (The control ability of V_{GS} on I_D)

The output conductance: $g_o = \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{\Delta V_{GS}=0}$

From the definition;

$$g_m = \beta(V_{GS} - V_T)(1 + \lambda V_{DS})\frac{2 + \lambda(V_{GS} - V_T)}{2\left[1 + \lambda(V_{GS} - V_T)^2\right]}$$

$$g_m \cong \beta(V_{GS} - V_T) = \sqrt{2\beta I_D} \quad \text{(for small values of } \lambda\text{)}$$

For a velocity saturated MOS transistor;

$$|I_D| = kWC_{ox}(V_{GS} - V_T)v_{sat}$$

$$g_m = \frac{dI_D}{dV_{GS}} = kWC_{ox}v_{sat}$$

Note that;

- For a non velocity sturated transistor g_m increases with I_D,
- For a velocity saturated transistor g_m does not change with I_D.

From the definition of g_o;

$$g_o = g_{ds} = I_D \frac{\lambda}{(1+\lambda V_{DS})}$$

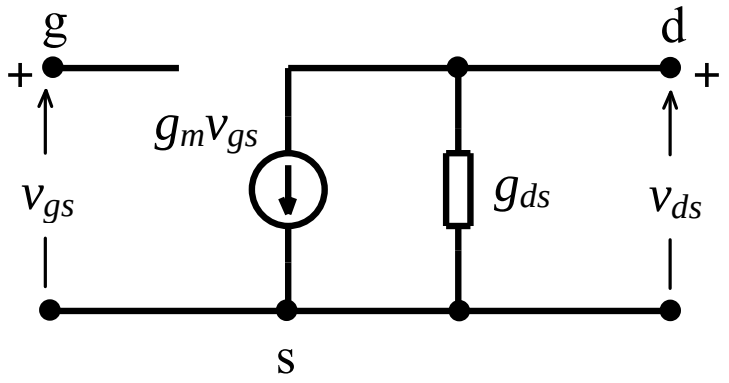
$$g_o = g_{ds} \cong I_D \lambda \quad \text{(for small values of } \lambda\text{)}$$

The small amplitude signal (small signal) component of the drain current can be expressed as;

$$i_d = g_m v_{gs} + g_{ds} v_{ds}$$

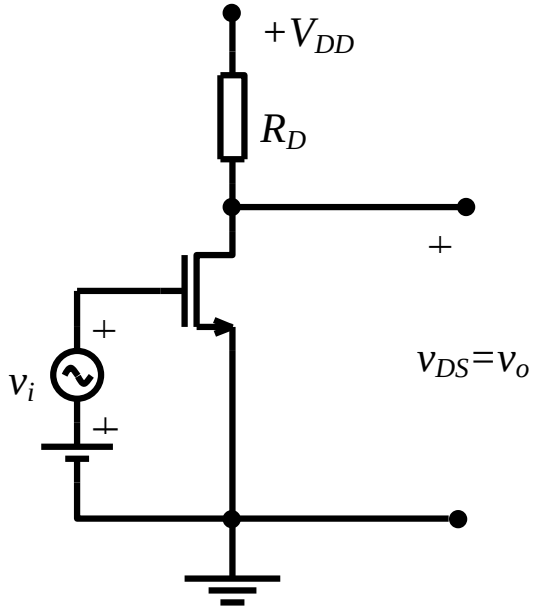
where v_{gs} and v_{ds} are the small signal components of V_{gs} and V_{ds}.

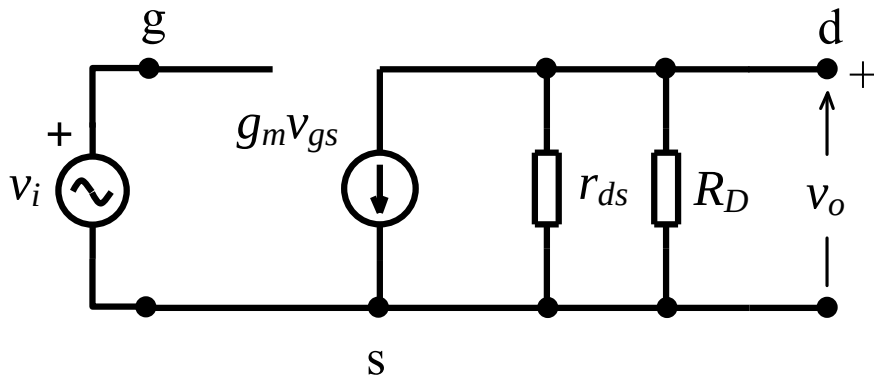
The equivalent circuit that represents this expression:



Example:

The circuit diagram and the small signal equivalent circuit of a resistance loaded amplifier.





$$v_{gs} = v_i, \quad r_{ds} = \frac{1}{g_{ds}}$$

The small signal voltage gain: $A_v = \dfrac{v_o}{v_i} = -g_m(r_{ds} \,//\, R_D) = -g_m \dfrac{r_{ds} R_D}{r_{ds} + R_D}$

For $r_{ds} \gg R_D$: $A_v \cong -g_m R_D$

$$|A_v| \cong g_m R_D = \sqrt{2\beta I_D} \cdot R_D$$

Note that for a symmetrical dynamic range

$$I_D = \frac{1}{2}\frac{(V_{DD} - V_{DS(sat)})}{R_D}$$

$$\Downarrow$$

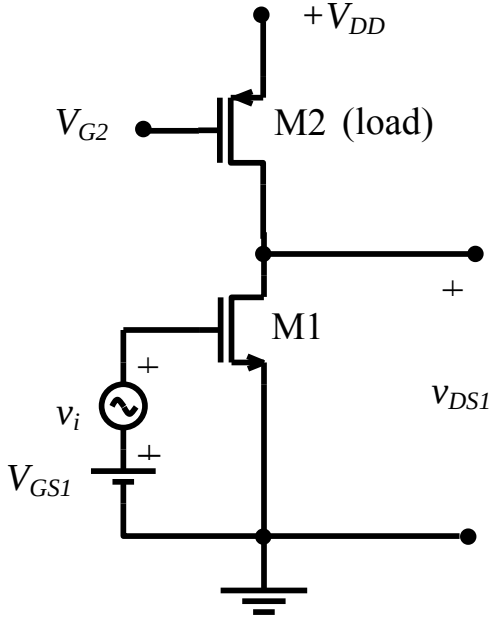
$$|A_v| \cong \sqrt{\beta(V_{DD} - V_{DS(sat)})R_D}$$

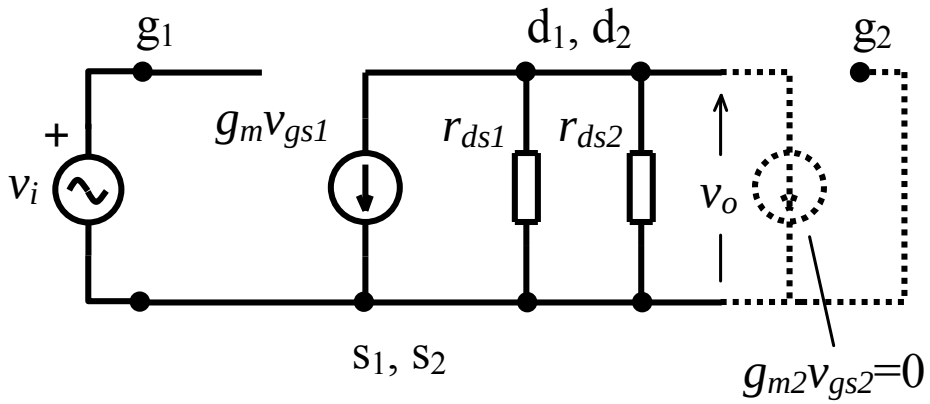
To obtain a high voltage gain for a certain technology:

- High (W / L)
- High V_{DD} (technology limited!)
- High R_D (Limits the frequency band)

Example:

The circuit diagram and the small signal equivalent circuit of a passive PMOS (DC current source) loaded amplifier.





$$v_{gs1} = v_i, \quad v_{gs2} = 0, \quad r_{ds1} = \frac{1}{g_{ds1}}, \quad r_{ds2} = \frac{1}{g_{ds2}}$$

The small signal voltage gain:

$$A_v = \frac{v_o}{v_i} = -g_{m1}(r_{ds1} \,//\, r_{ds2}) = -\frac{g_{m1}}{(g_{ds1} + g_{ds2})}$$

In terms of the transistor parameters and I_D;

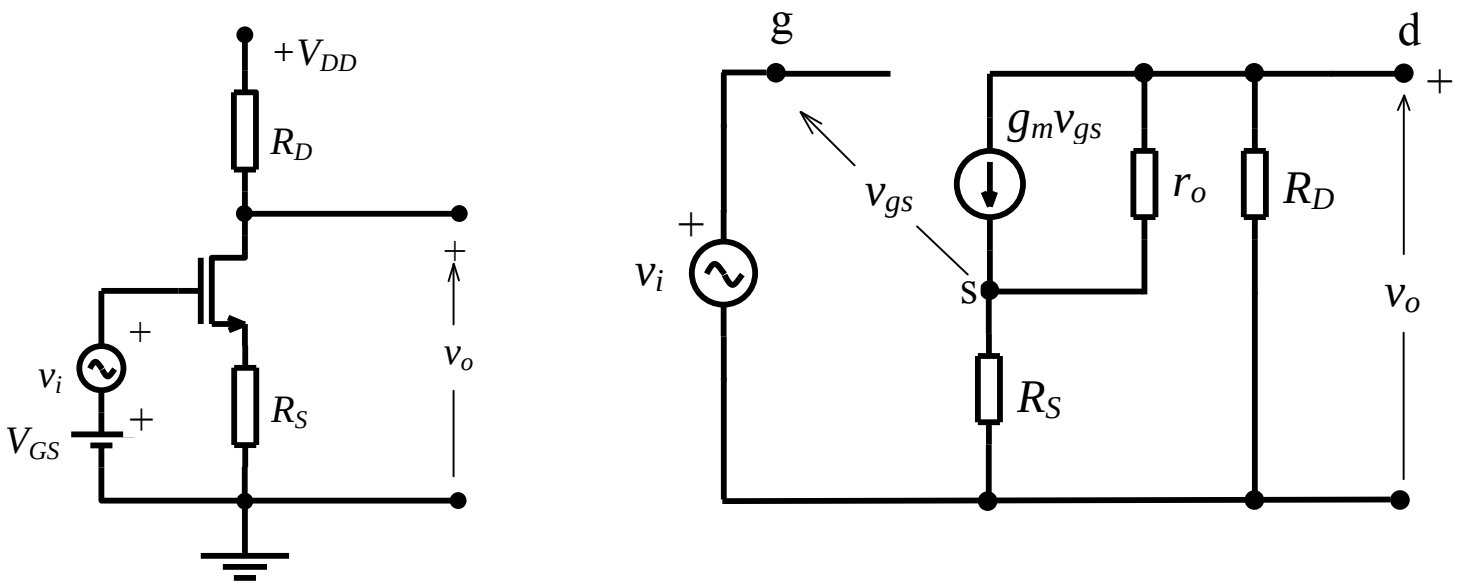
$$A_v \cong -\sqrt{2\beta_1 I_{D1}}\,\frac{1}{I_{D1}\lambda_1 + \left|I_{D2}\right|\lambda_2} = -\sqrt{\frac{2\beta_1}{I_{D1}}}\,\frac{1}{(\lambda_1+\lambda_2)}$$

To obtain a high voltage gain for a certain technology:

- High (W / L) for M1
- low λ_1 and λ_2 (long channel devices)
- Low I_D (Limits the frequency band)

It must be noted that to adjust the DC operating point to approx. (V_{DD} / 2) the bias of M2 must be fine-tuned!

CS amplifier with a source resistance, R_S

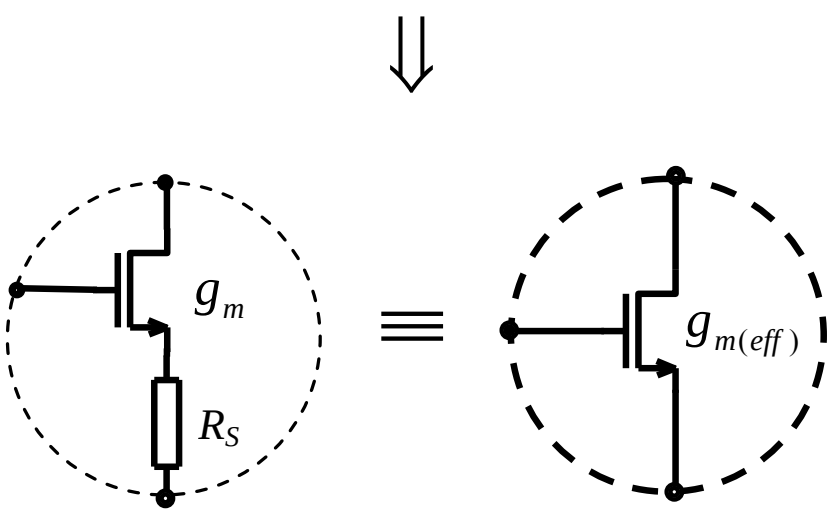


$$A_v = -g_m \frac{R_D}{(1+g_m R_S) + \dfrac{(R_D + R_S)}{r_o}}$$

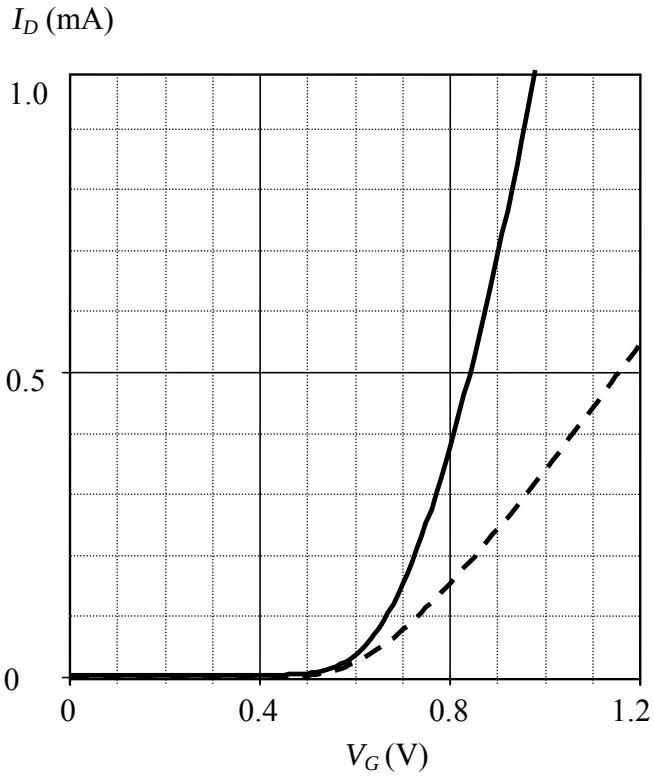
$$A_v \cong -\frac{g_m}{(1+g_m R_S)} R_D \quad \text{for} \quad r_o \gg (R_D + R_S)$$

If we compare the gain expressions of a CS amplifier without and with R_S;

$$A_v = -g_m R_D \quad \text{and} \quad A_v = -\frac{g_m}{(1+g_m R_S)} R_D$$



$$g_{m(eff)} \cong \frac{g_m}{(1+g_m R_S)}$$



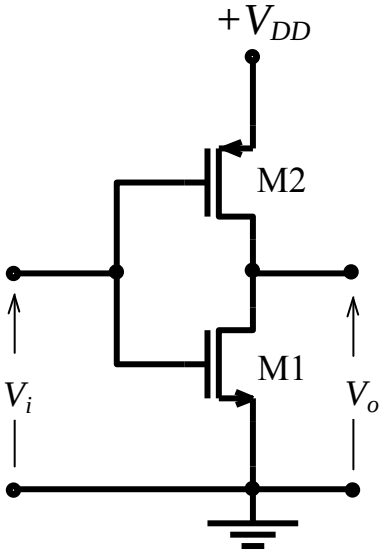
R_S reduces and linearizes g_m

2. Active Transistor Loaded MOS Amplifier (CMOS Inverter Amplifier)

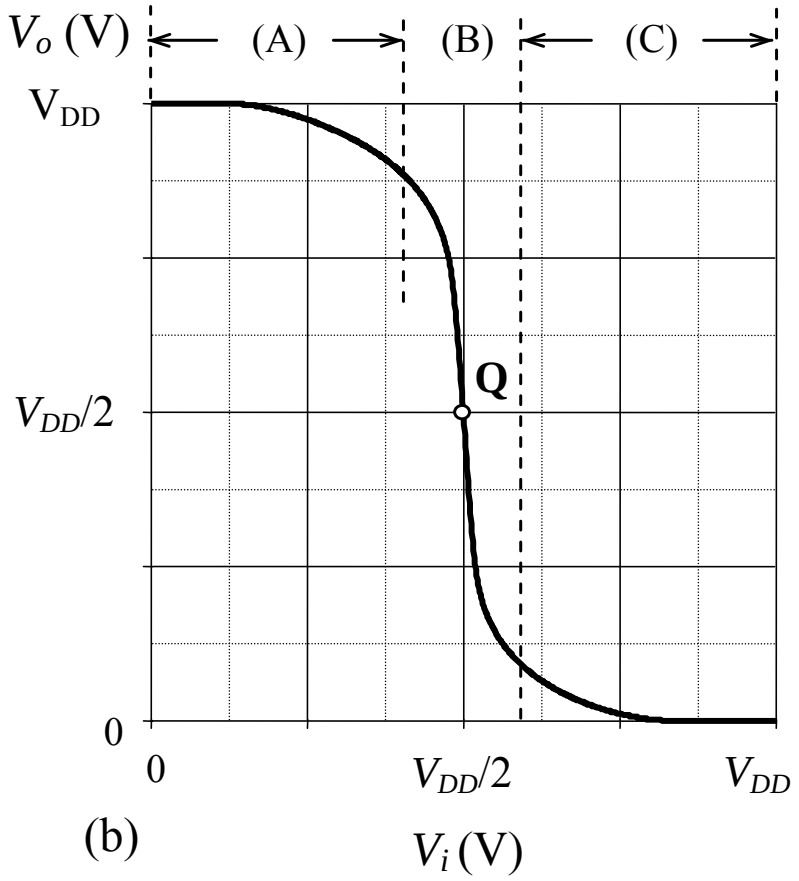
Main features:

- Low input resistance; $r_i \cong 1/(g_{m1} + g_{m2})$,
- Low output resistance,
- Relatively high transresistance
- High (negative) voltage gain.
- Rail-to-rail output voltage swing.

The well-known CMOS logic inverter:



(a)

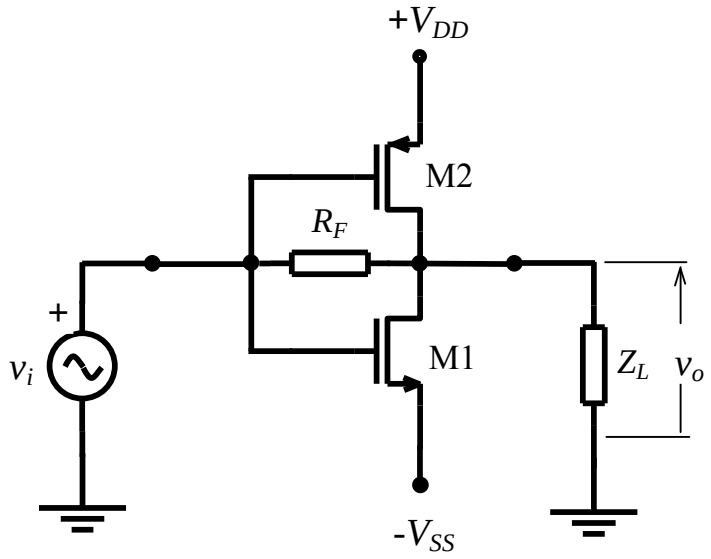


(b)

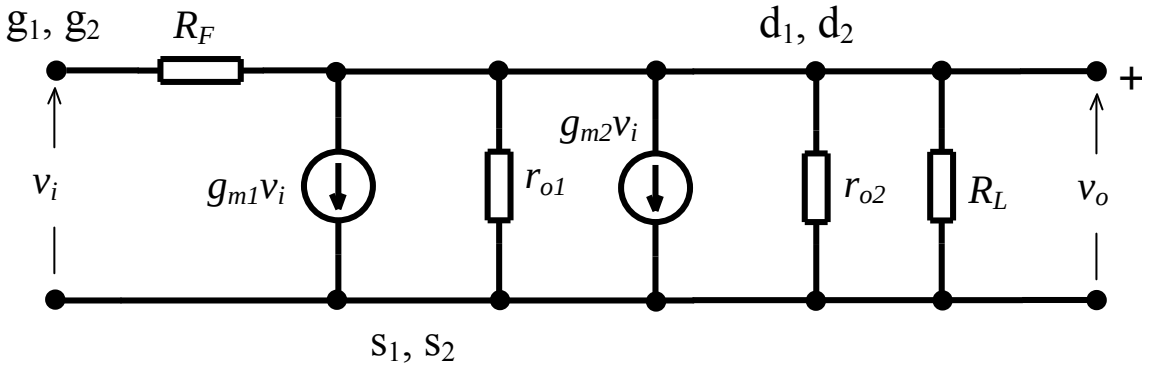
If the circuit is biased at Q,

it can be used as a high gain analog amplifier.

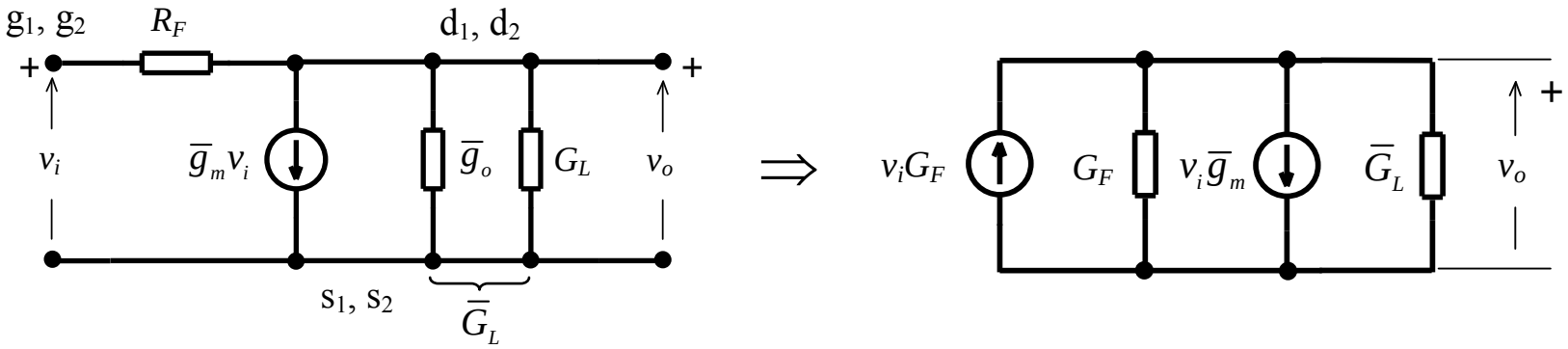
Biasing the circuit for zero input and zero output quiescent voltages:



The small-signal equivalent circuit



Development of the equivalent circuit:



$\bar{g}_m = g_{m1} + g_{m2}$, $\bar{g}_o = g_{o1} + g_{o2}$

After Thevenin-Norton conversion

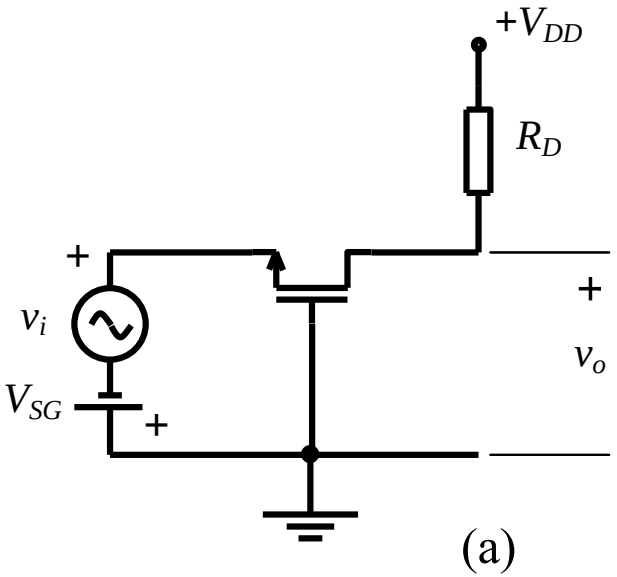
Voltage gain: $A_v = -\dfrac{\bar{g}_m - G_F}{\bar{G}_L + G_F}$

Transresistance: $R_m = \dfrac{v_o}{i_i} = \dfrac{v_o}{v_i}\dfrac{v_i}{i_i} = A_v r_i = -\dfrac{\bar{g}_m - G_F}{\bar{g}_m + \bar{G}_L}\dfrac{1}{G_F}$

$R_m \cong -R_F$ for $G_F, \bar{G}_L \ll \bar{g}_m$

Input res. $g_i = \dfrac{\bar{G}_L + \bar{g}_m}{\bar{G}_L + G_F} G_F$ $\qquad g_i \cong \bar{G}_L + \bar{g}_m \cong \bar{g}_m$ for $G_F \ll \bar{G}_L$

3. Common Gate (CG) Amplifier:



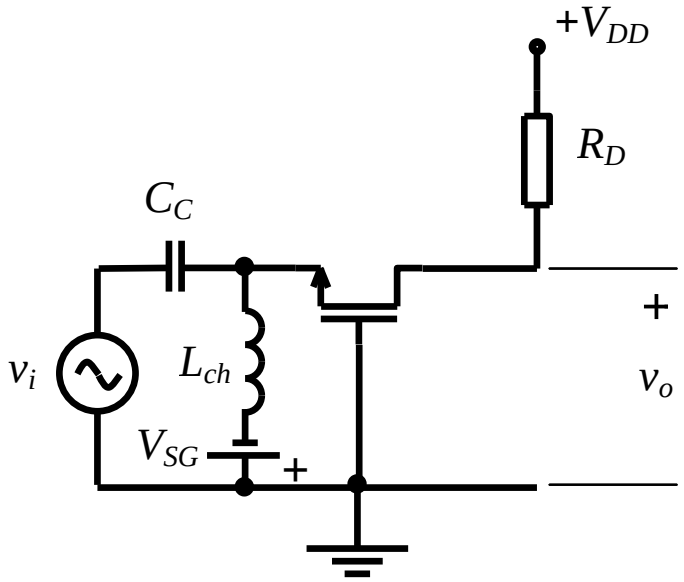
(a)

Main features:

- Low input resistance,
- Very high output resistance,
- High (positive) voltage gain.
- Unity current gain.

DC Biasing arrangements:

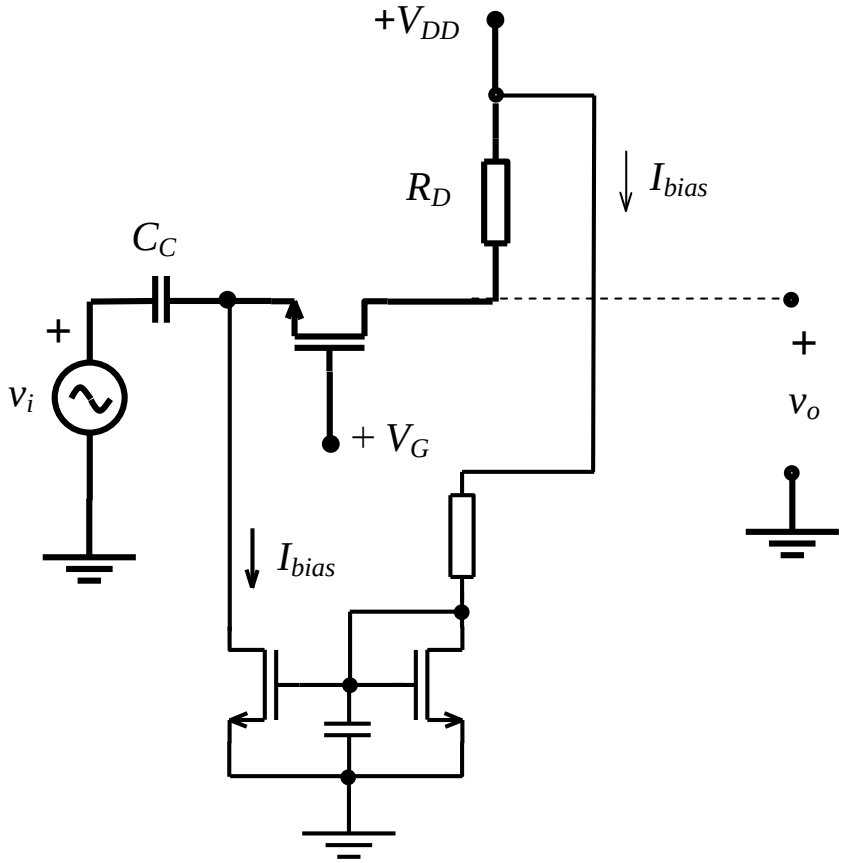
a) Biasing via an inductor



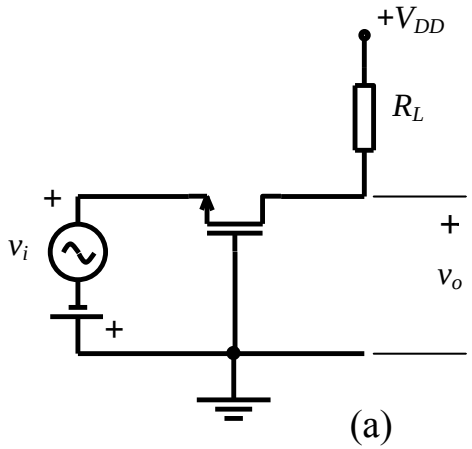
L_{ch} : High inductance choking coil

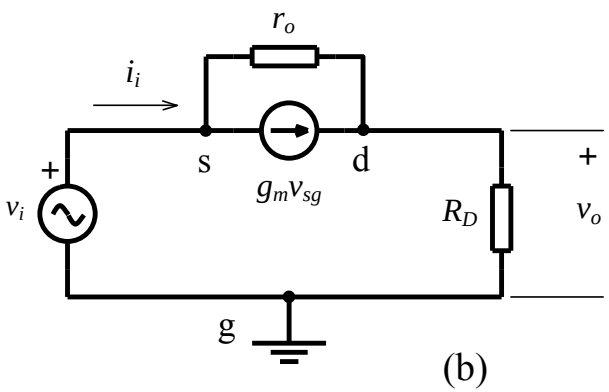
Usually not suitable for on-chip solutions!

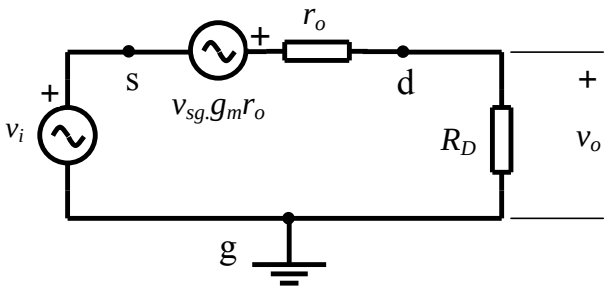
b) Determination of the DC quiescent current with a current source



The small-signal equivalent circuit:





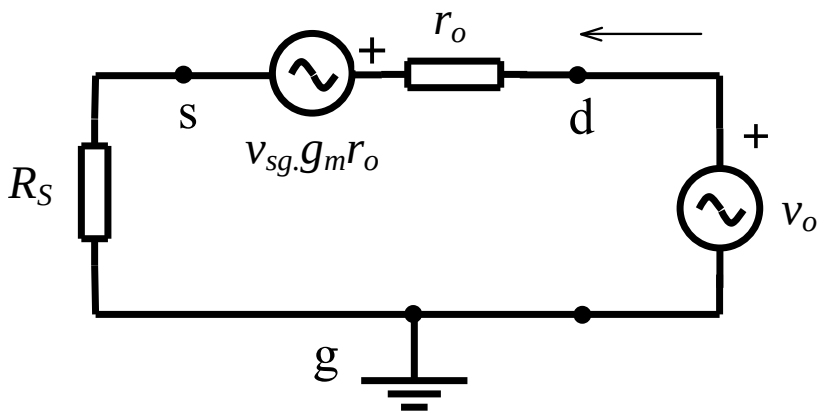


$$A_v = \frac{v_o}{v_i} = \frac{1 + g_m r_o}{(r_o + R_D)} R_D$$

$A_v \cong +g_m R_D$ for $g_m \gg (1/r_o)$ and $r_o \gg R_D$

$$r_i = \frac{r_o + R_D}{1 + g_m r_o} \qquad r_i \cong \frac{1}{g_m} \text{ for } g_m \gg (1/r_o) \text{ and } r_o \gg R_D$$

Equivalent circuit to calculate the output resistance for a non-zero input signal source resistance (R_S):



$$i_o = \frac{(v_o - v_{gs} g_m r_o)}{r_o + R_S} \quad , \quad v_{sg} = i_o R_S$$

$$i_o \left(r_o + R_S + R_S g_m r_o \right) = v_o$$

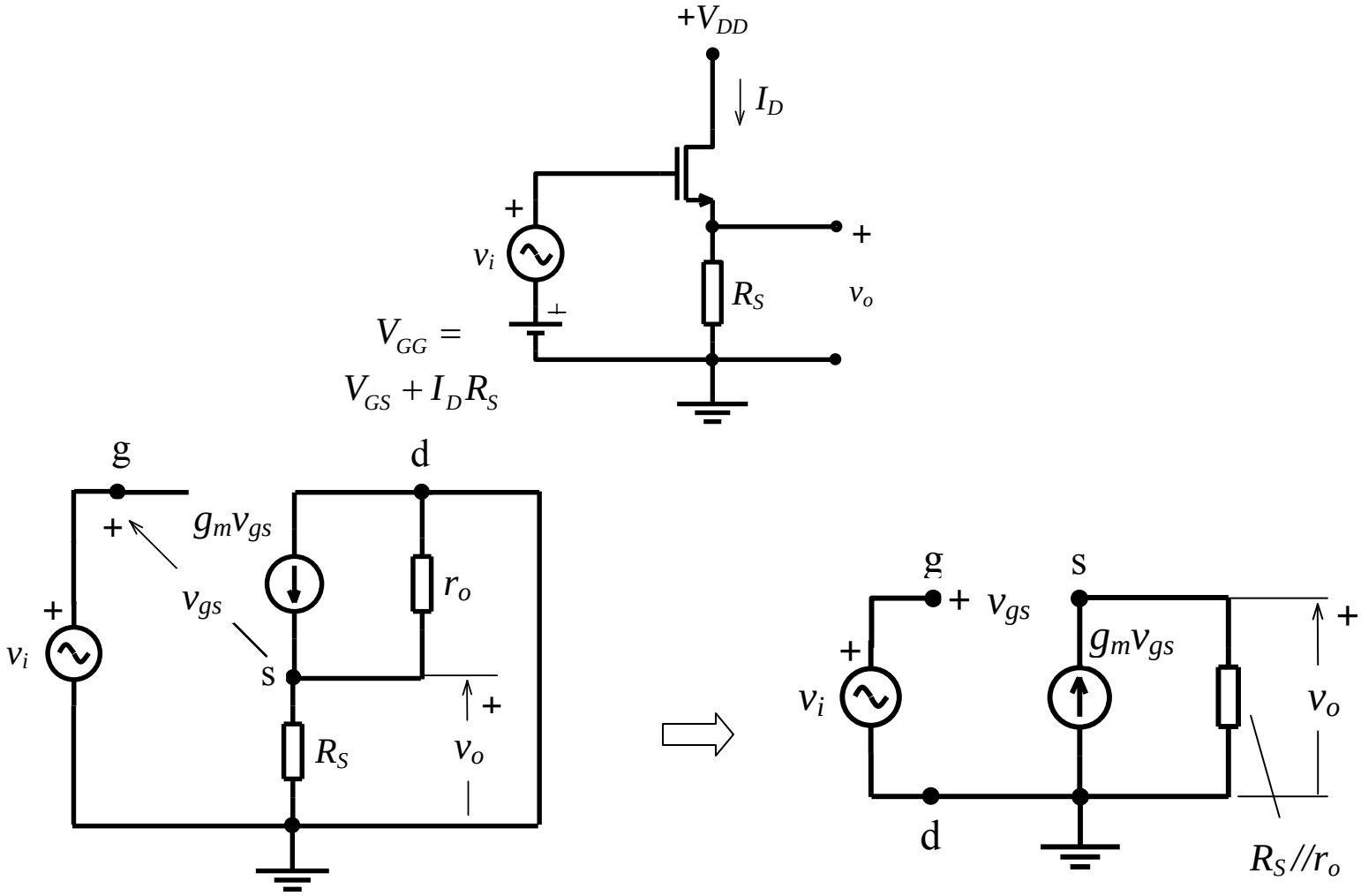
$$r_{out} = \frac{v_o}{i_o} = r_o (1 + R_S g_m) + R_S$$

$r_{out} \gg r_o$ for $R_S g_m \gg 1$

4. Common Drain Amplifier (The Source Follower):

Main features:

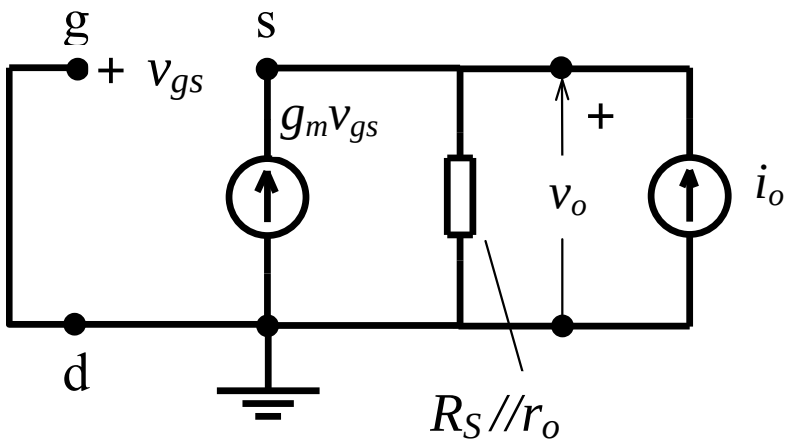
- High input resistance,
- Low output resistance,
- Unity (positive) voltage gain.



$$A_v = \frac{g_m \bar{R}}{1 + g_m \bar{R}} \ , \ \bar{R} = (r_o \,//\, R_S)$$

$$A_v \cong +1 \quad \text{for} \quad g_m \bar{R} \gg 1$$

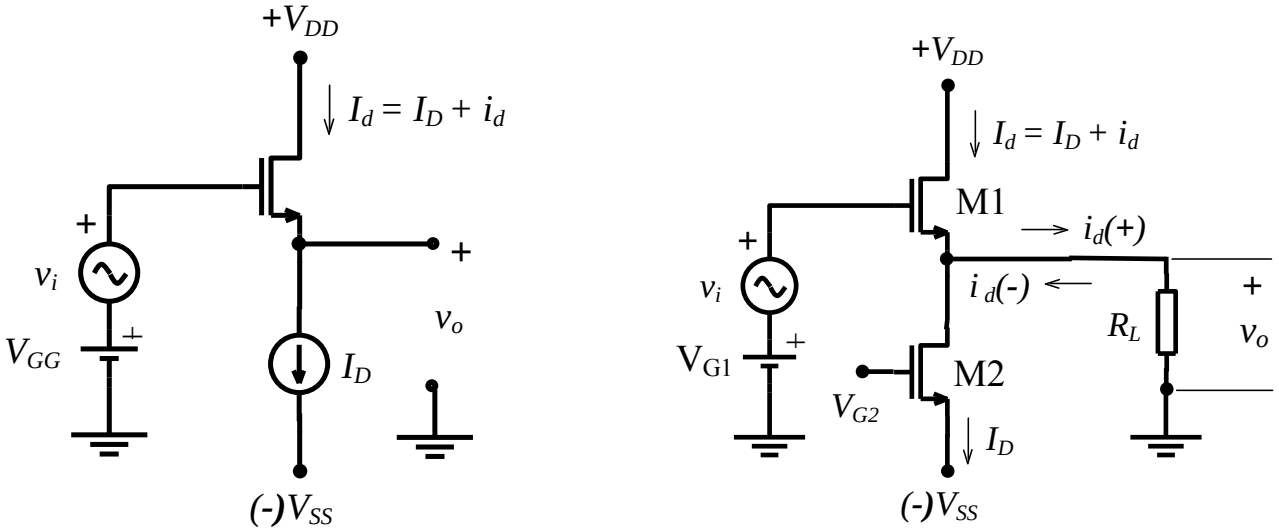
Equivalent circuit to calculate the output resistance:



$$r_o = \frac{v_o}{i_o} = \frac{\bar{R}}{1 + g_m \bar{R}}$$

$$r_o \cong \frac{1}{g_m} \quad \text{for} \quad g_m \bar{R} \gg 1$$

For zero output quiescent voltage:



- For $v_i = 0$; $I_{D1} = I_{D2}$, $I_{D2} = I_D$ = constant, $v_o = 0$

- For negative peak of v_i $(v_i = \breve{v}_i)$; $I_{D1} = 0$, $\breve{v}_o = -I_D R_L$

  Saturation condition for M2: $V_{DS2} = (V_{SS} - I_D R_L) \geq (V_{GS2} - V_T)$

- For positive peak of v_i $(v_i = \hat{v}_i)$; $I_{D1} = 2I_D$, $\hat{v}_o = +I_D R_L$

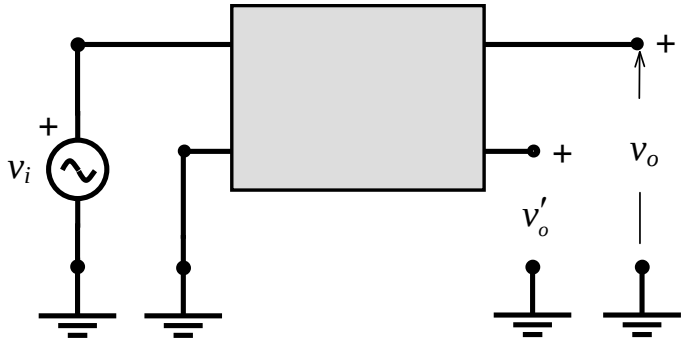
  Saturation condition for M1: $V_{DS1} = (V_{DD} - \hat{v}_o) \geq \left[\left(V_{G1} + \hat{v}_i \right) - V_T \right]$

5. Differential Amplifier (The Long-Tailed Pair):

Main features:

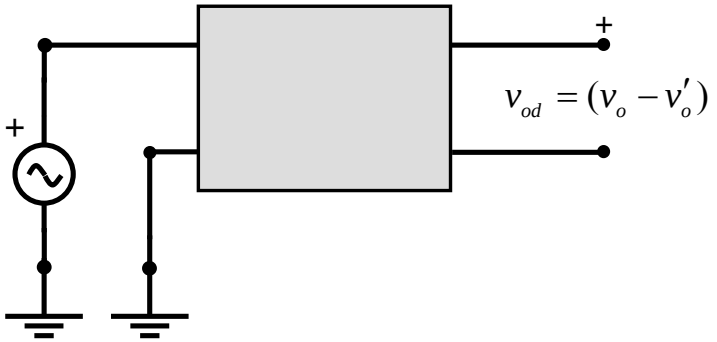
- Differential or single-ended input,
- Differential or single-ended output,
- High input resistance,
- Low or high output resistance,
- High voltage gain and high transconductance.

Differential amplifier configurations:



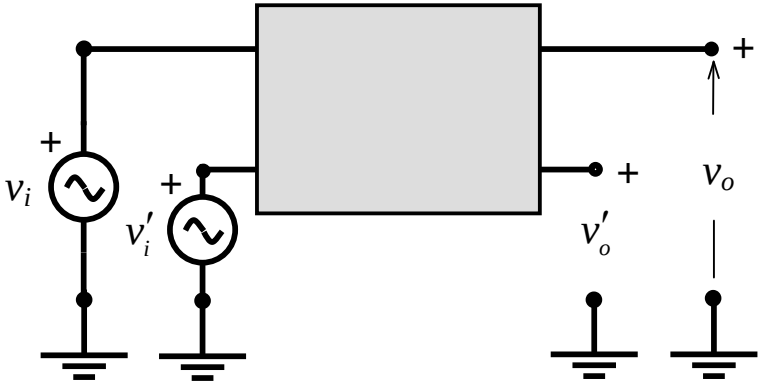
$$v_o = -A_v v_i \quad , \quad v_o' = +A_v v_i$$

Single-ended input,
two single-ended outputs



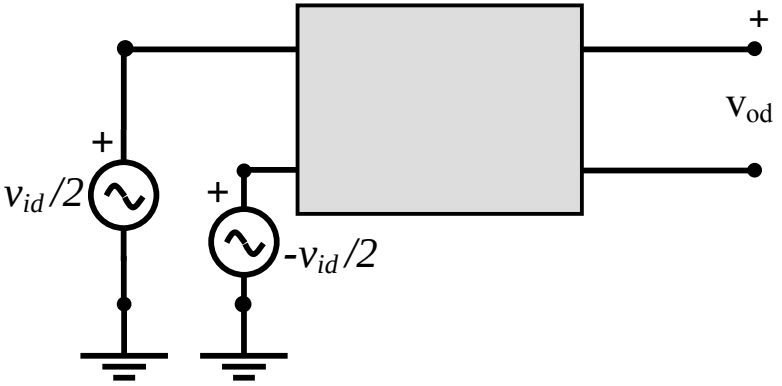
$$v_{od} = A_{vd} v_i \ , \ A_{vd} = 2A_v$$

Single-ended input,
differential output



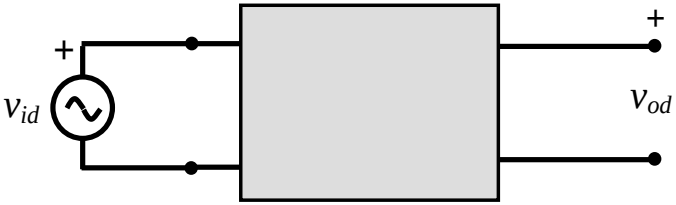
$$v_o = -A_v(v_i - v_i^{'}) \quad , \quad v_o^{'} = +A_v(v_i - v_i^{'})$$

Two single-ended inputs,
two single-ended outputs



$$v_{od} = A_{vd} v_{id}$$

Differential with respect to ground inputs,
differential output

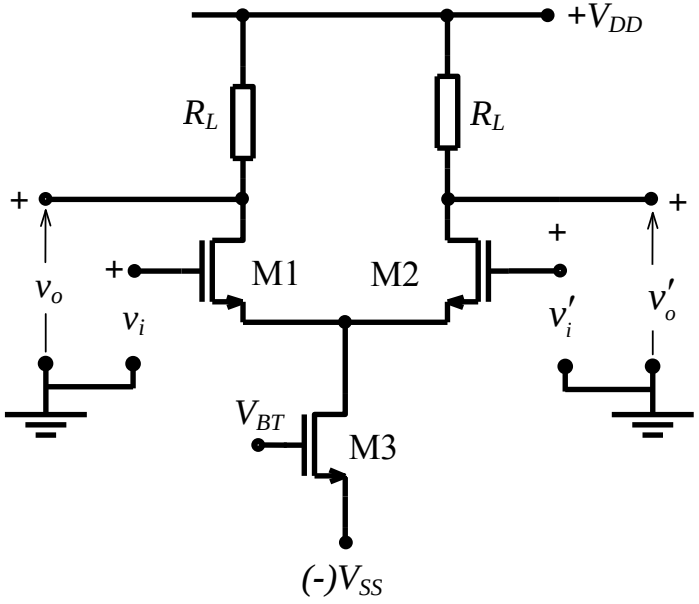


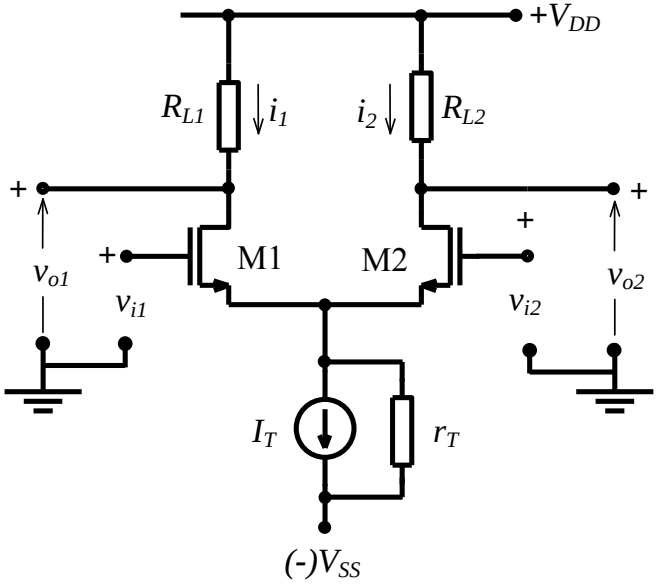
$$v_{od} = A_{vd} v_{id}$$

Differential input, differential output

Typical circuits:

a) Resistor loaded long-tailed pair



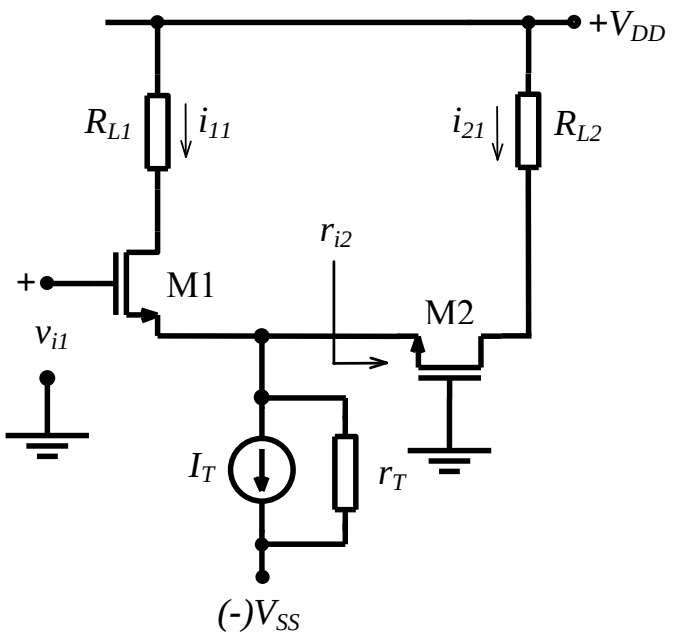


M1 and M2 are identical.

For $v_{i1} = 0,\ v_{i2} = 0;\ \ I_{D1} = I_{D2} = \dfrac{I_T}{2}$

Transconductances of M1 and M2: $g_m = \sqrt{\beta_N I_T}\ ,\ \beta_N = \mu_n C_{ox} \dfrac{W}{L}$

Redrawn for $v_{i1} \neq 0$, $v_{i2} = 0$:



The source load of M1:

$$r_{S1} = r_T \,//\, r_{i2} \cong r_{i2} = \frac{1}{g_m}$$

The effective transconductance of M1:

$$g_{m(eff)} = \frac{g_m}{1 + g_m r_{S1}} = \frac{g_m}{2}$$

$$i_{11} = v_{i1}\frac{g_m}{2}, \quad i_{21} = -i_{11} = -v_{i1}\frac{g_m}{2}$$

Similarly for $v_{i2} \neq 0$, $v_{i1} = 0$: $i_{22} = v_{i2}\frac{g_m}{2}$, $i_{12} = -i_{22} = -v_{i2}\frac{g_m}{2}$

Under small-signal conditions, with superposition;

$$i_1 = i_{11} + i_{12} = \frac{g_m}{2}(v_{i1} - v_{i2}), \quad i_2 = i_{21} + i_{22} = -\frac{g_m}{2}(v_{i1} - v_{i2})$$

Single-ended output voltages of M1 and M2:

$$v_o = -\bar{R}_L i_1 = -\bar{R}_L \frac{g_m}{2}(v_i - v_i')$$

$$v_o' = -\bar{R}_L i_1' = \bar{R}_L \frac{g_m}{2}(v_i - v_i')$$

Differential output voltage:

$$(v_o - v_o') = -\bar{R}_L g_m (v_i - v_i')$$

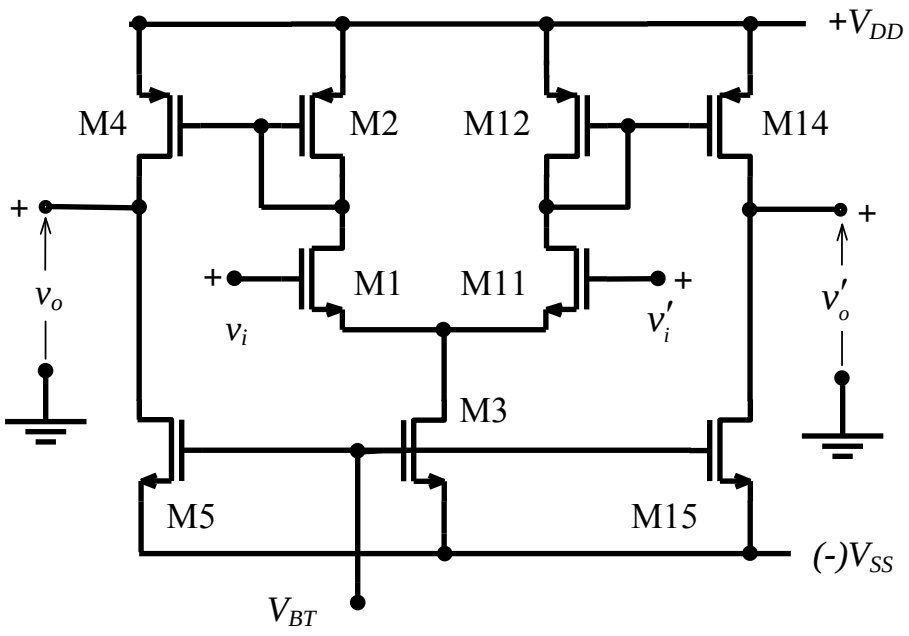
Voltage gains from differential input to single-ended outputs:

$$A_v = \frac{v_o}{(v_i - v_i')} = -\frac{1}{2} g_m \bar{R}_L, \qquad A_v' = \frac{v_o'}{(v_i - v_i')} = \frac{1}{2} g_m \bar{R}_L$$

Voltage gain from differential input to differential output:

$$A_{vd} = \frac{(v_o - v_o')}{(v_i - v_i')} = -g_m \bar{R}_L$$

b) Differential OTA with diff. voltage input, diff. current output:



$$i_o = -Bi_1 = \frac{1}{2} g_m B(v_i - v_i')$$

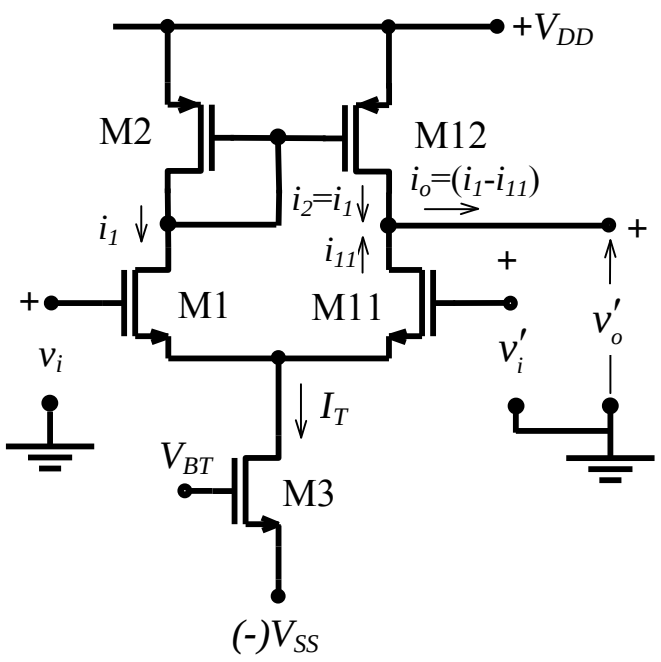
$$i_o' = -Bi_1' = -\frac{1}{2} g_m B(v_i - v_i')$$

The differential transconductance:

$$G_{md} = \frac{(i_o - i_o')}{(v_i - v_i')} = g_m B$$

- Quiescent currents of M4-M5 and M14-M15 are equal.
- Quiescent output voltages are zero.
- Signal currents of M1 and M11 mirrored to M4 and M14.
- Mirroring coefficient : B (not necessarily equal to unity).

c) Differential input, single ended output long-tailed pair:



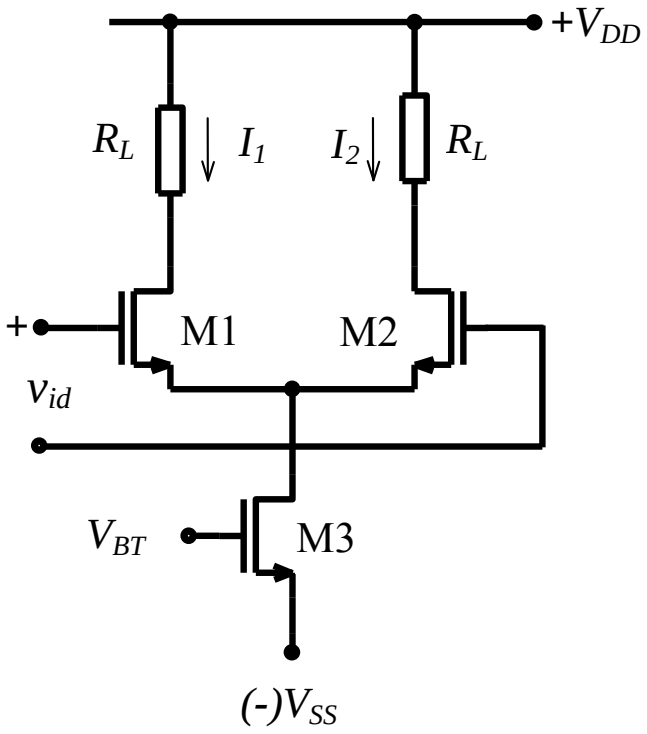
- Signal current of M1 mirrored to M12.
- Load current is the sum of load currents of M2 and M12.
-The output signal voltage:

$$v_o' = 2i_1 R_L' = g_m R_L' (v_i - v_i')$$

$$A_v = \frac{v_o'}{(v_i - v_i')} = g_m R_L'$$

(Widely used as the input stage of op-amps)

The Large Signal Behavior of the Long-Tailed Pair



For $v_{id} = 0$; $\quad I_1 = I_2$

$$I_1 \cong \frac{1}{2}\beta(V_{gs1} - V_T)^2 \ , \quad I_2 \cong \frac{1}{2}\beta(V_{gs2} - V_T)^2$$

$$(V_{gs1} - V_T) \cong \sqrt{\frac{2I_1}{\beta}} \ , \quad (V_{gs2} - V_T) \cong \sqrt{\frac{2I_2}{\beta}}$$

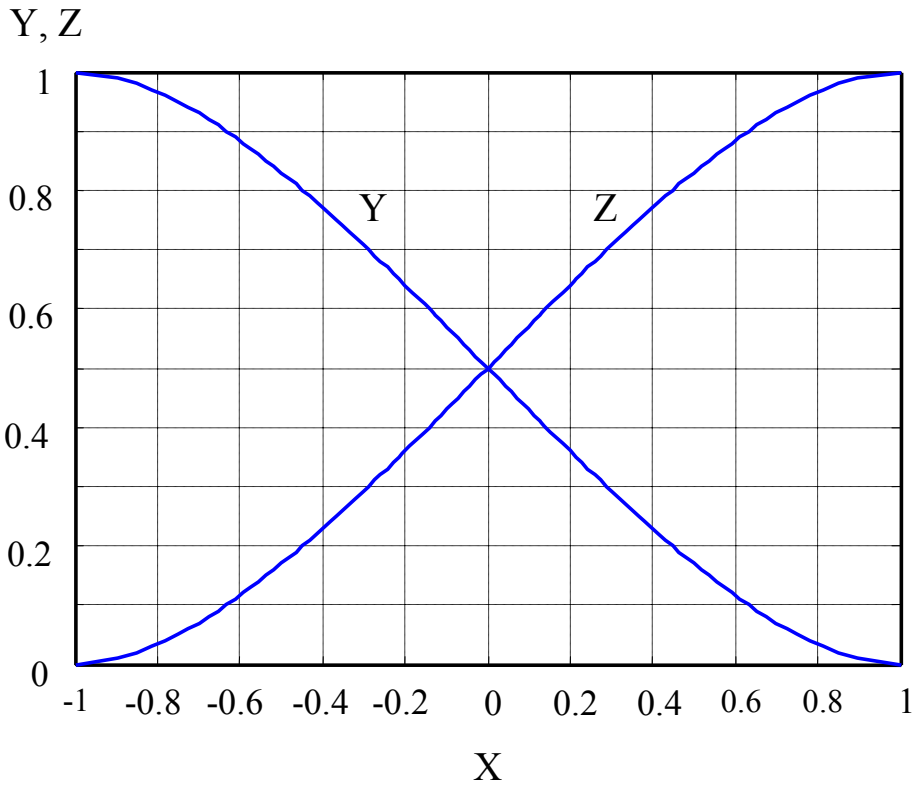
The differential input voltage;

$$v_{id} = V_{g1} - V_{g2} = V_{gs1} - V_{gs2} = \sqrt{\frac{2I_1}{\beta}} - \sqrt{\frac{2I_2}{\beta}}$$

For $v_{id} \neq 0$; $\quad I_2 = I_T - I_1$

$$\frac{v_{id}}{\sqrt{2I_T / \beta}} = \sqrt{\frac{I_1}{I_T}} - \sqrt{1 - \frac{I_1}{I_T}}$$

Variations of I_1 and I_2, normalized to I_T as a function of the differential input voltage



$$X = v_{id} / \sqrt{2I_T / \beta}, \quad Y = I_1 / I_T, \quad Z = 1 - Y$$

Note that; for $v_{id} = +\sqrt{2I_T / \beta}$, the tail current is completly switched to M1,

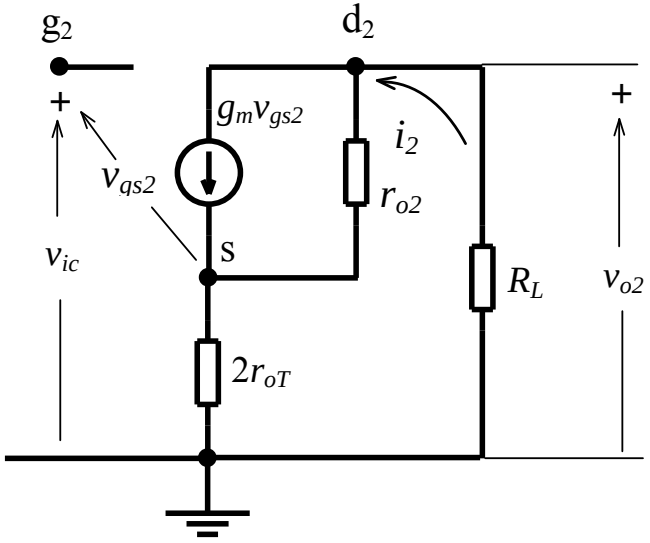
for $v_{id} = -\sqrt{2I_T / \beta}$, the tail current is completly switched to M2.

The common-mode gain of a differential amplifier

- The tail current source of a differential amplifier is never ideal; has a finite internal resistance.

- If a same signal (the common mode input signal) is applied to both of the inputs, an output voltage appears at both outputs.

- The ratio of this output voltage to the common mode input voltage is called as the "common mode gain" of the amplifier; v_{o2} / v_{ic} or v_{o1} / v_{ic}



- The common mode gain can be calculated as

$$A_{vc} = \frac{v_{o2}}{v_{ic}} = -g_m R_L \frac{1}{(1+2r_{oT}g_m) + \frac{2r_{oT}+R_L}{r_{o2}}} \approx -\frac{R_L}{2r_{oT}}$$

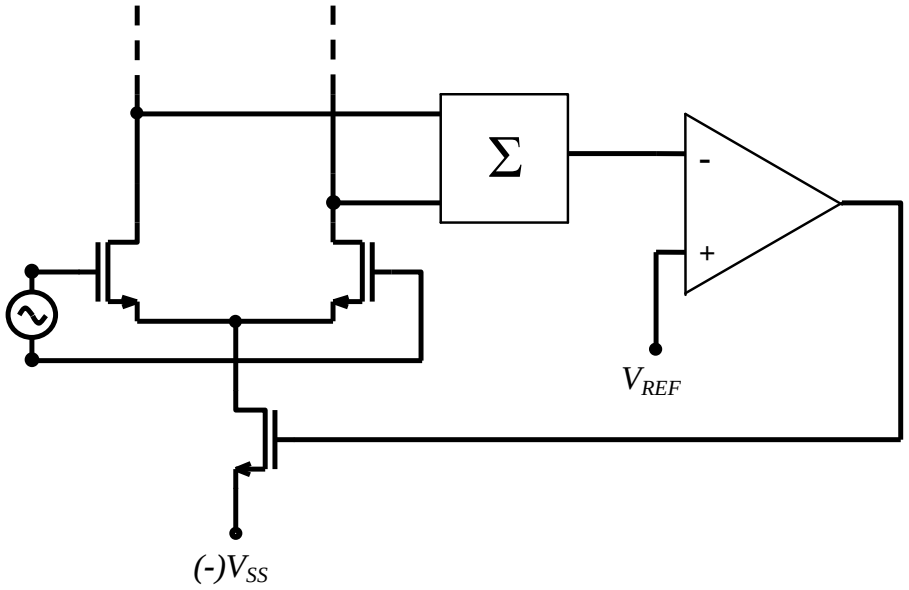
- If the input signals are different but have a common component, the voltage at an output node is the sum of a common mode signal related component and a differential signal related component.

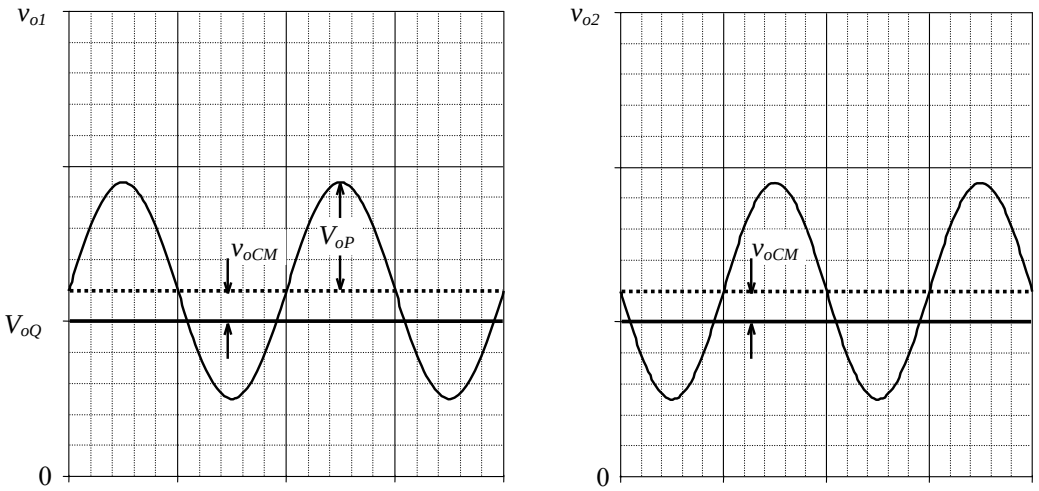
- The ratio of the differential gain to the common mode gain is called as the "Common-Mode Rejection Ratio" (CMRR):

$$CMRR = \frac{A_{vd}}{A_{vc}} \approx 2g_m r_{oT}$$

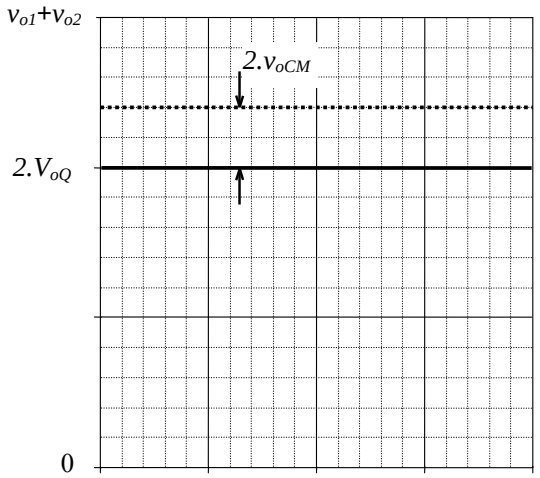
The Common Mode Feedback

The CMFB helps to eliminate the common-mode components at the outputs, as well as to clamp the DC voltages of the output nodes to a reference value.

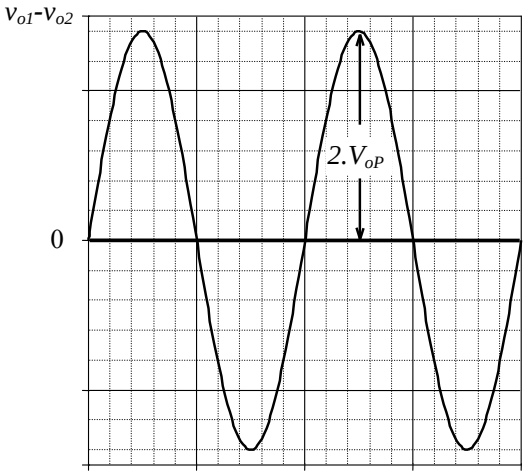




The output voltages with their diff. and C.M. components



Sum of the output voltages used as the feedback signal



The differential output voltage