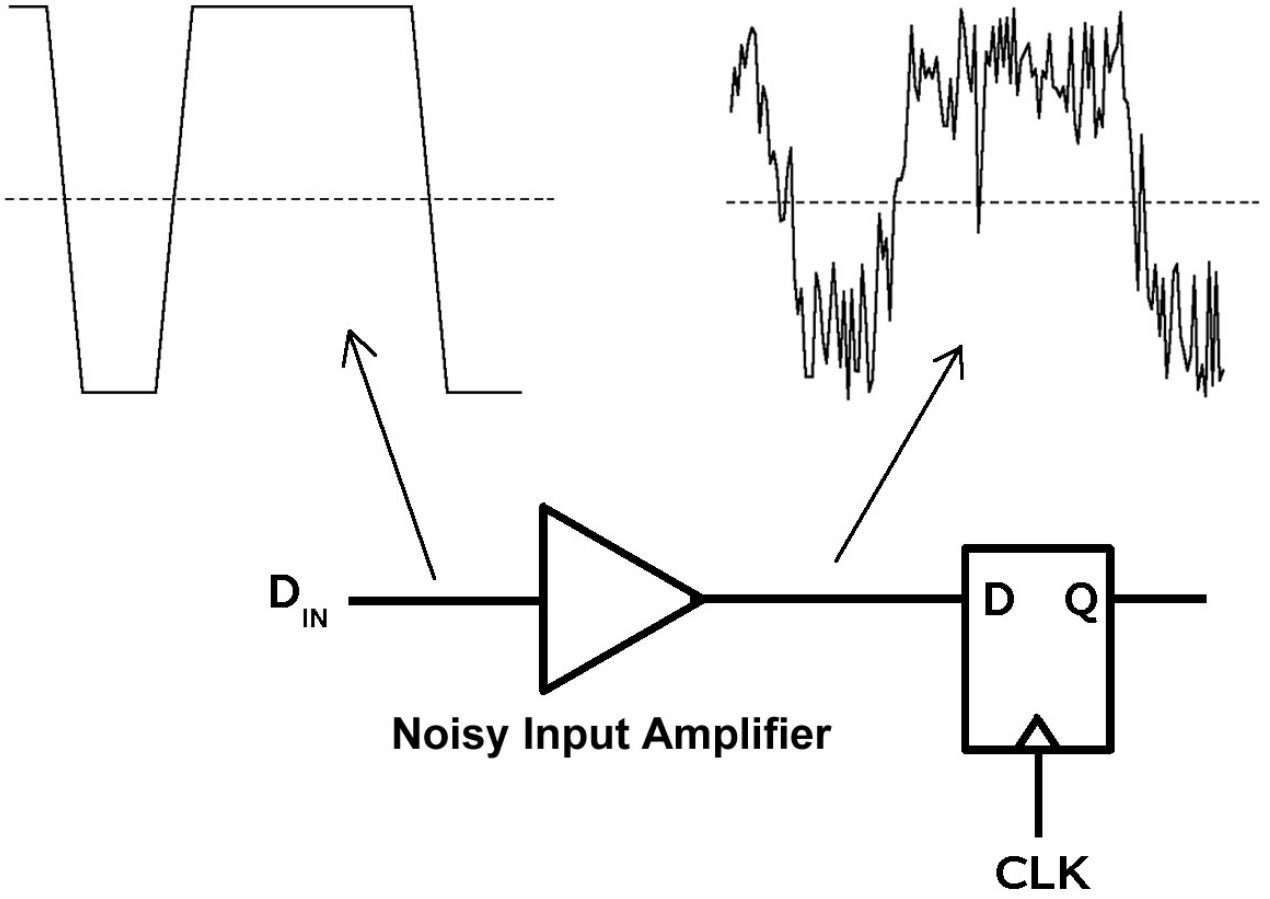
8. Broadband LNA/TIA Design

Outline

- Broadband LNAs
  - Applications of TIAs
  - TIA design methodology
  - TIA circuit examples

Typical problem in broadband systems



Applications of broadband LNAs in HF systems

- Low-noise broadband amplifiers in **optical receivers**: signal source photodiode
  - **Goal:** Minimize the noise of the TIA-Photodiode ensemble while maximizing bandwidth and minimizing power

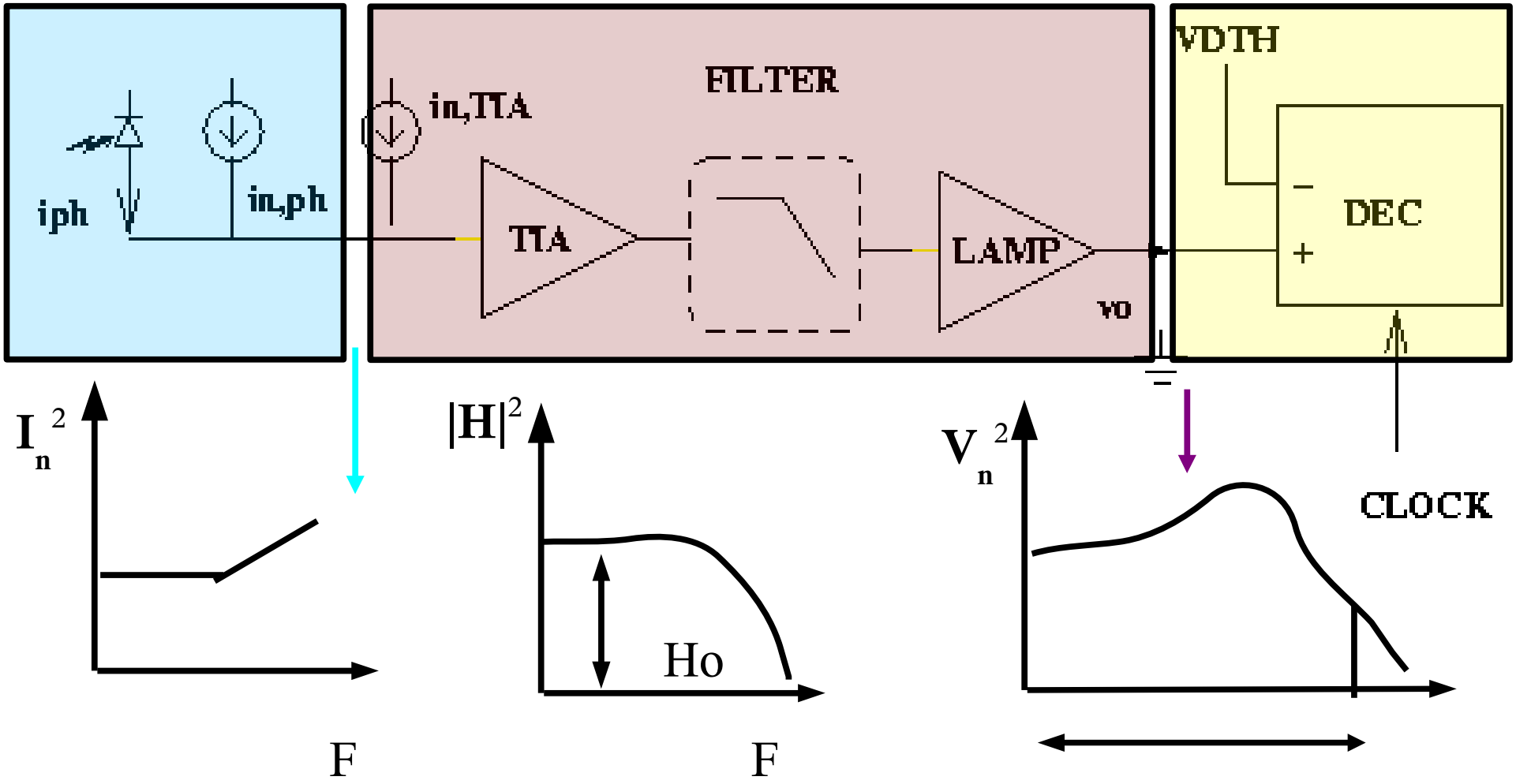
$$FoM = \frac{Z_T \cdot I_{max} \cdot BW_{3dB}}{i_{neq}^{rms} P}$$

- Low noise broadband input comparators in **backplane communications, UltraWideBand (UWB) radio** and **high speed ADCs**: 50Ω signal source

$$FoM = \frac{A_V \cdot V_{imax} BW_{3dB}}{v_{neq}^{rms} P}$$

  - **Goal**: Minimize noise in 50-Ohm system e.g. minimum input amplitude of broadband data: 10 mVpp at 40 Gb/s

Typical short-reach fiberoptic receiver



General observations

Problem

Either the real part of the input impedance or the real part of the noise impedance, or both, are frequency dependent.

Consequence

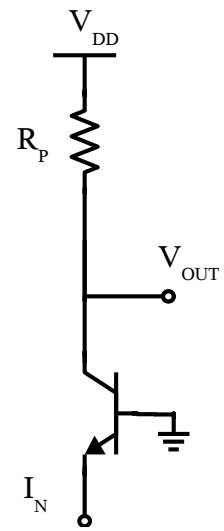
Cannot match both simultaneously over broad bandwidth without compromising F_{MIN}!

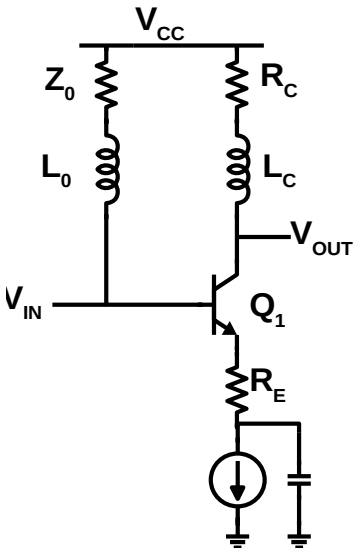
Solution

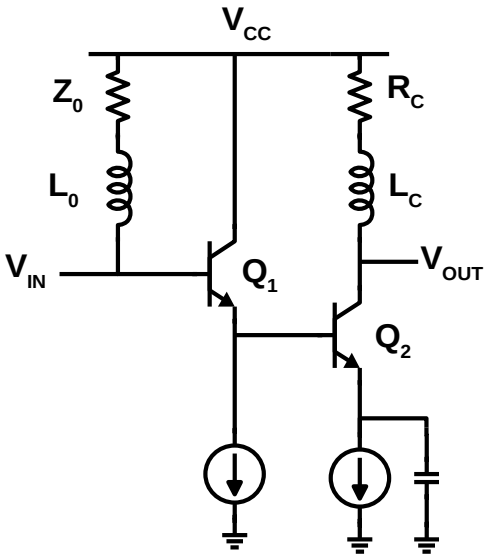
Use lossy feedback to accomplish both with minimal damage.

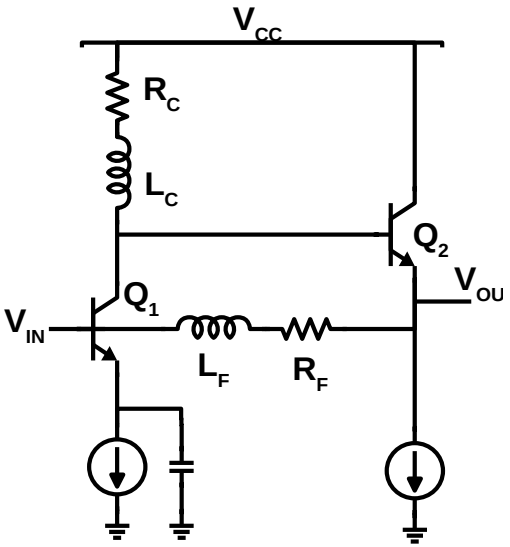
Shunt feedback is best because it minimizes power dissipation

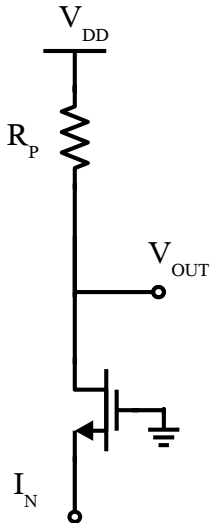
Low-noise broadband amplifiers

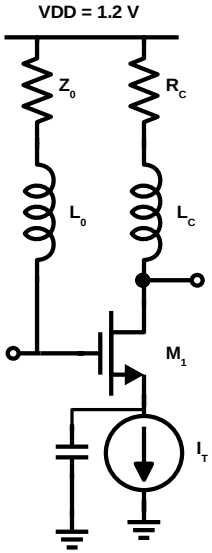


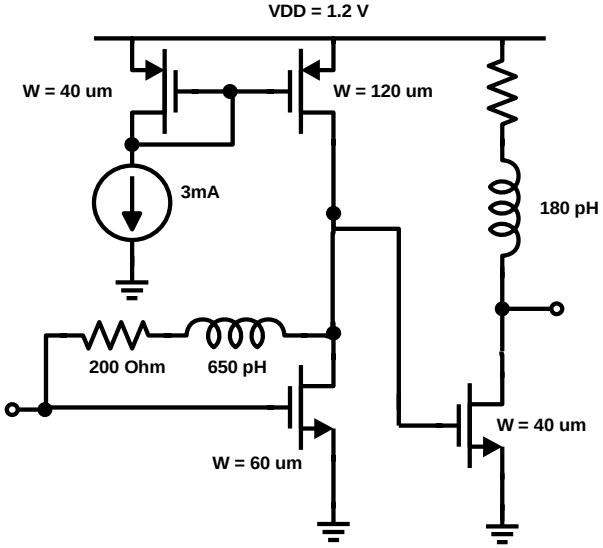


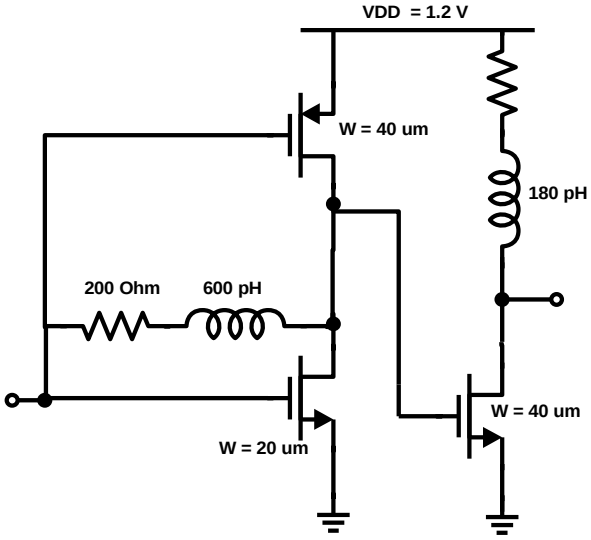










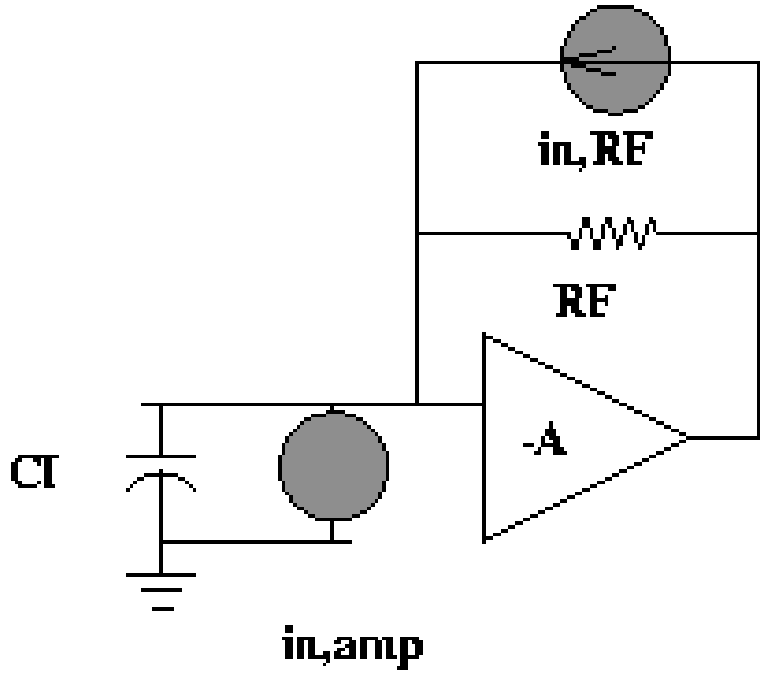


TIA signal path analysis: infinite bandwidth amp

$$Z_T(s) = \frac{-R_T}{1 + s/\omega_p}$$

$$R_T = \frac{A}{A+1} R_F \qquad \omega_p = \frac{A+1}{R_F C_T}$$

$$C_T = C_I + C_D$$



Single-pole, finite bandwidth amplifier

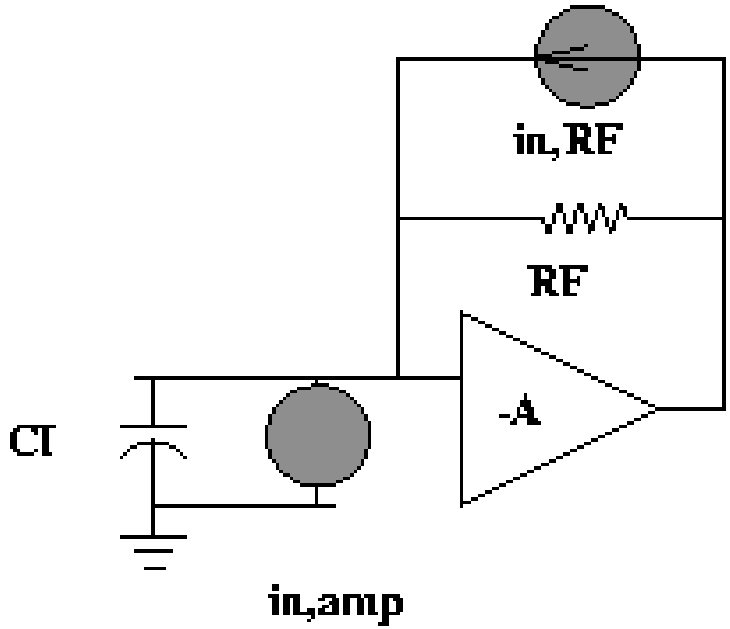
If amplifier has a finite bandwidth f_A , then the two-pole transfer function stability condition (Q=0.707) gives:

$$Z_T(s)=\frac{-R_F\left(\frac{A}{1+A}\right)}{\frac{s^2}{\omega_p\omega_A(1+A)}+s\left(\frac{\omega_p+\omega_A}{\omega_p\omega_A(1+A)}\right)+1}$$

$$f_A>\frac{1}{2\pi}\frac{2A}{R_F C_T}$$

$$BW_{3dB}=\frac{1}{2\pi}\frac{\sqrt{2A(A+1)}}{R_F C_T}$$

$$R_T\leqslant\frac{A f_A}{2\pi C_T BW_{3dB}^{\ 2}}$$



TIA noise matching in 50-Ohm system

$$F_{Zo}=1+R_{NA}Z_0\left|Y_{CORA}+\frac{1}{Z_0}+\frac{1}{R_F}\frac{1-j\,\omega_0}{1+\omega_0^2}\right|^2+Z_0G_{NA}+\frac{Z_0}{R_F}\frac{1}{1+\omega_0^2}$$

$$I_E(W_{OPT})=\frac{1}{\omega}\sqrt{\left(\frac{1}{Z_0}+\frac{1}{R_F}\frac{1}{1+\omega_0^2}\right)^2+\left(\frac{1}{R_F}\frac{\omega_0}{1+\omega_0^2}\right)^2}\sqrt{\frac{1}{\frac{G}{R}+G_C^2+B^2}}$$

$$Z_{IN}=\frac{R_F}{1+\frac{R_C I_T}{V_T}}$$

$$\omega_0=\frac{R_F}{L_F}$$

Finding $I_E(W)_{OPT}$ is equivalent to matching the TIA(HBT) noise impedance to 50Ω at ω.

Algorithmic design methodology for broadband low-noise TIAs

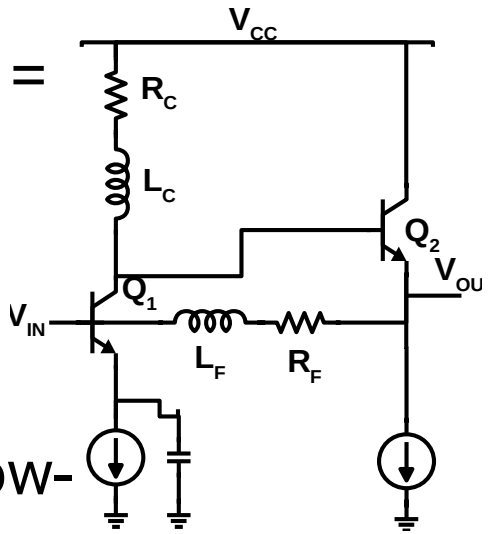
1. Bias HBT(MOSFET) at optimal noise current density J_{OPT} (0.15 mA/μm) at amplifier's BW_{3dB}

2. Choose the DC voltage drop across R_C for linearity requirements. This fixes the loop gain A = $g_m R_C$ (=$g_m r_o$)

3. Set the feedback resistance R_F for 50Ω input match.

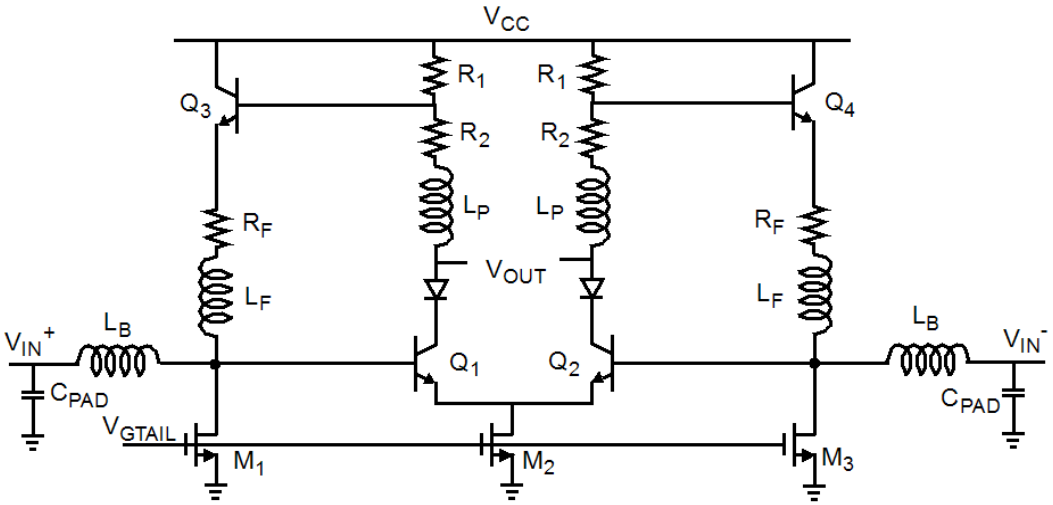
4. Size the emitter length (gate width) of Q1 for low-noise, using the equation from the previous slide.

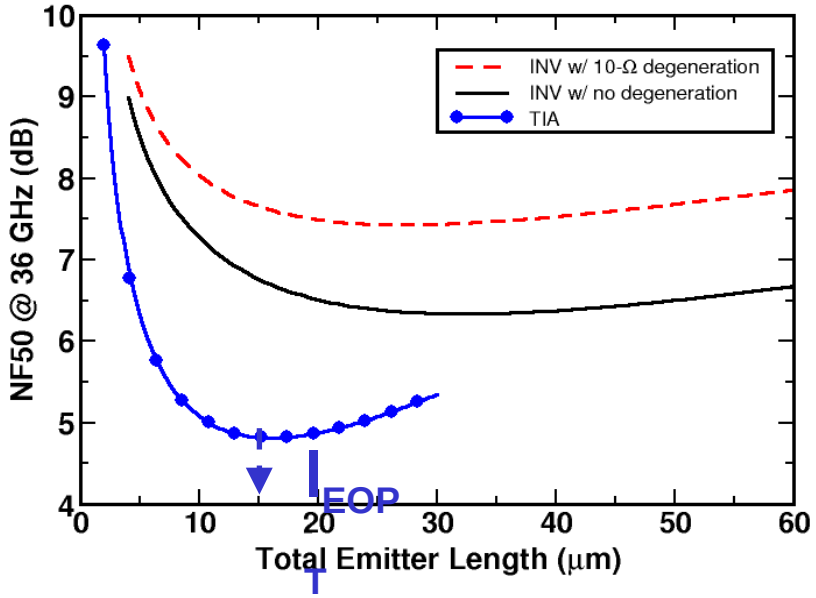
5. Add inductors to extend bandwidth and filter high-frequency noise.



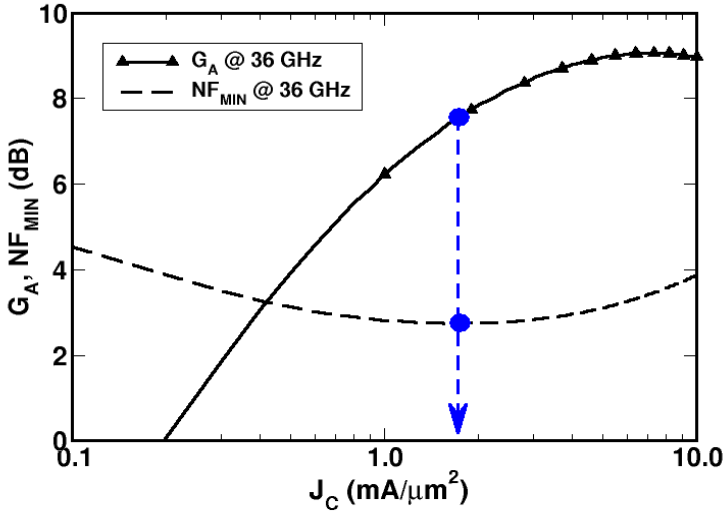
50Ω, 43-Gb/s SiGe HBT TIA

(T.Dickson et al., JSSC, Aug.-06)



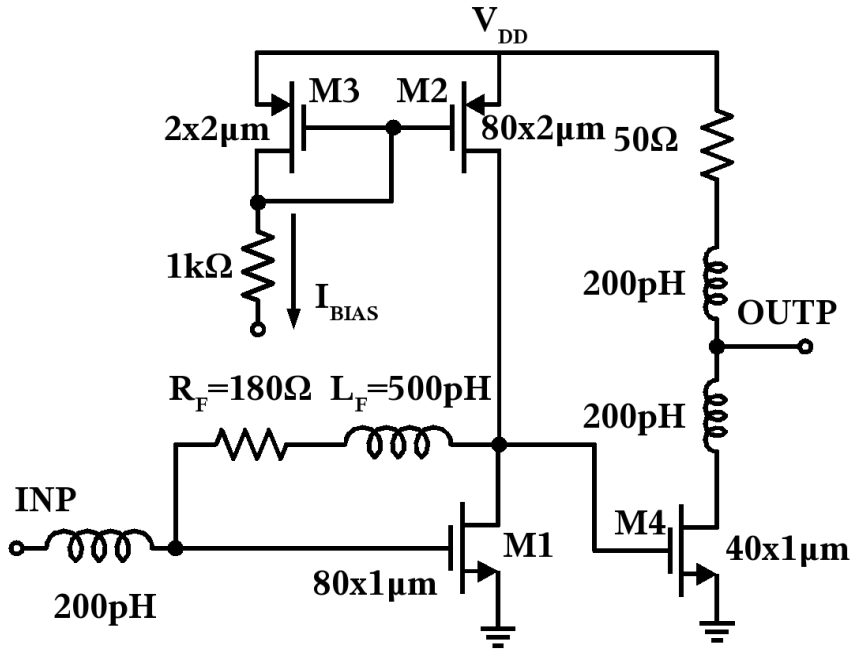


- J_{opt} at GHz =1.5mA/μm²
- I_T= 8mA, $I(Q_{1,2})$ = 2 ×$I(Q_{3,4})$=4mA
- $Q_{1,2,3,4}$=2x0.17μmx8μm
- R_1= R_2= 27Ω, R_F= 260 Ω
- A = $g_m(R_1+R_2)/2$ = 4.2



Example: 90-nm n-MOS TIA

- Bias at min. noise current density 0.15 mA/μm.
- p-MOS active load to increase gain at low V_{DD}.
- Feedback inductor L_F resonates out the capacitance at the TIA node and helps improve BW
- L_F =500pH designed for high SRF.



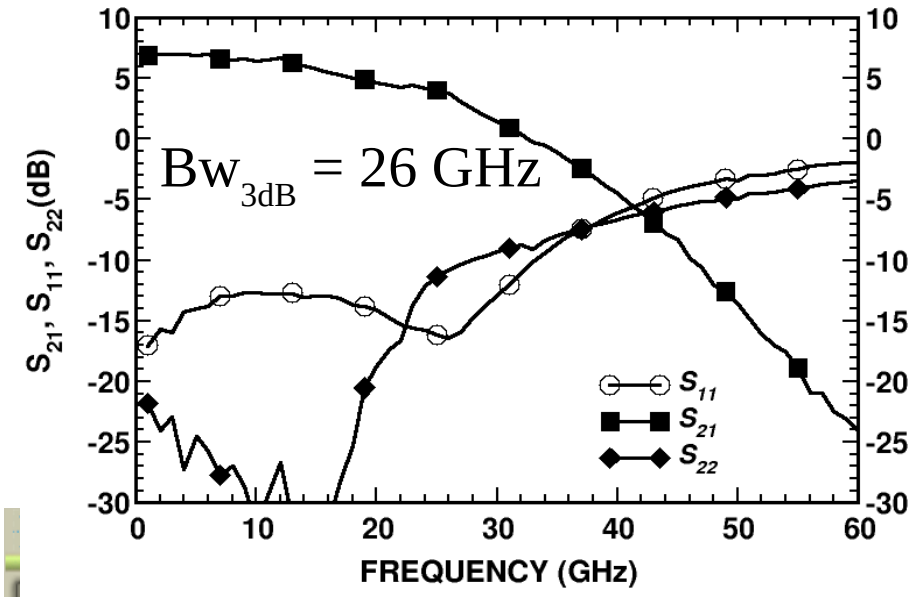
$$Z_{IN}=\frac{R_F}{1+A}=\frac{180}{2.92}=60.8\Omega$$

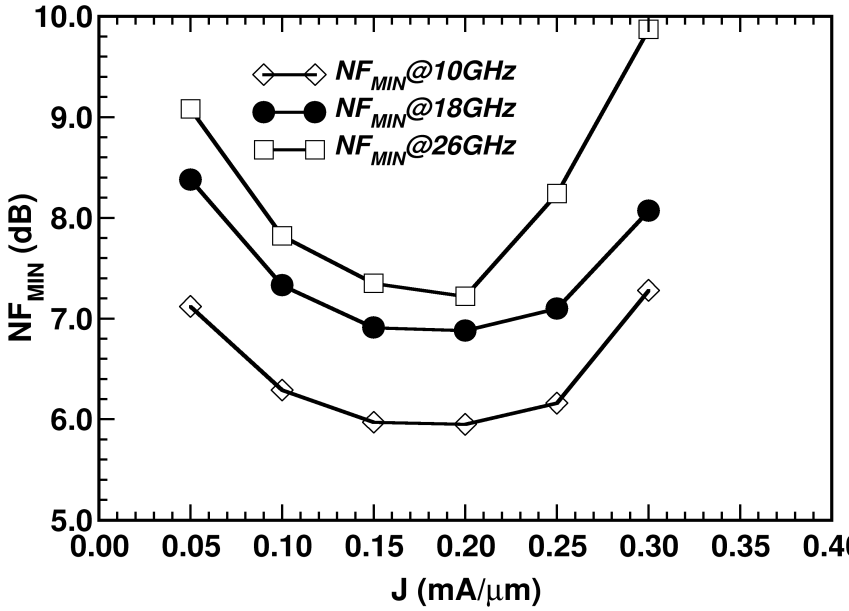
$$A=\frac{g_{m1}}{g_{o1}+g_{o2}+\frac{1}{R_F}}=\frac{80mS}{12mS+24mS+5.55mS}=1.92$$

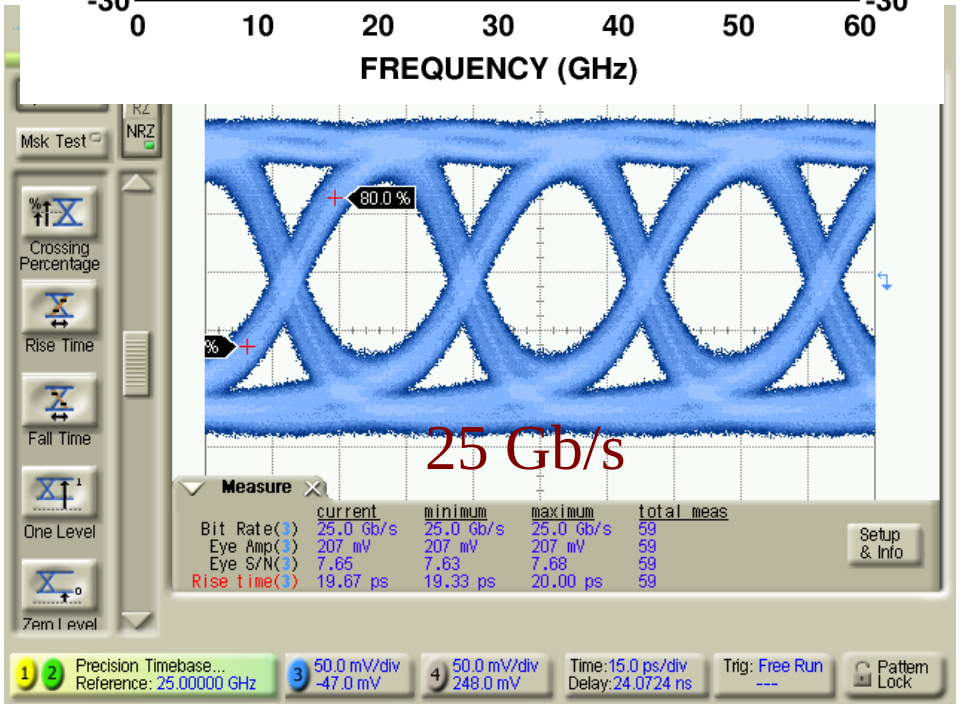
$$C_{IN}=C_{gs1}+(1+A)C_{gd1}=(2.5fF/um)\times 80um=200fF$$

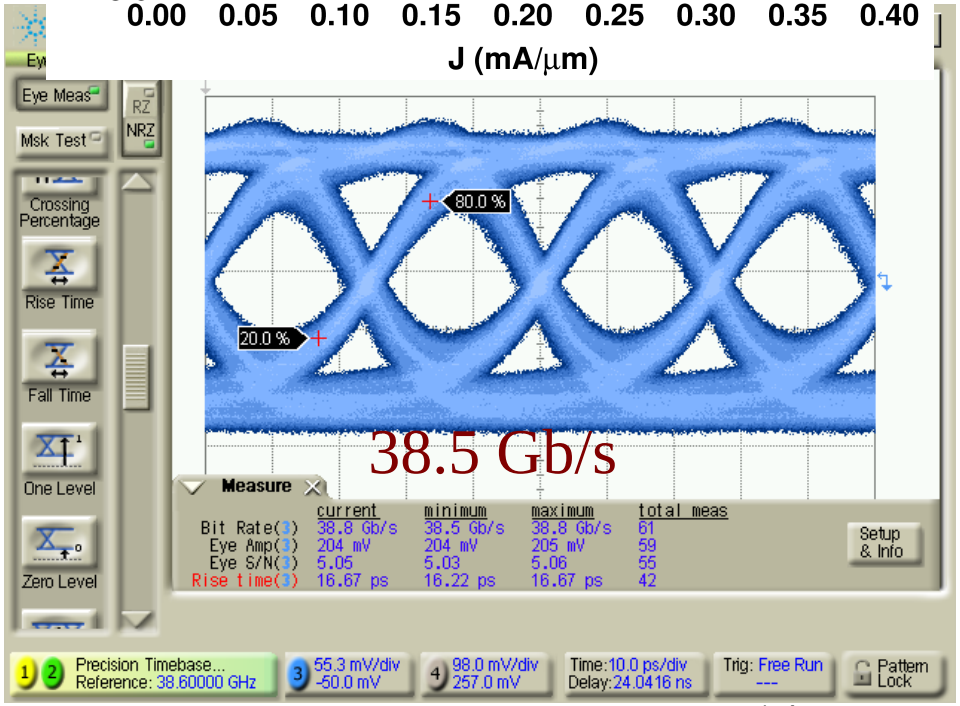
$$C_{out}=C_{db1}+C_{gd1}+C_{gd2}+C_{db2}+C_{gs3}+2C_{gd3}=120+40+80+320+40+40=640fF$$

90-nm CMOS TIA (T. Dickson et al. JSSC-Aug.06)

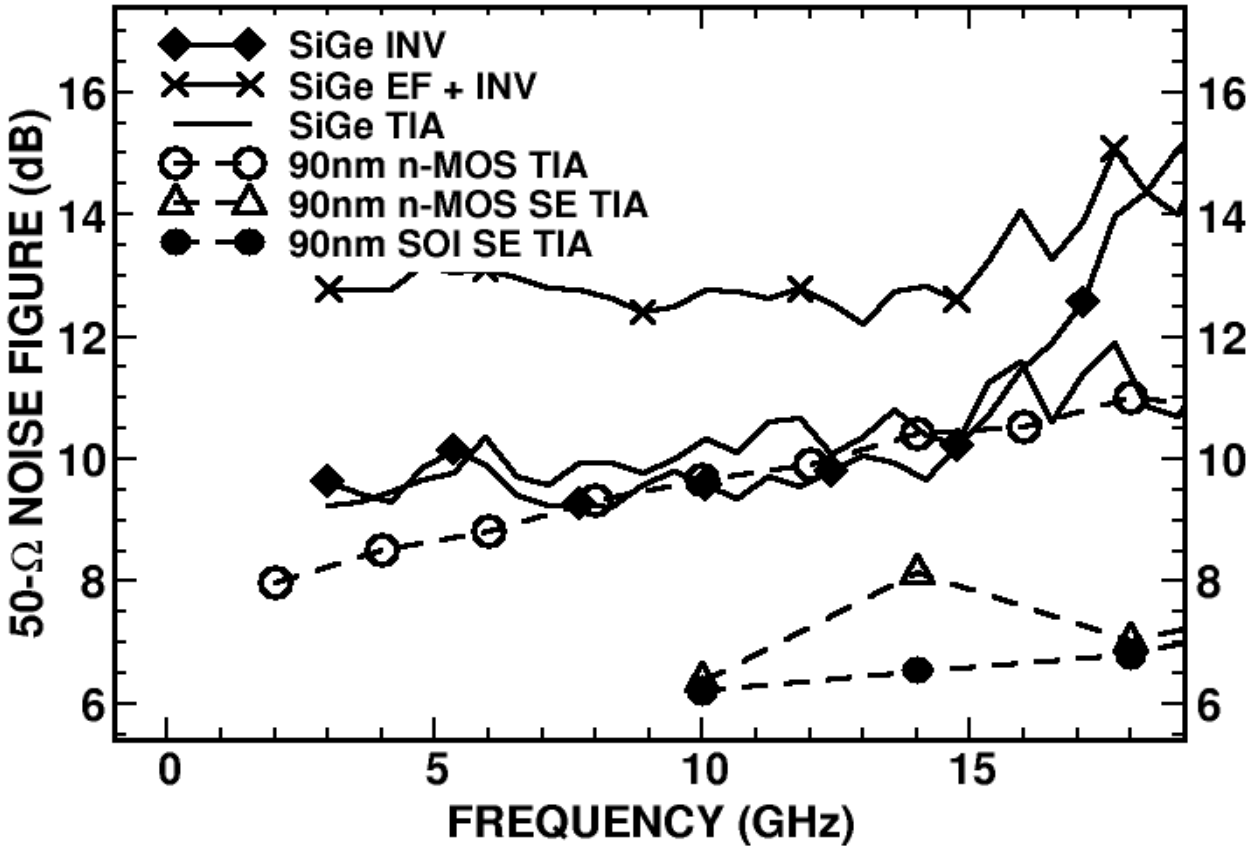








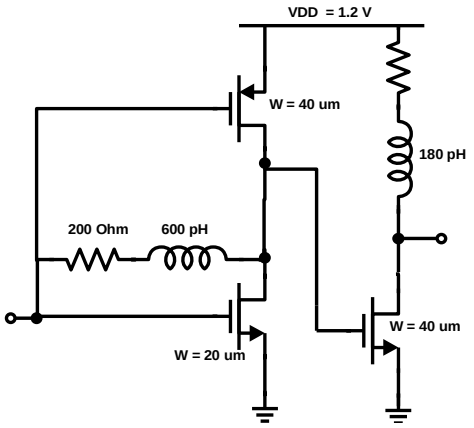
Noise Figure comparison of TIAs

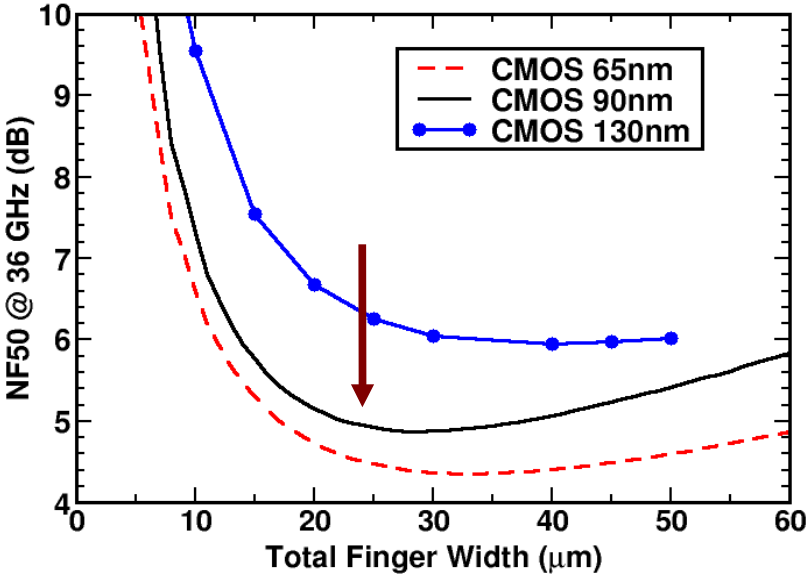


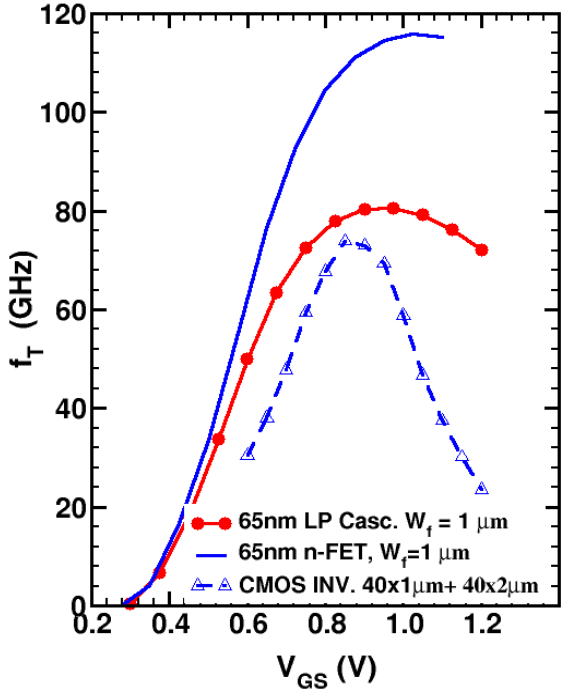
MOSFET TIAs exhibit lower noise than SiGe HBT TIAs

Broadband CMOS LNA topology scaling

- f_T of 65-nm CMOS inv = n-MOS cascode f_T
- MOSFETs biased at 0.15 mA/μm
- Size and current of MOS TIA do not change with technology nodes
- Noise and bandwidth improve as technology scales

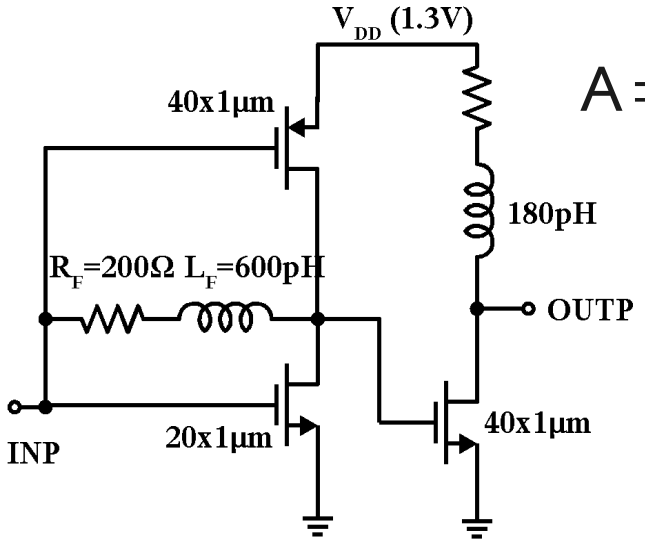






65-nm LP CMOS vs. n-MOS TIAs

(T. Chalvatzis et al. JSSC Aug. 2007)



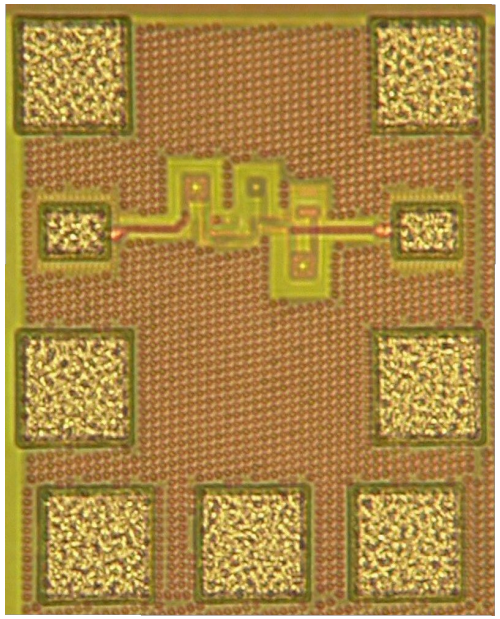
$$A = \frac{g_{m1} + g_{m2}}{g_{o1} + g_{o2} + \frac{1}{R_F}} = \frac{40\text{mS}}{3\text{mS} + 6\text{mS} + 5\text{ms}} = 2.85$$

$$Z_{IN} = \frac{R_F}{1 + A} = \frac{200}{3.85} = 52\Omega$$

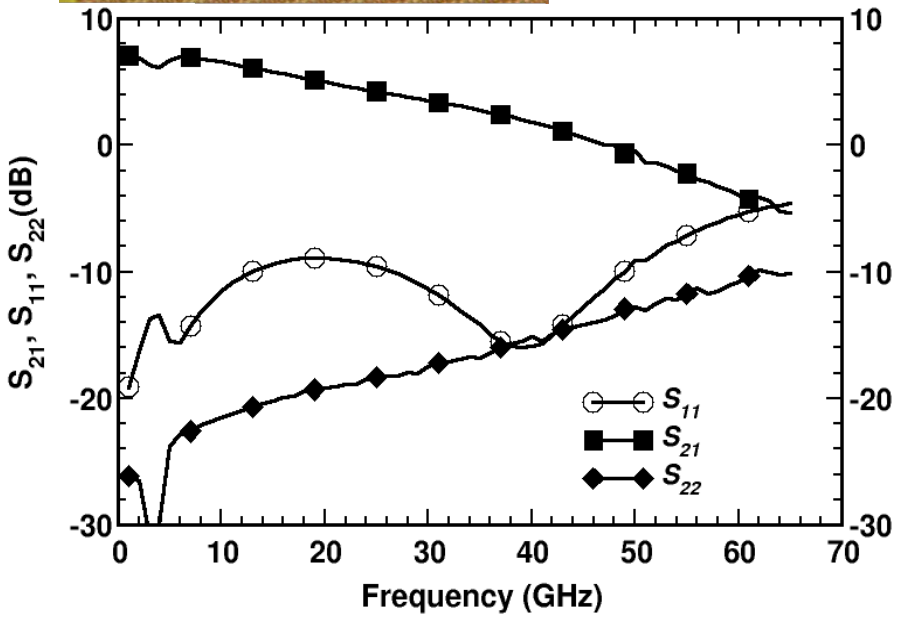
$$C_{IN} = C_{gs1} + C_{gs2} + (1 + A)(C_{gd1} + C_{gd2}) = 20\text{fF} + 40\text{fF} + 3.85 \times 30\text{fF} = 175.5\text{fF}$$

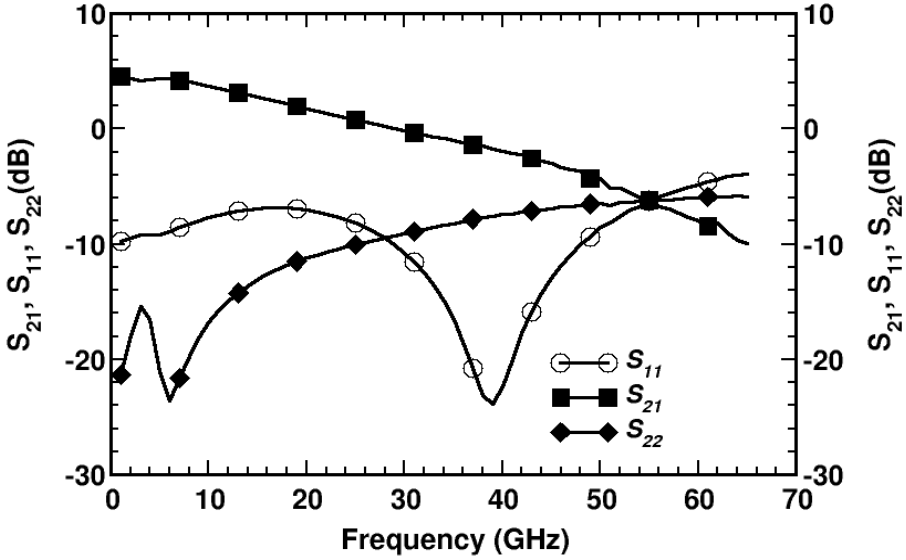
$$C_{out} = C_{db1} + C_{gd1} + C_{gd2} + C_{db2} + C_{gs3} + 2C_{gd3} = 30 + 10 + 20 + 60 + 40 + 40 = 200\text{fF}$$

65-nm LP CMOS vs. n-MOS TIAs

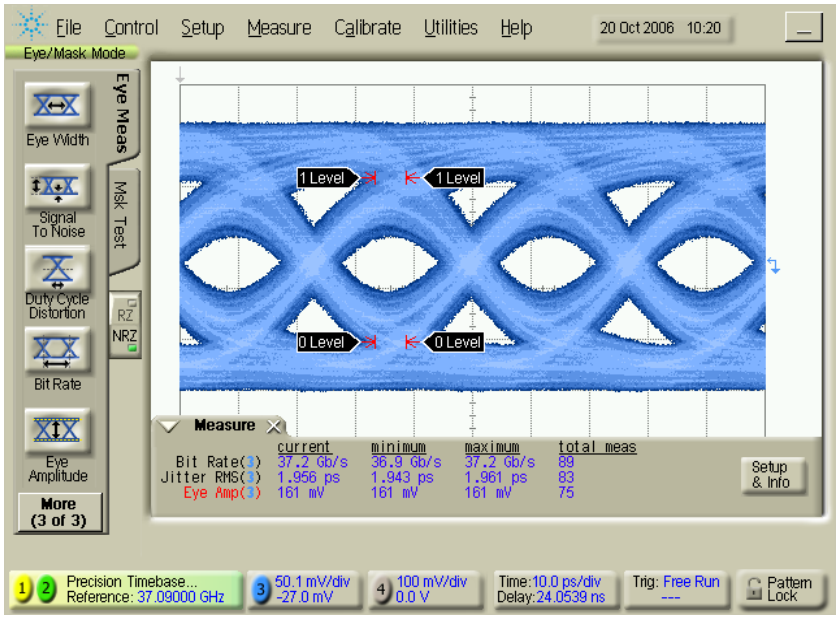


- CMOS vs. n-MOS
- 3.9 mW 14.4 mW
- 28 GHz 21 GHz

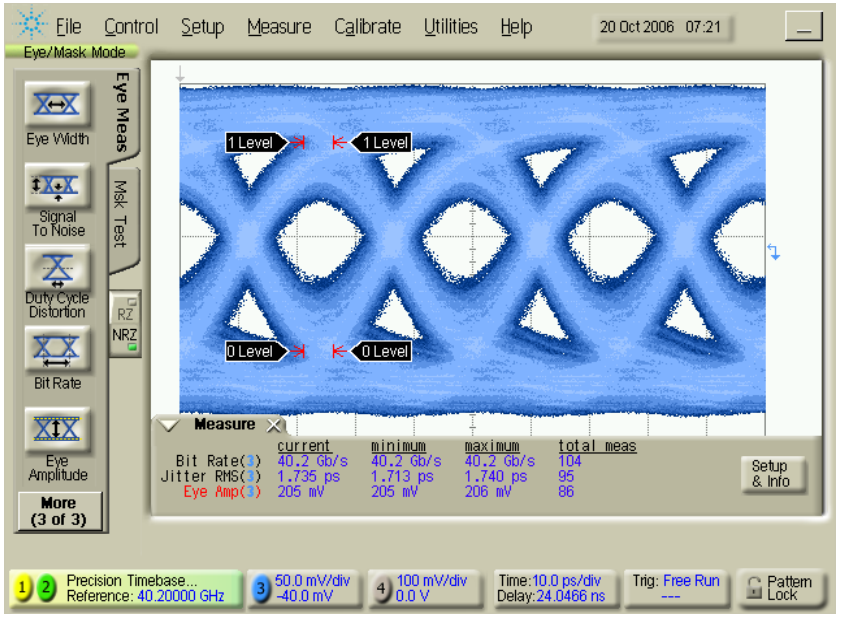




65-nm LP n-MOS vs CMOS TIAs (cont'd)

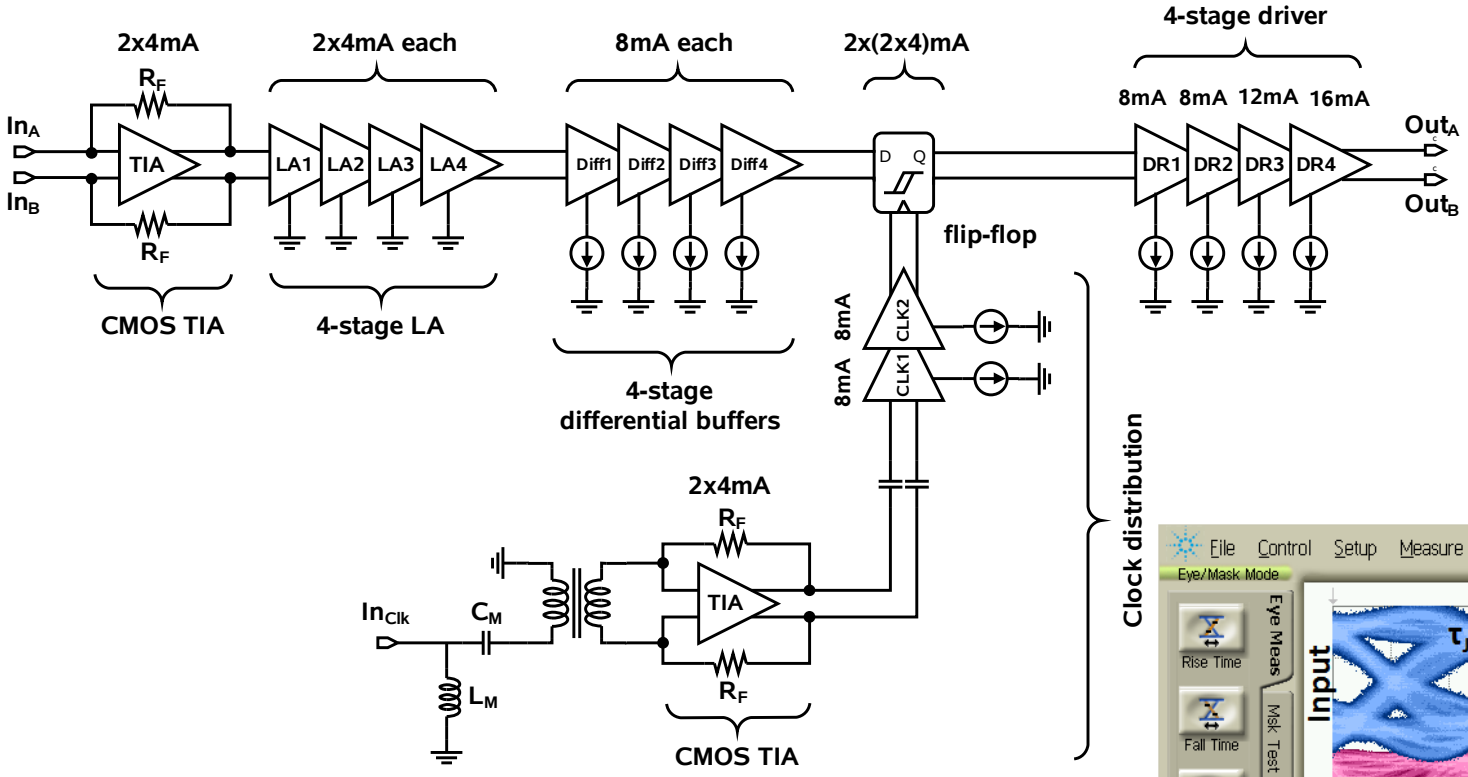


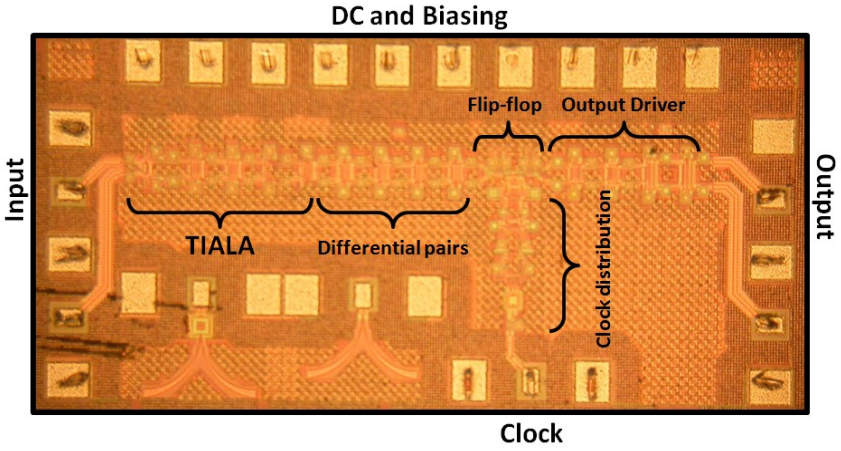
n-MOS: 37 Gb/s

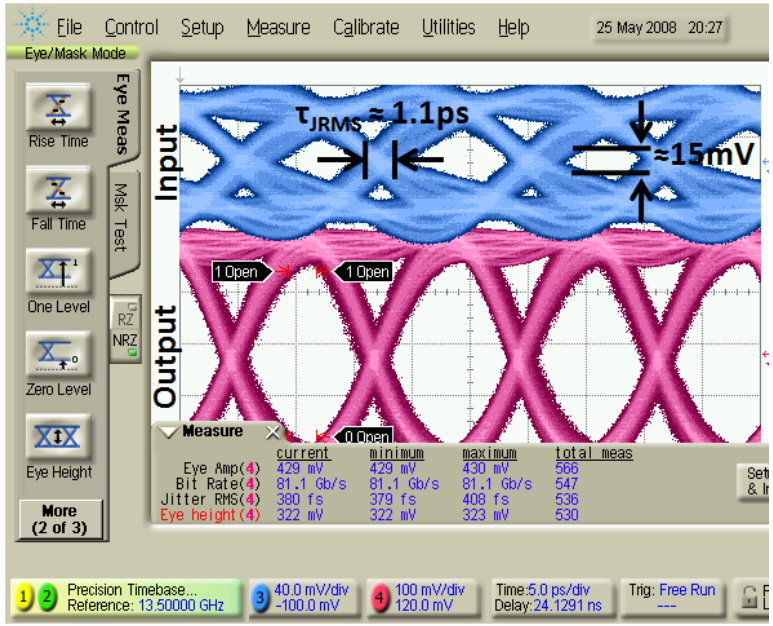


CMOS: 40 Gb/s

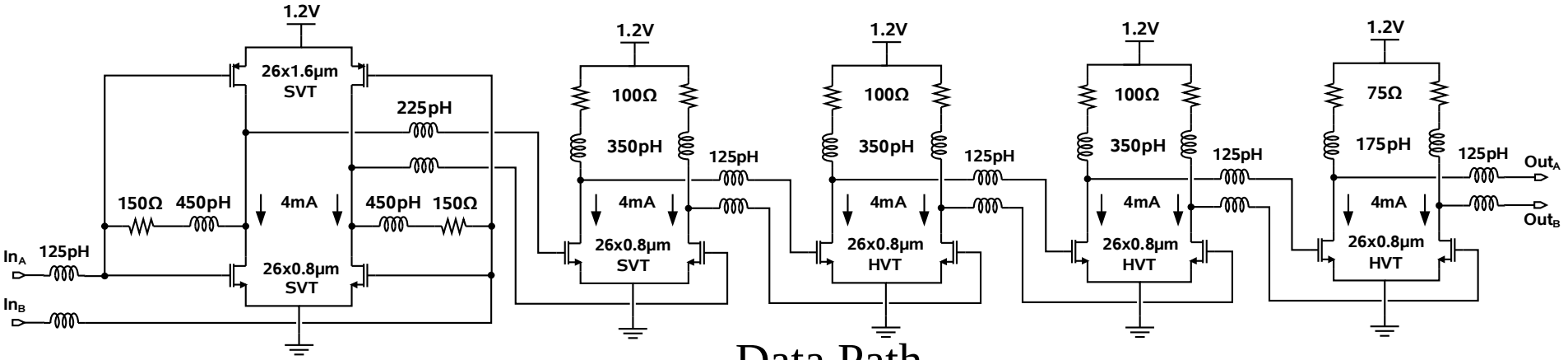
81-Gb/s retimer (S. Shahramian , CSICS 2008)



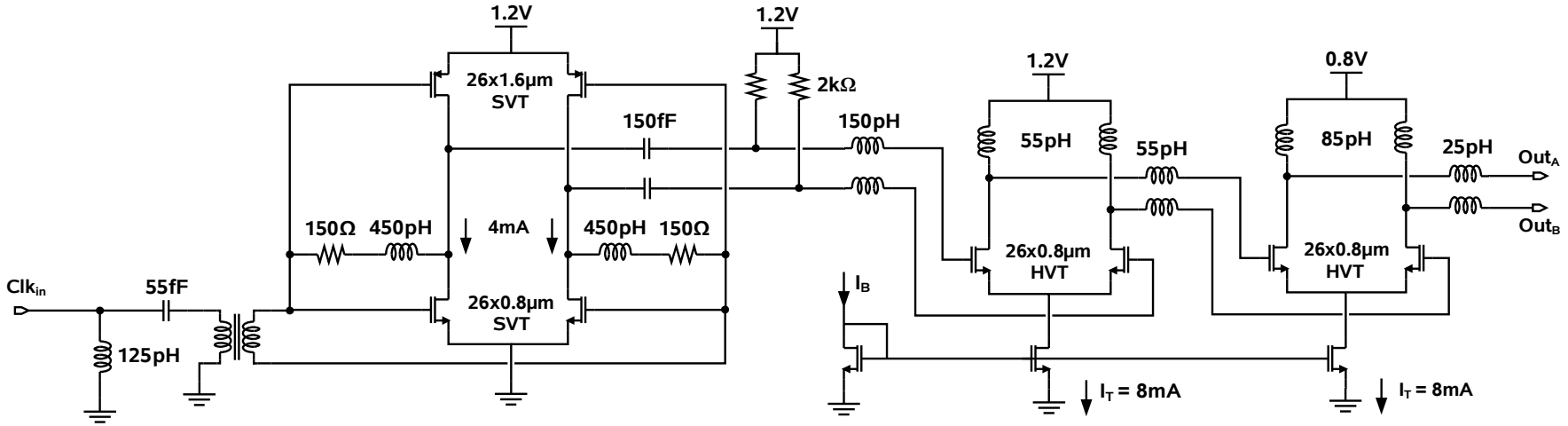




65-nm bulk p-MOSFETs at 80 Gbs/GHz

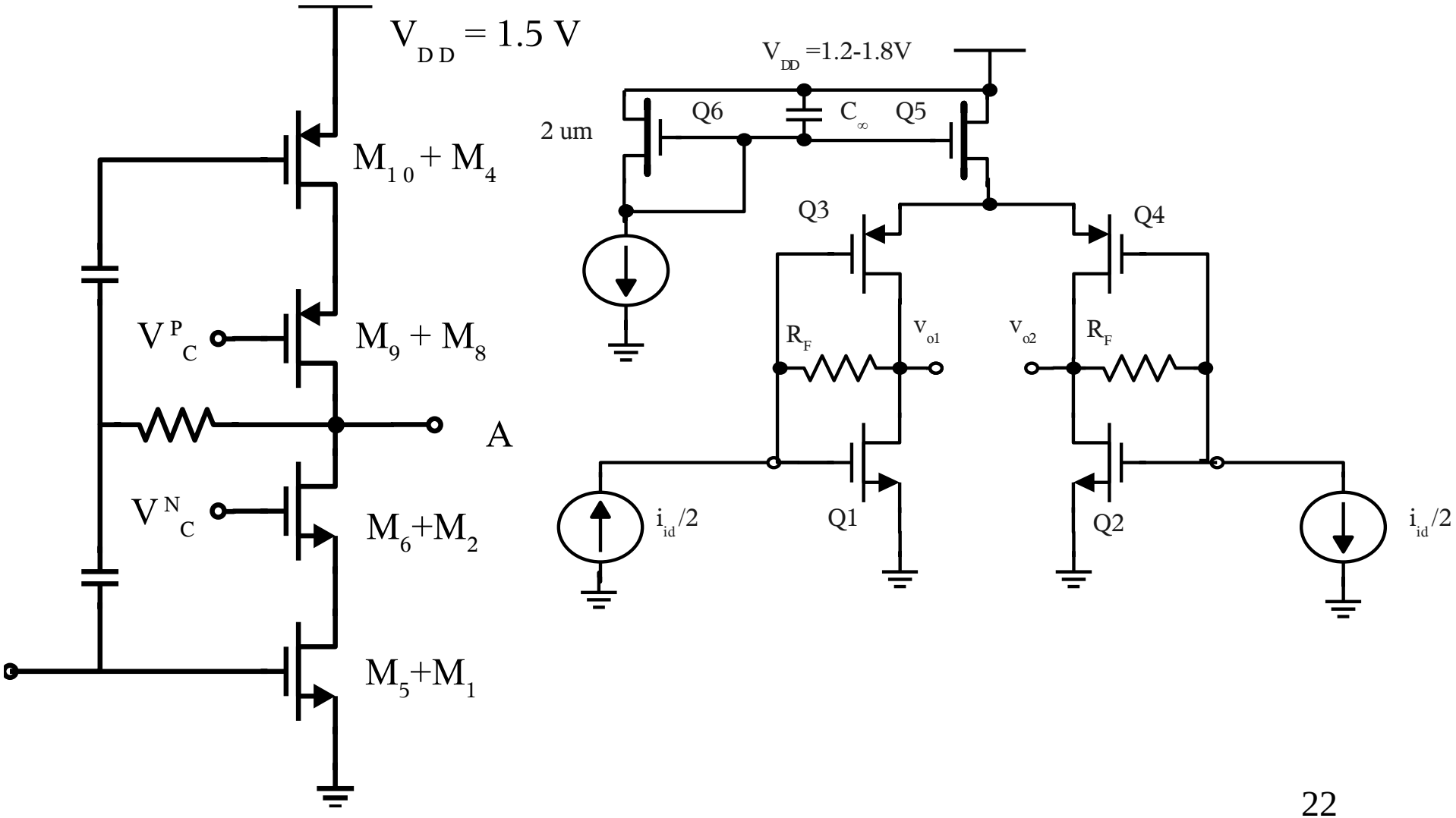


Data Path



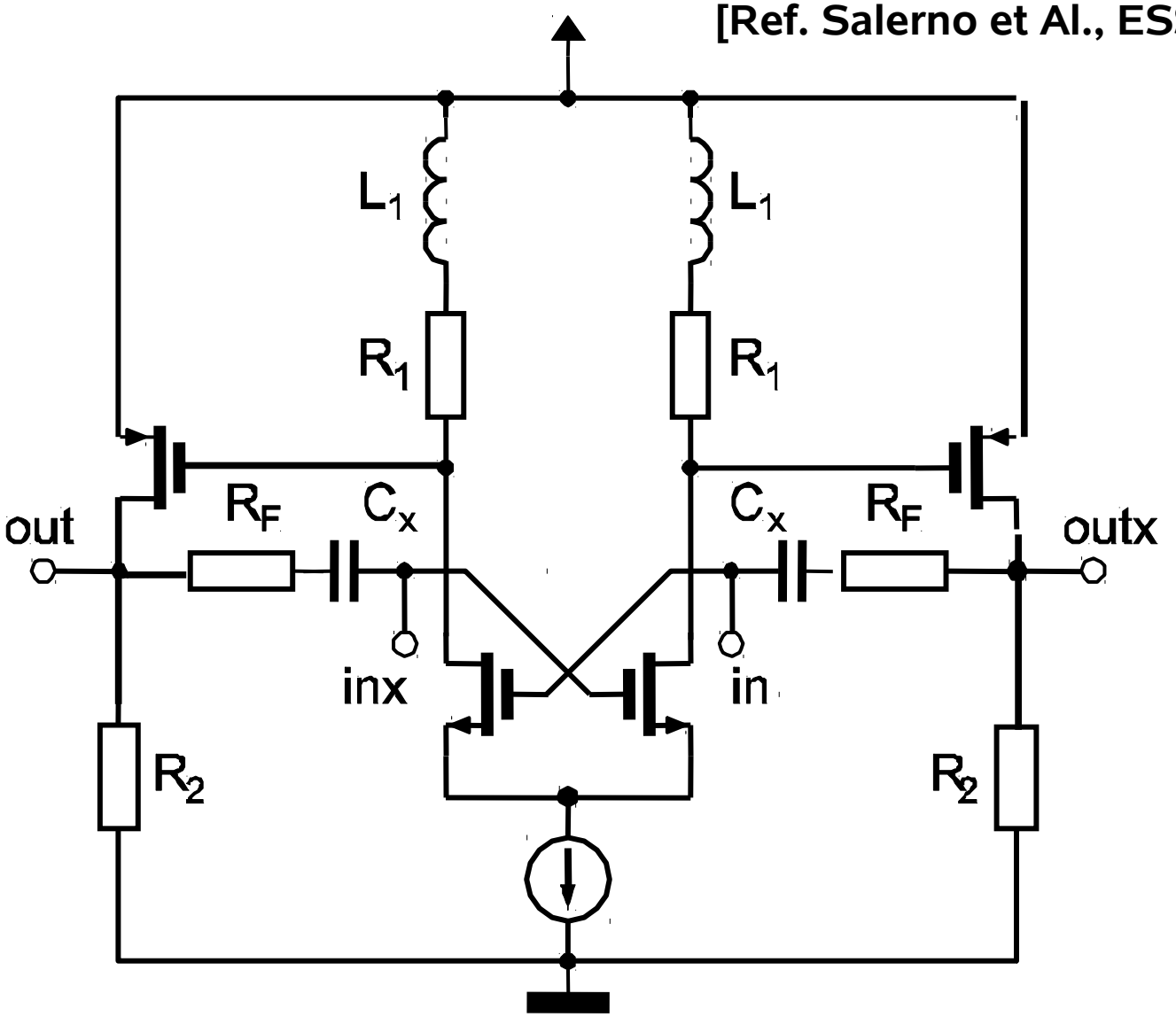
Clock path

Cascoded and diff. CMOS TIA topologies

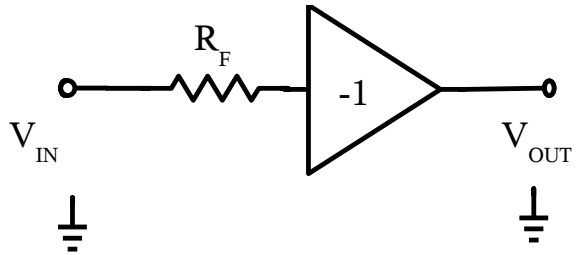


UWB LNA: Marc Tibout (Infineon), CSICS-06 Short Course

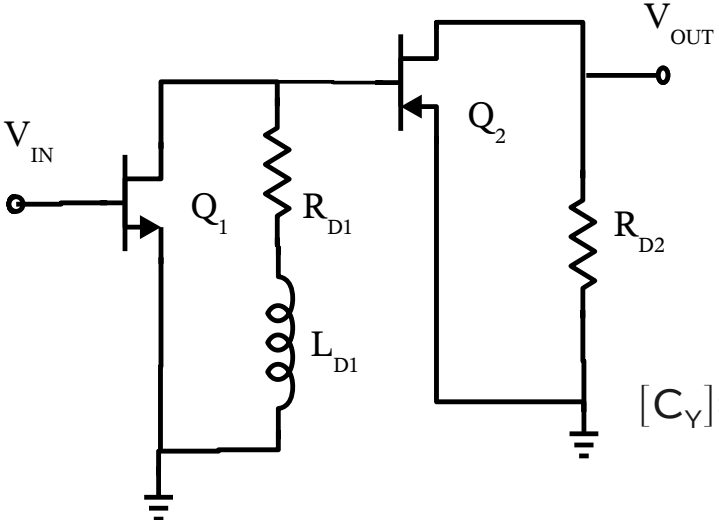
[Ref. Salerno et Al., ESSCIRC, Sep. 2005]



Diff. mode half-ckt. for feedback and amplifier networks



$$[Y]=\begin{bmatrix}\frac{1}{R_F} & \frac{1}{R_F}\\ \frac{1}{R_F} & \frac{1}{R_F}\end{bmatrix} \qquad [C_Y]=4kT\Delta f\,\Re[Y]=4kT\Delta f\begin{bmatrix}\frac{1}{R_F} & \frac{1}{R_F}\\ \frac{1}{R_F} & \frac{1}{R_F}\end{bmatrix}$$



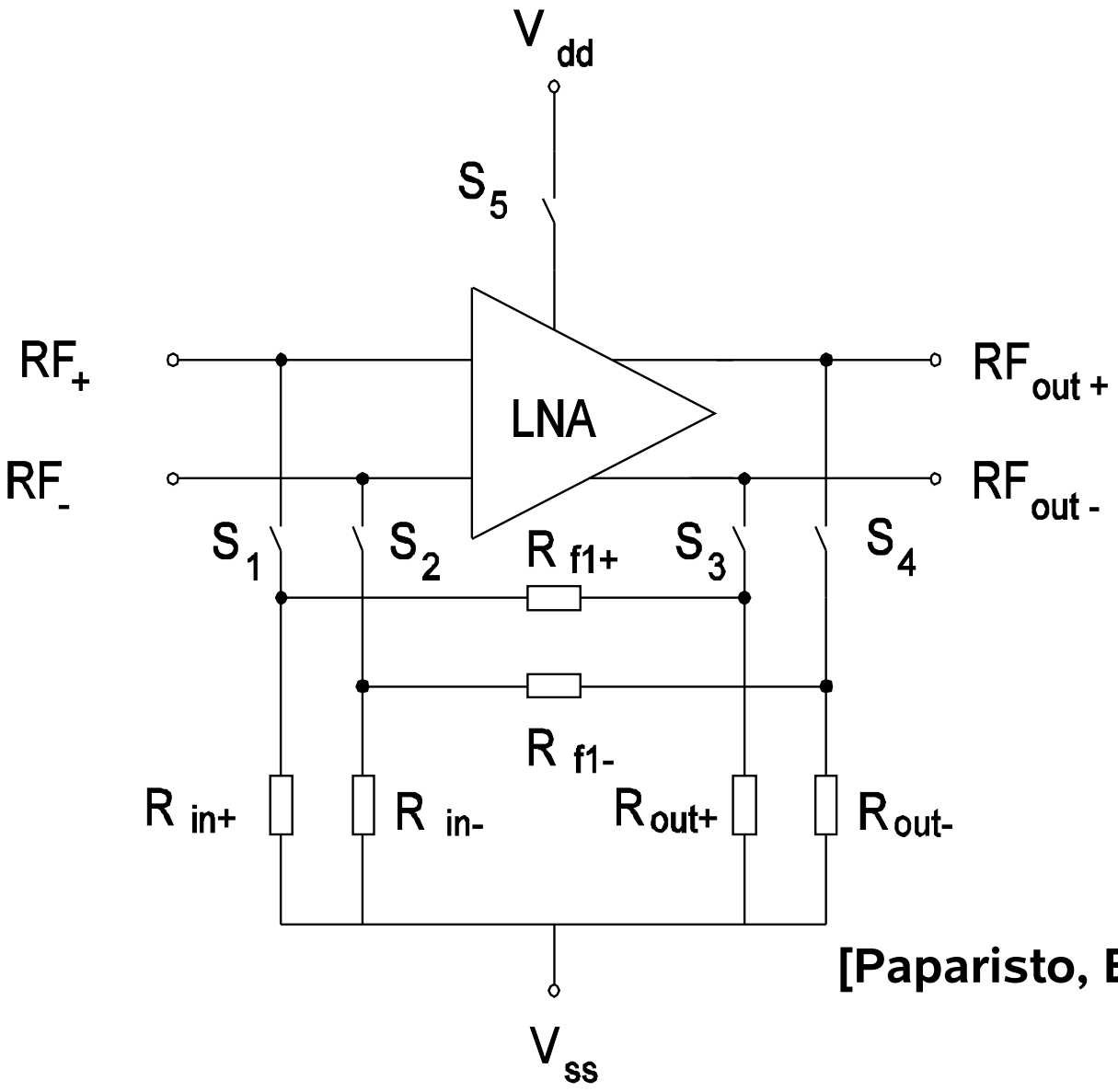
$$\langle i_{n1}, i_{n1}^*\rangle=4KT\Delta f R g_m\frac{f^2}{f_T^2} \qquad \langle i_{n2}, i_{n2}^*\rangle=4KT\Delta f P g_m$$

$$\langle i_{n1}, i_{n2}^*\rangle=4KT\Delta f\, jC\sqrt{PR}\,g_m\frac{f}{f_T}$$

$$[C_Y]=[C_{Ya}]+[C_{Yf}]=4kT\Delta f\begin{bmatrix} Rg_{m1}\frac{f^2}{f_{T1}^2}+\frac{1}{R_F} & \frac{1}{R_F}+jC\sqrt{PR}\,g_{m1}\frac{f}{f_{T1}}\\ \frac{1}{R_F}-jC\sqrt{PR}\,g_{m1}\frac{f}{f_{T1}} & Pg_{m1}+\frac{1}{R_F}\end{bmatrix}$$

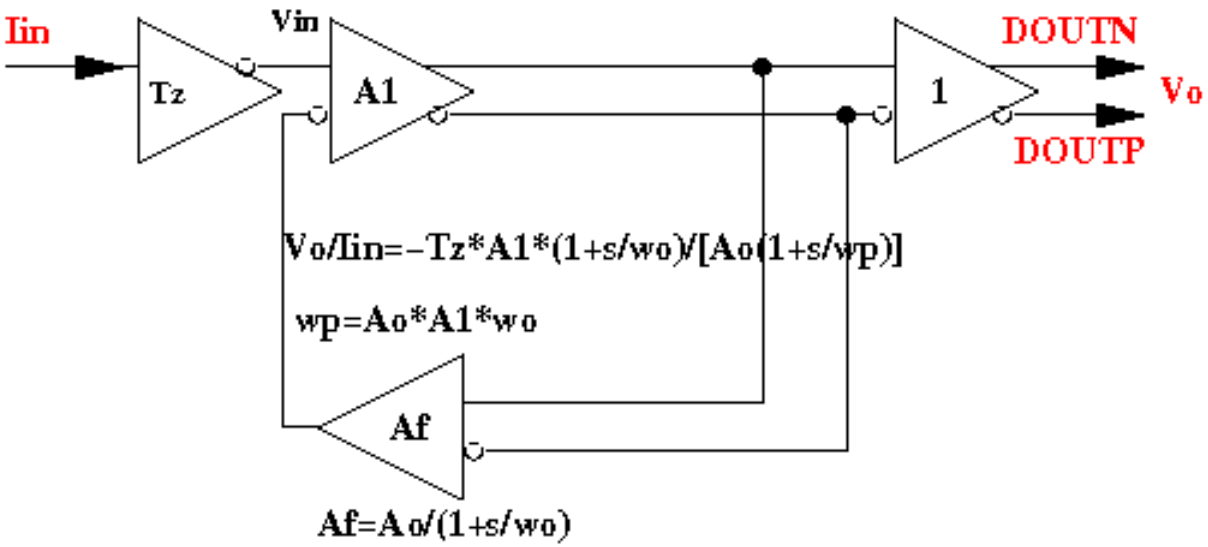
$$[Y]=[Y_a]+[Y_f]\approx\begin{bmatrix} j\omega[C_{gs1}+C_{gd1}(1+g_{m1}R_{D1})]+\frac{1}{R_F} & \frac{1}{R_F}\\ \frac{g_{m1}g_{m2}}{g_{o1}}+\frac{1}{R_F} & \frac{1}{R_F}+g_{o2}+j\omega(C_{gd2}+C_{db2})\end{bmatrix}$$

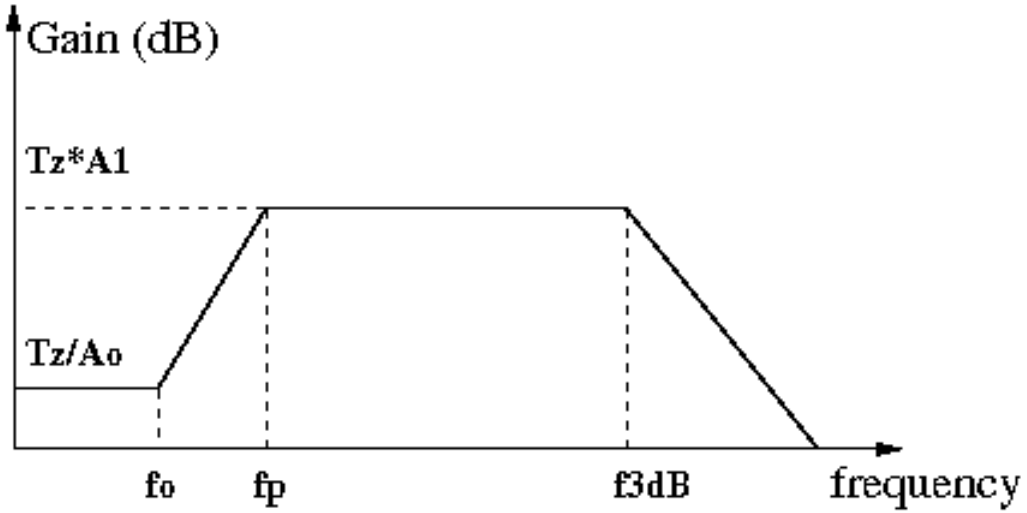
Low-gain mode



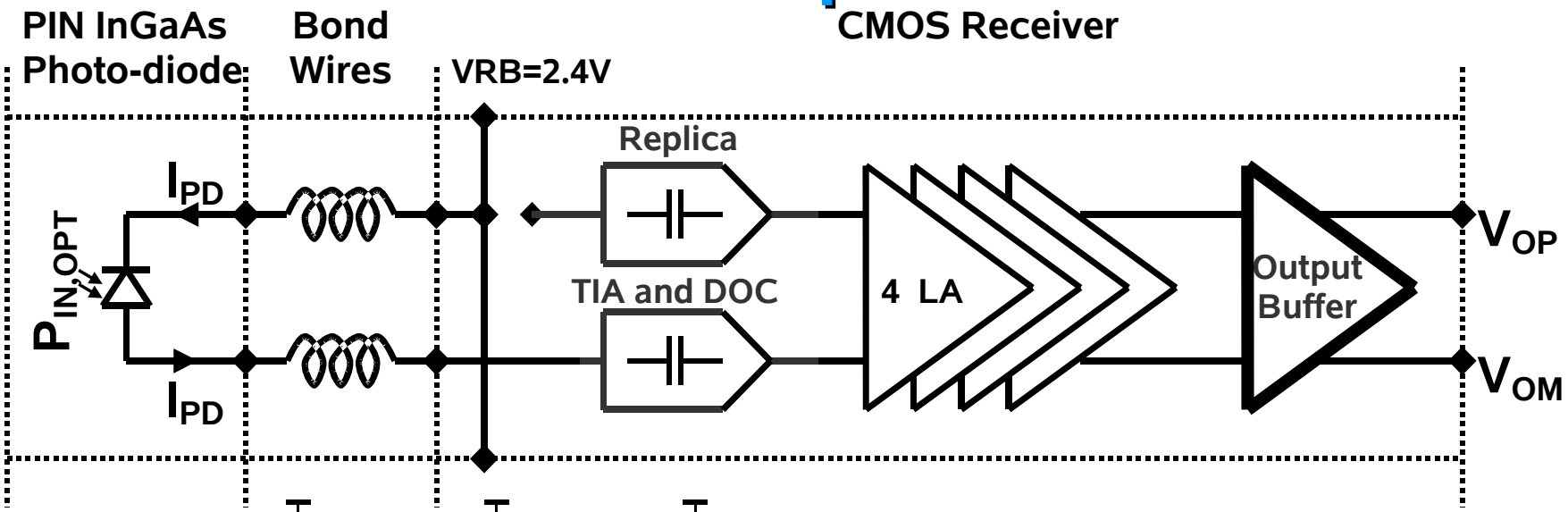
[Paparisto, ESSCIRC, Sep. 2002]

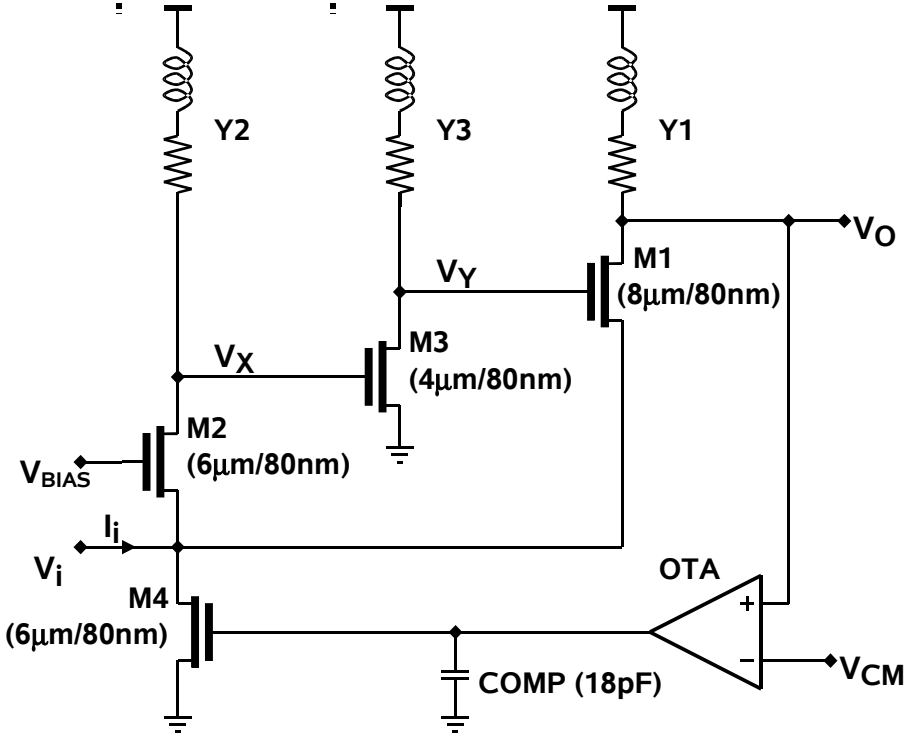
Transimpedance Limiting Amplifier



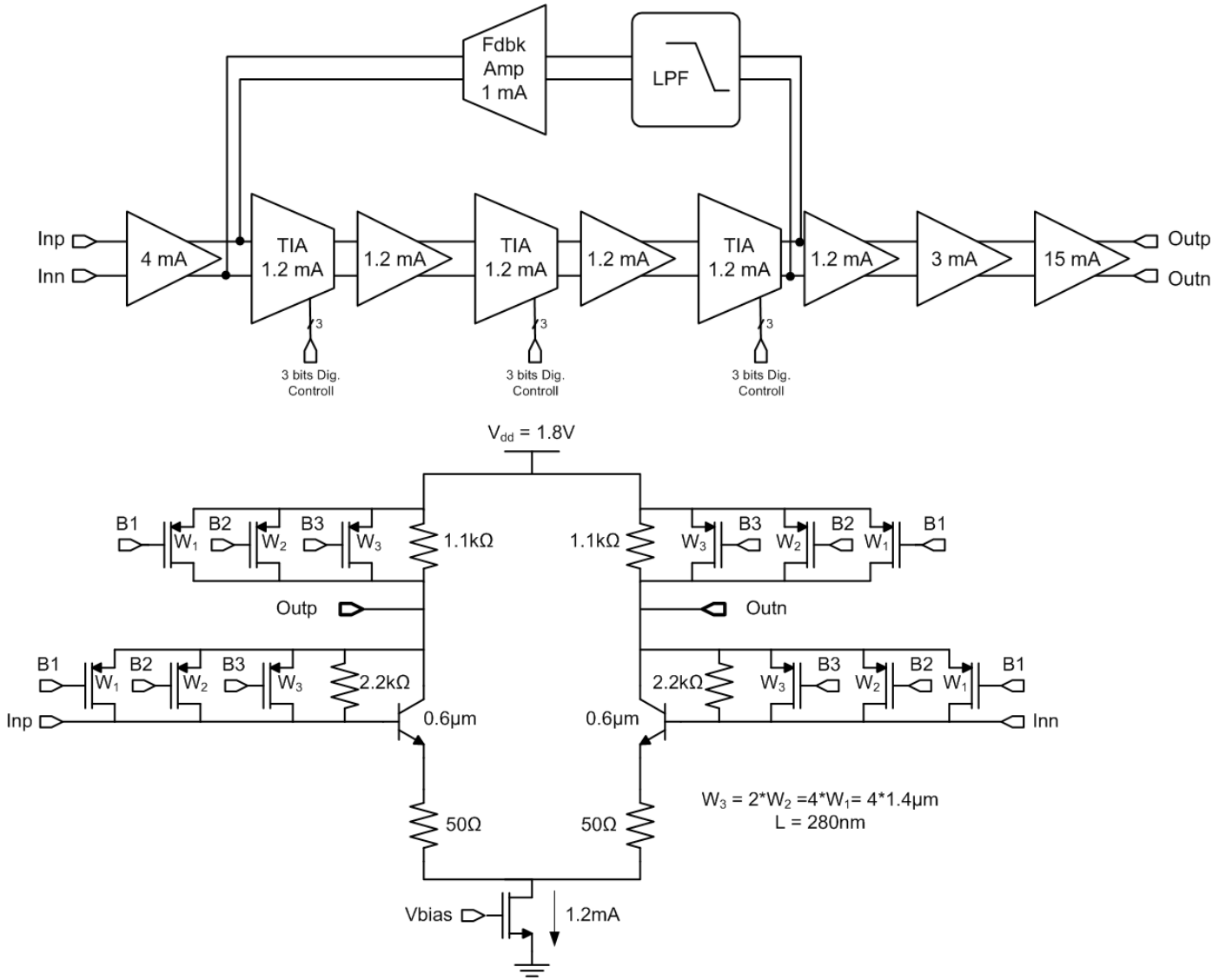


Example


PIN InGaAs
Photo-diode
Bond
Wires
VRB=2.4V
CMOS Receiver
Replica
I_{PD}
$P_{IN,OPT}$
I_{PD}
TIA and DOC
4 LA
Output
Buffer
V_{OP}
V_{OM}


Y2
Y3
Y1
V_O
V_Y
M1
(8µm/80nm)
V_X
M3
(4µm/80nm)
M2
(6µm/80nm)
V_{BIAS}
I_i
V_i
M4
(6µm/80nm)
OTA
+
−
COMP (18pF)
V_{CM}

Variable-Gain TIA



Summary

- TIAs feature the broadest bandwidth with the lowest noise and lowest power dissipation amongst lumped broadband amplifier topologies.
- TIAs offer optimal solution for fiberoptics, backplane and UWB applications
- An optimal transistor size exists for a given photodiode capacitance and/or 3dB bandwidth
- Transistors must be biased at J_{opt}
- Both SiGe HBT and CMOS TIAs are now viable at 10 to 80+ Gb/s