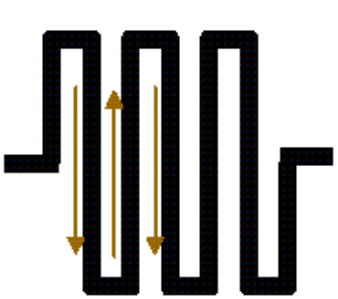
Chapter 4.5. High Frequency Passive Devices

Outline

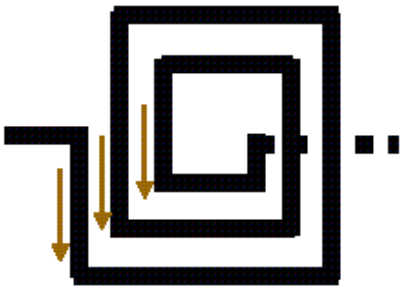
- Inductors
- Transmission lines
- Varactors
- MIM Capacitors
- Resistors

Types of integrated inductors (Yoon, RFIC-2003)

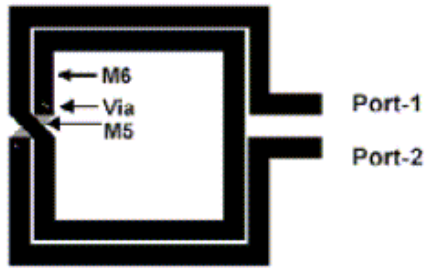


Meander Type

Solenoid Type



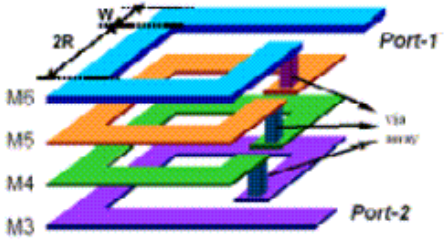
Spiral Type



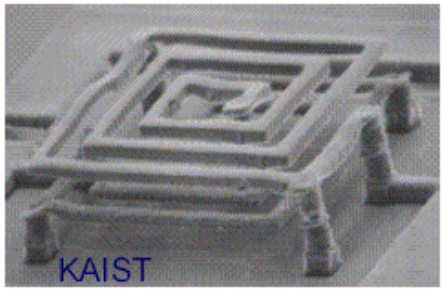
Symmetric Spiral Type

In silicon ICs:

- Spiral
- Multi-layer shunted
- Symmetrical spiral
- Stacked helical



Stacked Helical



Stacked MEMS

Types of inductors: by number of terminals

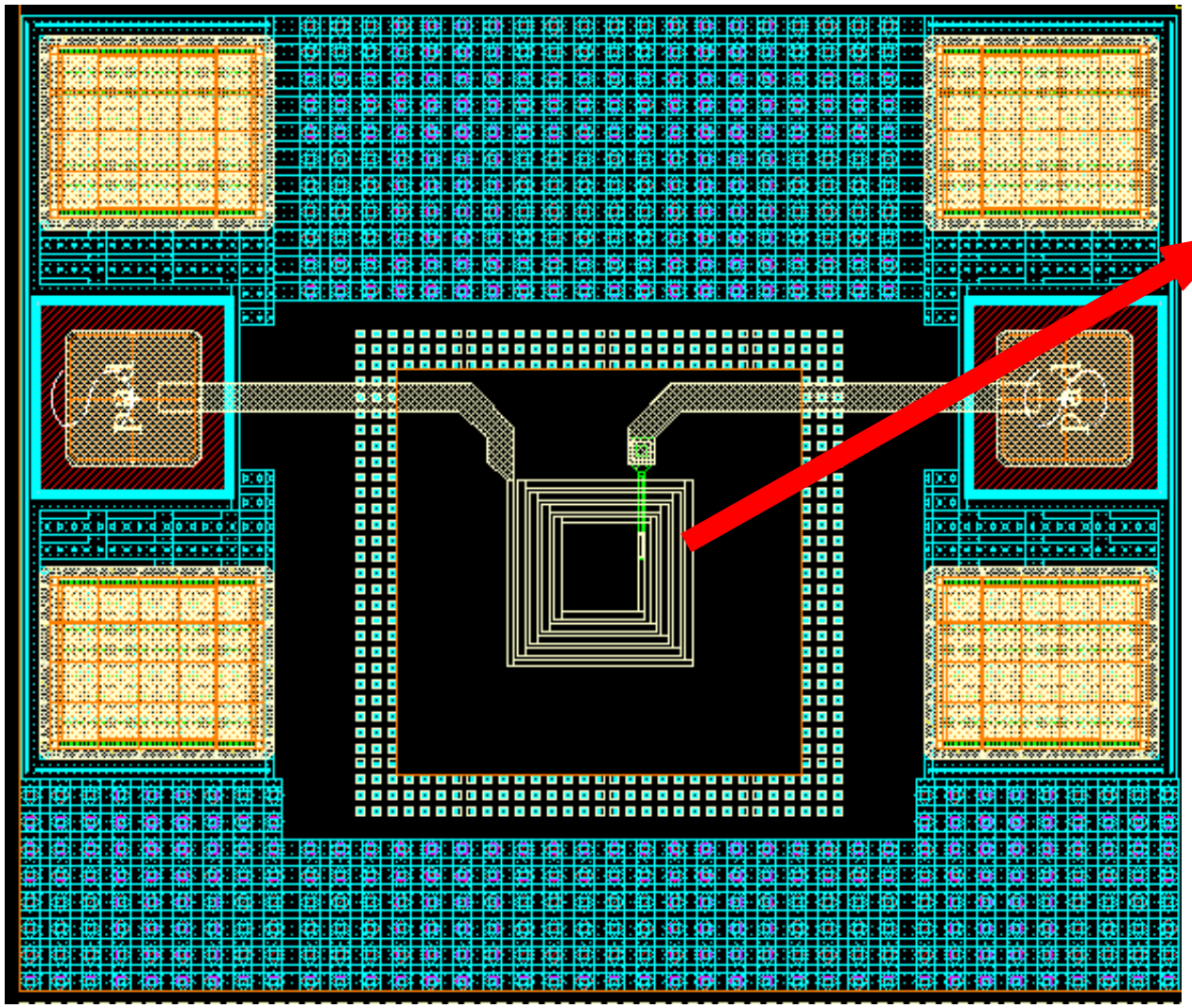
- 2-terminal
- 3-terminal (t-coil)
- transformers
- symmetrical transformers
  - (baluns)

Inductor integration issues

- Low quality factor (Q)
- Large chip area (high cost)
- Limited application frequency range:
  - lower bound limited by size and Q
  - upper bound (SRF=Self-Resonant-Frequency) limited by dielectric thickness
- Cross-talk through silicon substrate

GOAL is to AIM HIGH: high Q and high SRF

2-terminal inductor layout & cross-section



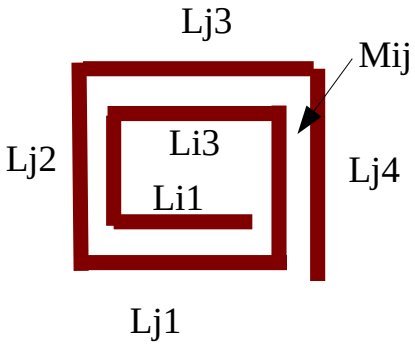
Main FOMs

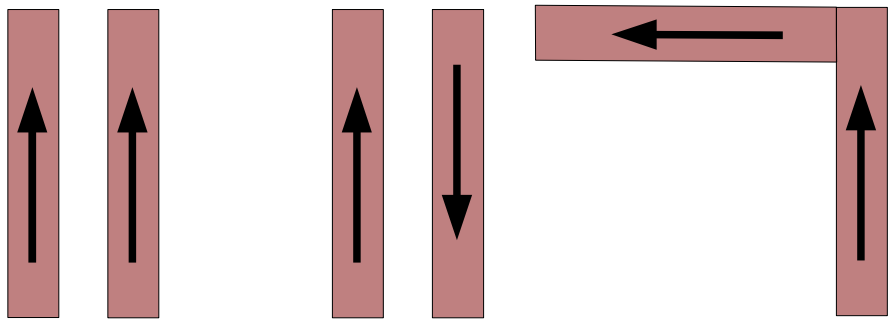
- Inductance L
- Quality factor Q
- SRF
- PQF

Inductance L

- Inductance: induces and stores magnetic field
- Greenhouse Equation $L = \frac{total\ flux}{current}$

$$L = Self\ Inductance\ (\sum_{i=1}^{n} L_i) + Mutual\ Inductance\ (\sum_{i=1}^{n} \sum_{j=2(j\neq i)}^{n} M_{ij})$$





M>0 M<0 M=0

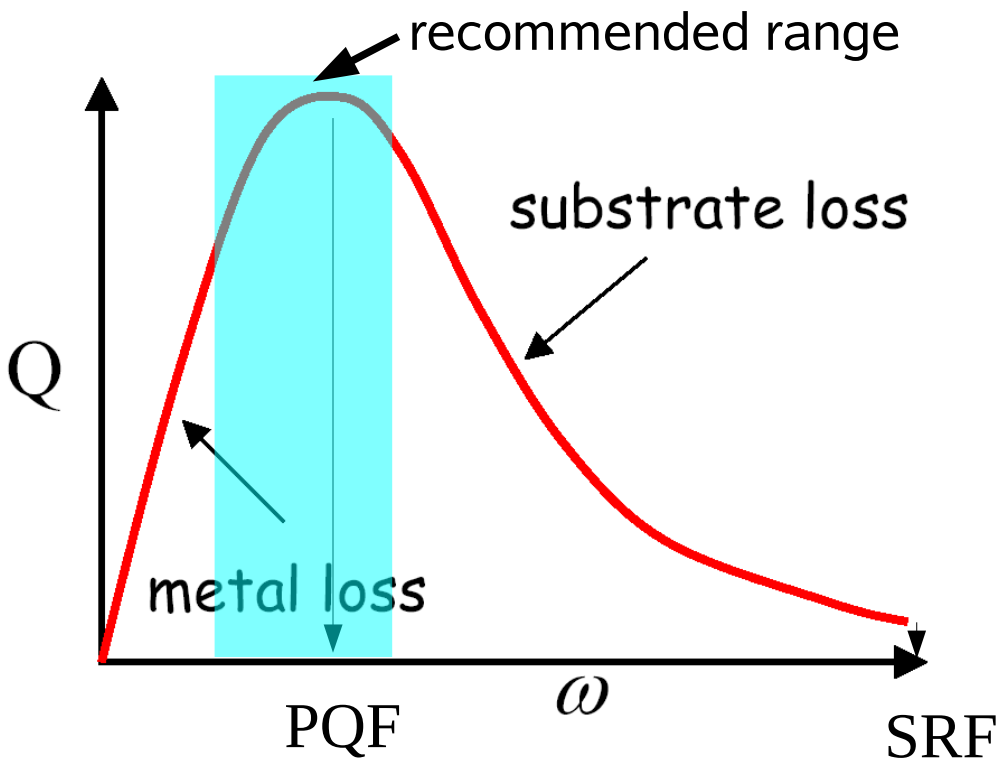
Inductor Q

- Q describes energy efficiency:

$$Q = \frac{\text{stored energy}}{\text{dissipated energy}}$$

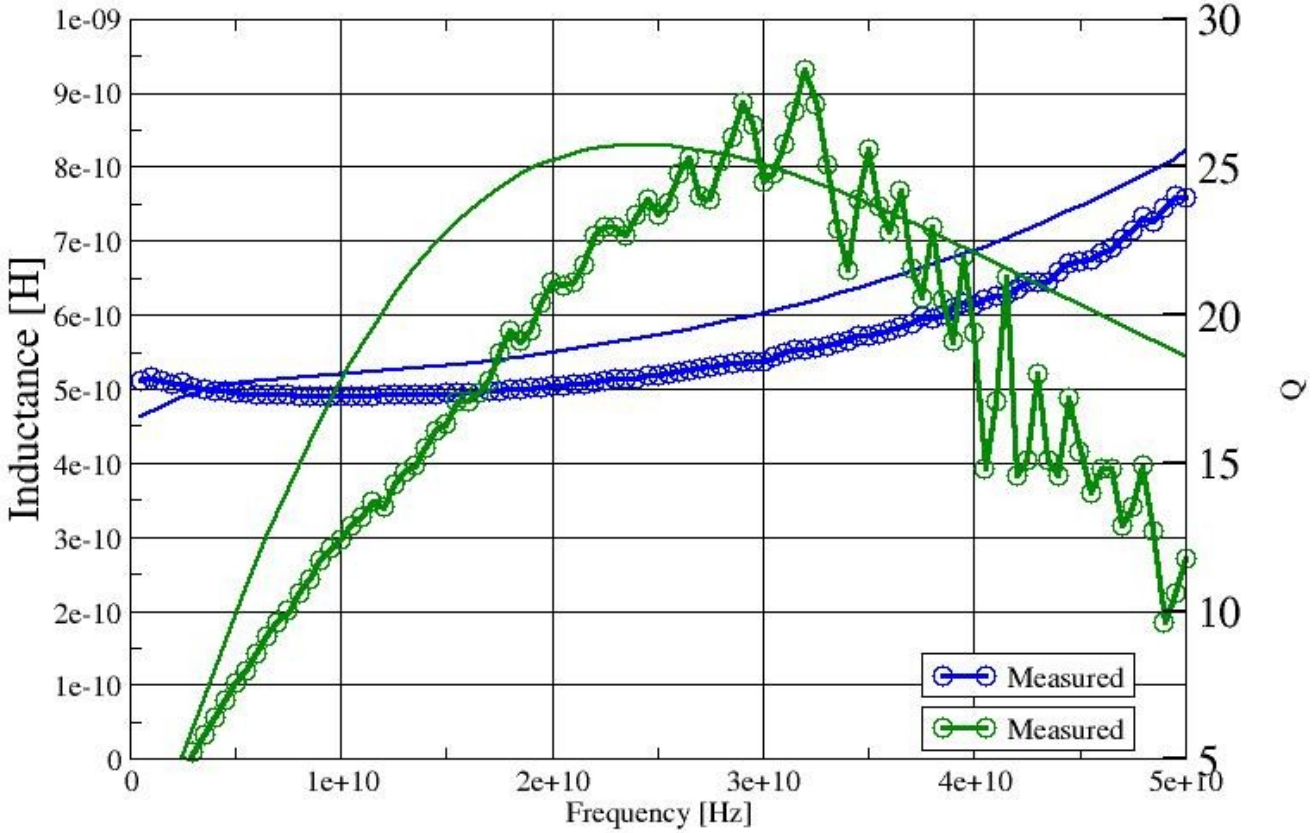
- Conventional definition:

$$Q_{eff} = \frac{\Im(-Y_{11})}{\Re(Y_{11})}$$

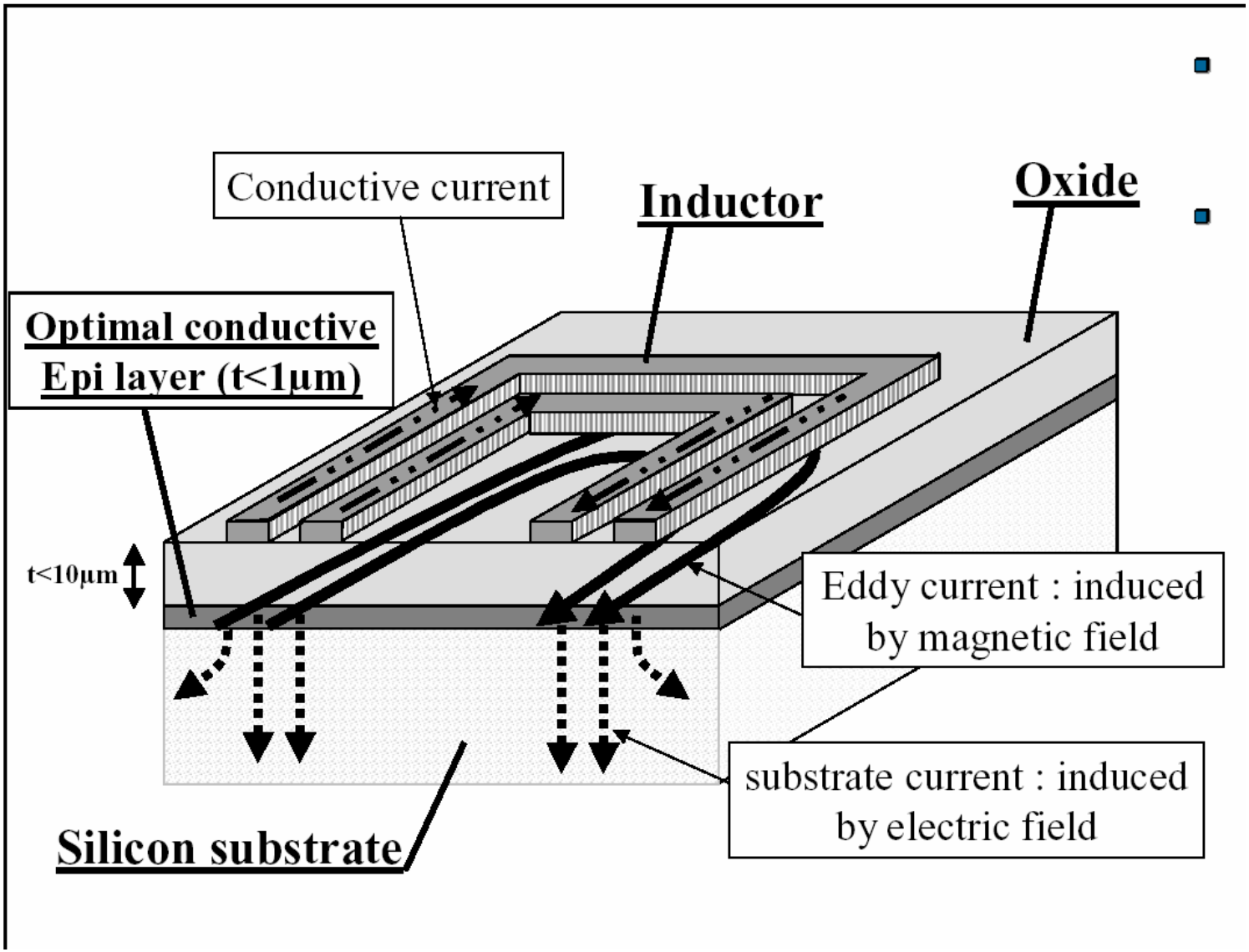


0.13 µm CMOS two-terminal inductor meas.

$$L_{eff} = \frac{\Im[(Y_{11})^{-1}]}{\omega} \qquad Q_{eff} = \frac{\Im[-Y_{11}]}{\Re[Y_{11}]}$$



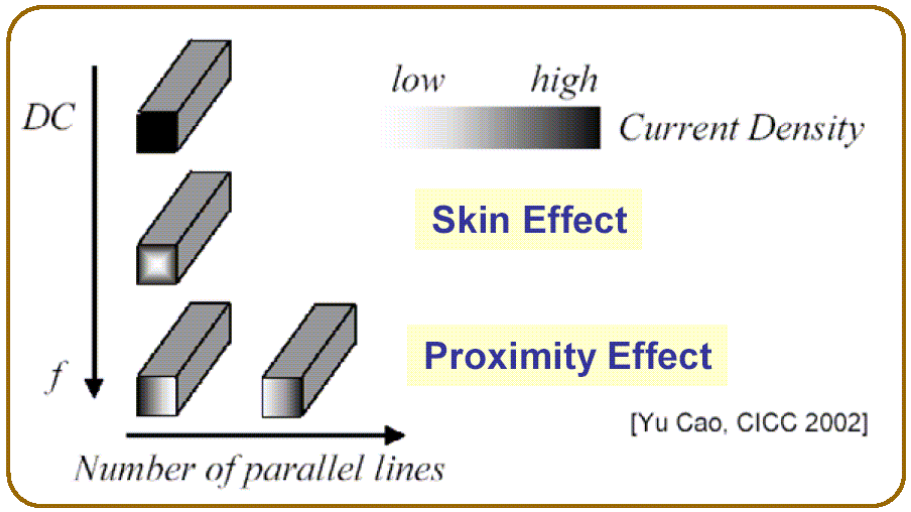
Loss mechanisms in inductors (Dubuc et al, IMS2002)



- loss in metal
- loss in substrate

Metal loss: series resistance Rs

- DC-loss due to thin metal and planar geometry
- Frequency-dependent cross-section due to skin effect (B induced by conductor itself)
- Non-uniform current density due to proximity effect (*B* induced by neighbours)



$J = J_p + J_e$ where

$\nabla \times J_p = 0;\ \ \nabla \times J_e = j\omega\sigma B;\ \ \nabla J_e = 0$

J_p = potential current

J_e = eddy current

Metal loss: techniques to reduce it

- Multiple metal layers shunted (reduces PQF and SRF)
- Thicker metal (needs process change)
- More conductive metal i.e. Cu instead of AlCu (needs process change)
- Use narrower inner turns to reduce eddy current loss and wider outer turns to reduce DC resistance (increases PQF and SRF)

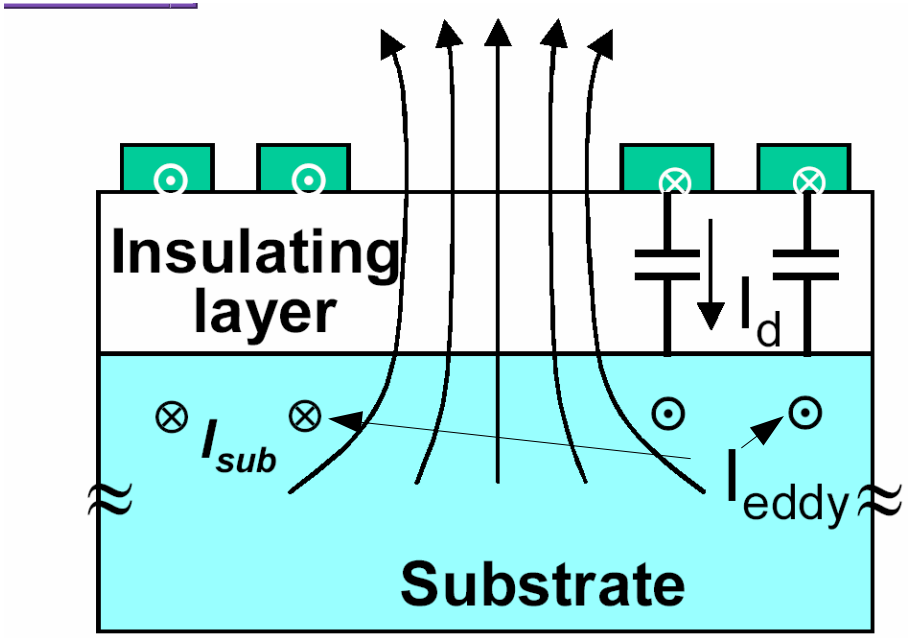
Substrate loss

- I_p = potential current in substrate, induced by electric field

$$J_p^{sub} = \sigma_{sub} E = -\sigma_{sub} \nabla \phi$$

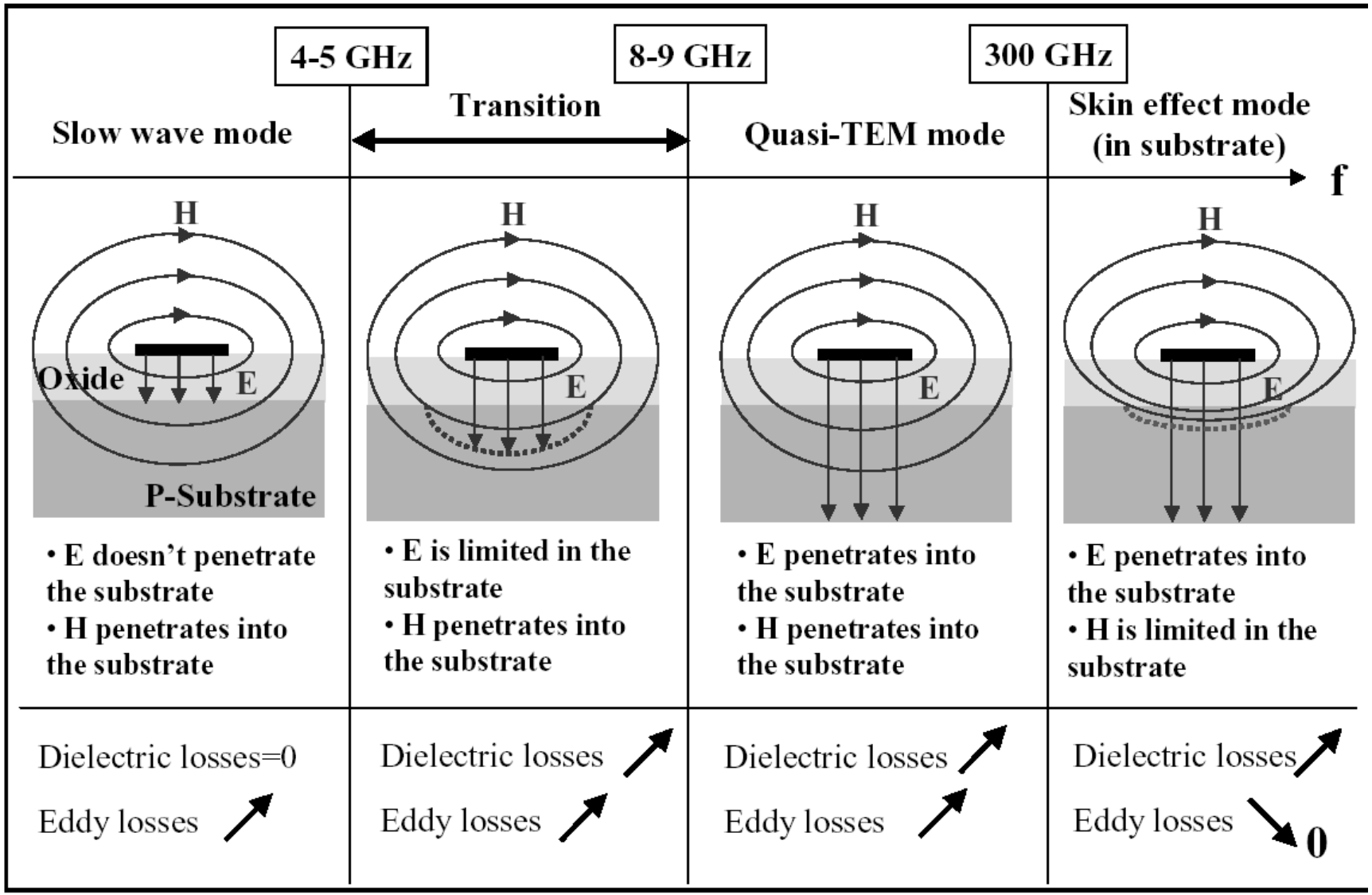
where $\nabla^2 \phi = 0$

- I_{eddy} = eddy current in substrate, induced by magnetic field causes inductance and resistance loss



$$\nabla \times J_{eddy}^{sub} = j\omega \sigma_{sub} B$$

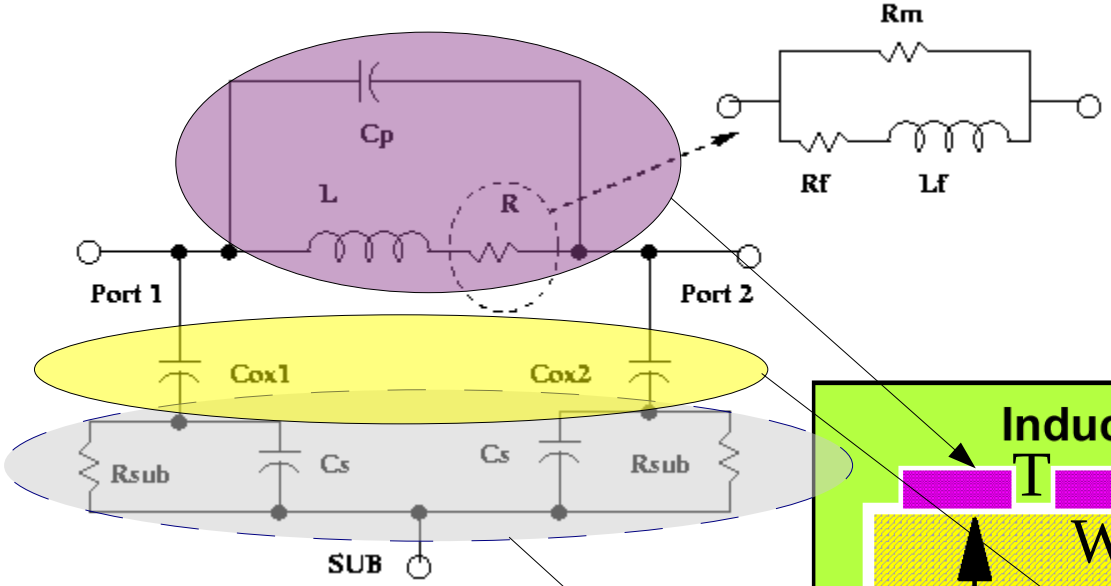
Propagation modes (Dubuc et al, IMS2002)



Substrate loss: techniques to reduce it

- Minimize electric coupling to substrate (I_d) (also increases SRF and PQF):
  - small inductor area
  - increase dielectric thickness (process change ?)
  - low-k dielectric (process change)
- Reduce eddy currents in substrate
  - pattern shield (reduces PQF, SRF)
- Reduce both eddy and potential currents in sub.
  - increase substrate ρ (σ =>0) (process change)
  - Place sub contacts 30 μm .. 50 μm from inductor

HF inductor equivalent circuits: simple π



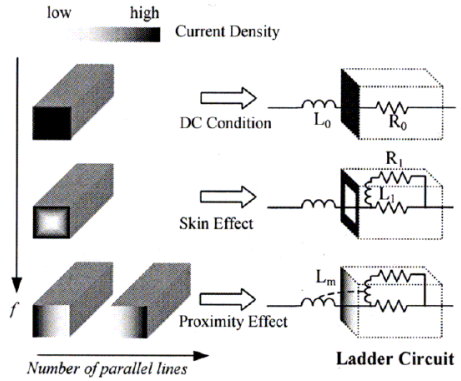
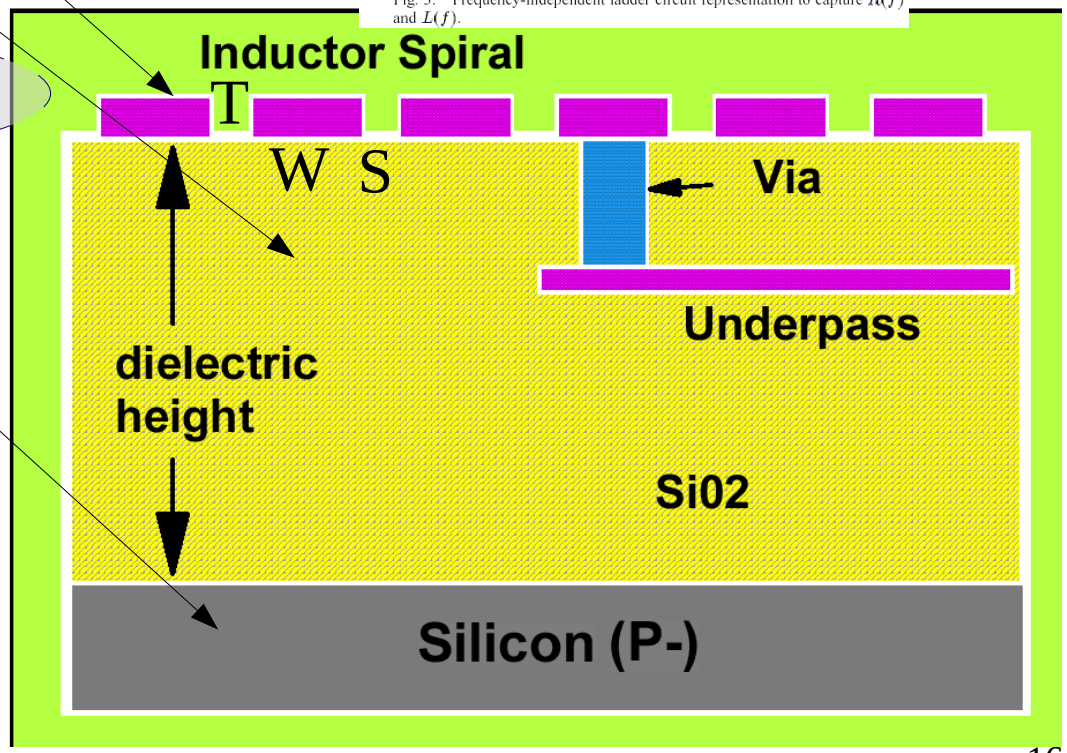


Fig. 3. Frequency-independent ladder circuit representation to capture $R(f)$ and $L(f)$.



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Equivalent circuit model equations: simple π

- Cao Y. et al., JSSC March 2003
- L (see t-line-over-substrate equations) $L \approx \frac{6\mu_0 n^2 d_{avg}^2}{11d - 7d_{avg}}$
  - n = number of turns
  - d = outer diameter of inductor
  - d_{avg} = arithmetic mean of inner and outer diameter
  - $\mu_0 = 4\pi\ 10^{-13}$ H/μm is the permeability of vacuum
- R_s has DC and AC (frequency dependent) terms $R_{DC} = \frac{\rho l}{W t}$
  - s is the conductivity of the metal

$$\delta = \sqrt{\frac{1}{\pi f \mu \sigma}}$$

$$R_{AC} = \frac{\rho l}{W \delta \left(1 - \exp\left(\frac{-t}{\delta}\right)\right)}$$

Equivalent circuit model equations (ii): simple π

- C_{oxi} (oxide capacitance) $C_{ox} = \frac{1}{2} l W \frac{\epsilon_{ox}}{h}$

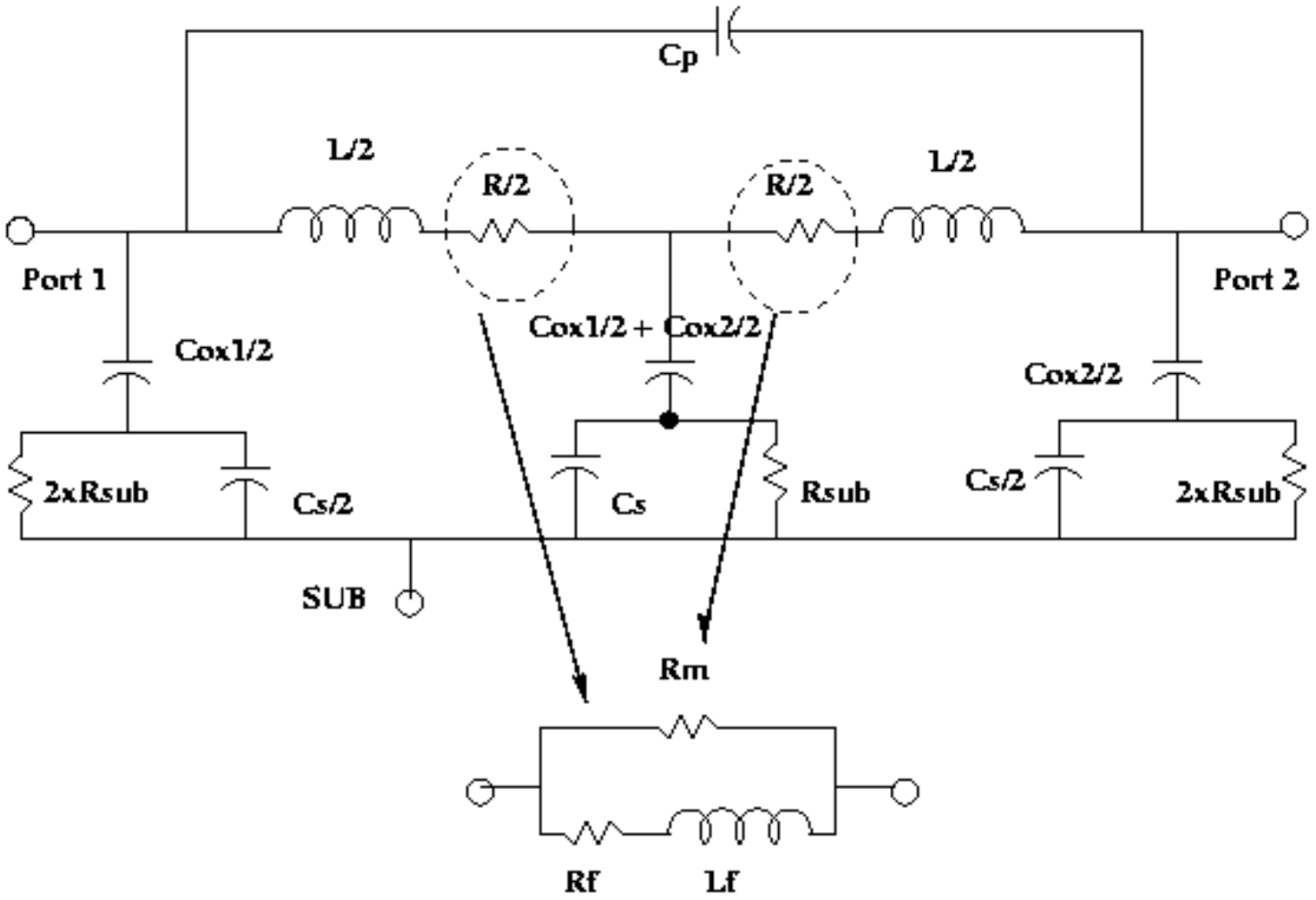
- C_p (overlap capacitance) $C_p = n W^2 \frac{\epsilon_{ox}}{h_{M9-M8}}$

- $C_{si,}$ R_{subi}: substrate network, describe losses in the silicon substrate, similar to the C_{sub}-R_{sub} network of the MOSFET and SiGe HBT.

$$R_{subi} C_{si} = \epsilon_r \epsilon_0 \times R_{su}$$

where R_{su} in Ω is the substrate resistivity, i=1..2

HF inductor equivalent circuit: 2-π



Parameter extraction (2-terminal π circuit)

- At low frequency (0.5 GHz to 1 GHz) extract directly:

$$L = \frac{\Im[-Y_{12}^{-1}]}{\omega} \qquad R = \Re[-Y_{12}^{-1}]$$

$$R_{sub1} = \Re[(Y_{11} + Y_{12})^{-1}] \qquad R_{sub2} = \Re[(Y_{22} + Y_{12})^{-1}]$$

$$C_{OX1} = \frac{[-\Im[(Y_{11} + Y_{12})^{-1}]]^{-1}}{\omega} \qquad C_{OX2} = \frac{[-\Im[(Y_{22} + Y_{12})^{-1}]]^{-1}}{\omega}$$

$$C_{si} = \frac{\epsilon_r \epsilon_0 \times R_{su}}{R_{subi}}$$

Parameter extraction (2-terminal π circuit)

- At high frequency (5 GHz to beyond SRF) :
  - calculate (and/or optimize):
    - C_P from imag(Y_{12}),
    - skin effect parameters L_f, R_f from real(Y_{12}),
    - C_{subi} from imag (Y_{ii}+Y_{12})

Scaling of inductors to mm-wave frequencies

- Scale size and frequency: f->f×S, W->W/S, l->l/S, d->d/S, h->h/S, t=ct.

$$L \approx \frac{6\mu_0 n^2 d_{avg}^2}{11d - 7d_{avg}} \longrightarrow \frac{L}{S} \approx \frac{6\mu_0 n^2 \left[\frac{d_{avg}}{S}\right]^2}{11\frac{d}{S} - 7\frac{d_{avg}}{S}}$$

- Small footprint to minimize loss in silicon

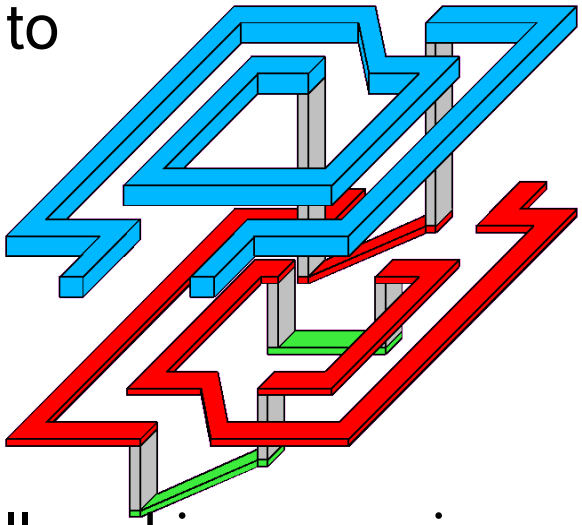
$$C_{ox} = \frac{1}{2} l W \frac{\epsilon_{ox}}{h} \longrightarrow \frac{C_{ox}}{S} = \frac{1}{2}\frac{l}{S}\frac{W}{S}\frac{\epsilon_{ox}}{\frac{h}{S}}$$

$$C_p = n W^2 \frac{\epsilon_{ox}}{h_{M9-M8}} \longrightarrow \frac{C_p}{S} = n\left(\frac{W}{S}\right)^2 \frac{\epsilon_{ox}}{\frac{h_{M9-M8}}{S}}$$

$$SRF \approx \frac{1}{2\pi\sqrt{L(C_{OX} + C_p)}} \longrightarrow S \times SRF = \frac{1}{2\pi\sqrt{\frac{L}{S}\left(\frac{C_{OX}}{S} + \frac{C_p}{S}\right)}}$$

Scaling of inductors to mm-wave frequencies

- Vertical stacking and magnetic coupling to
  - Increase inductance/area
  - reduce loss in substrate



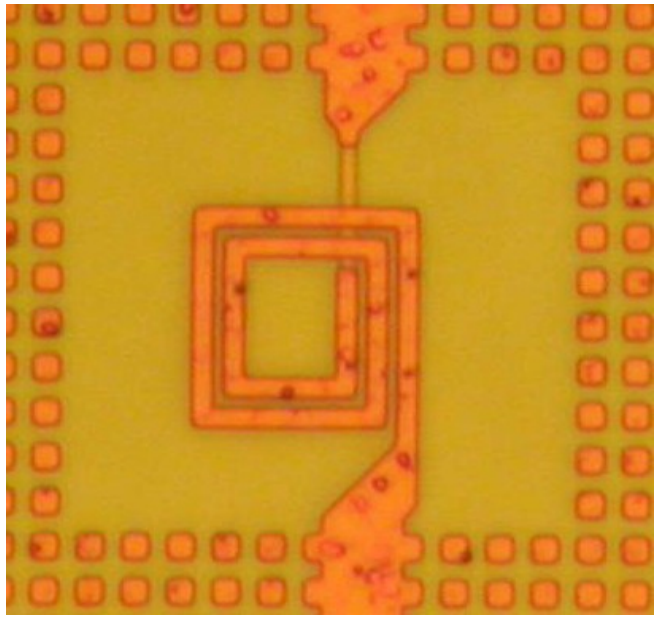
Outcome

- Inductors/transformers can be as small and inexpensive as transistors
- As in MOSFETs, series resistance does not scale
- Q remains the same, but at $f \times S$

$$R_{DC} = \frac{\rho l}{W t} \rightarrow R_{DC} = \frac{\rho \frac{l}{S}}{\frac{W}{S} t}$$

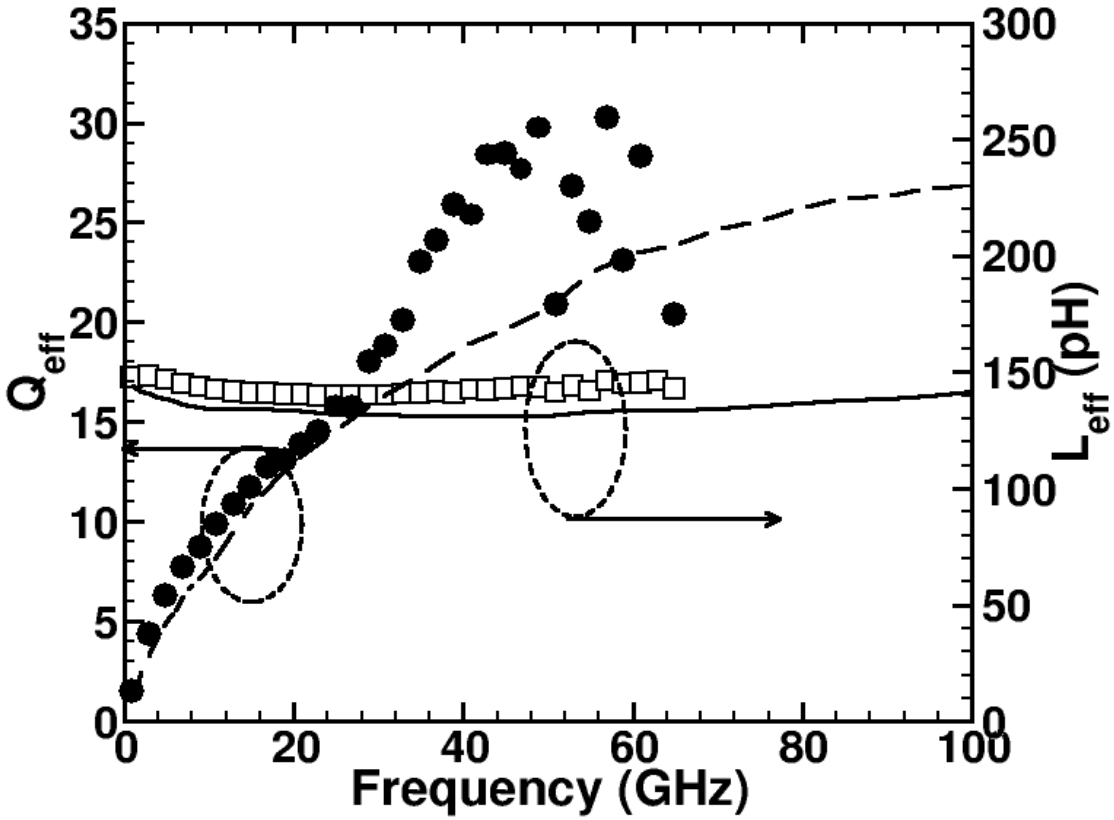
$$R_{AC} = \frac{\rho \frac{l}{S}}{\frac{W}{S} \delta \left(1 - \exp\left(\frac{-t}{\delta}\right)\right)}$$

140 pH Planar Spiral Inductor in 90-nm CMOS



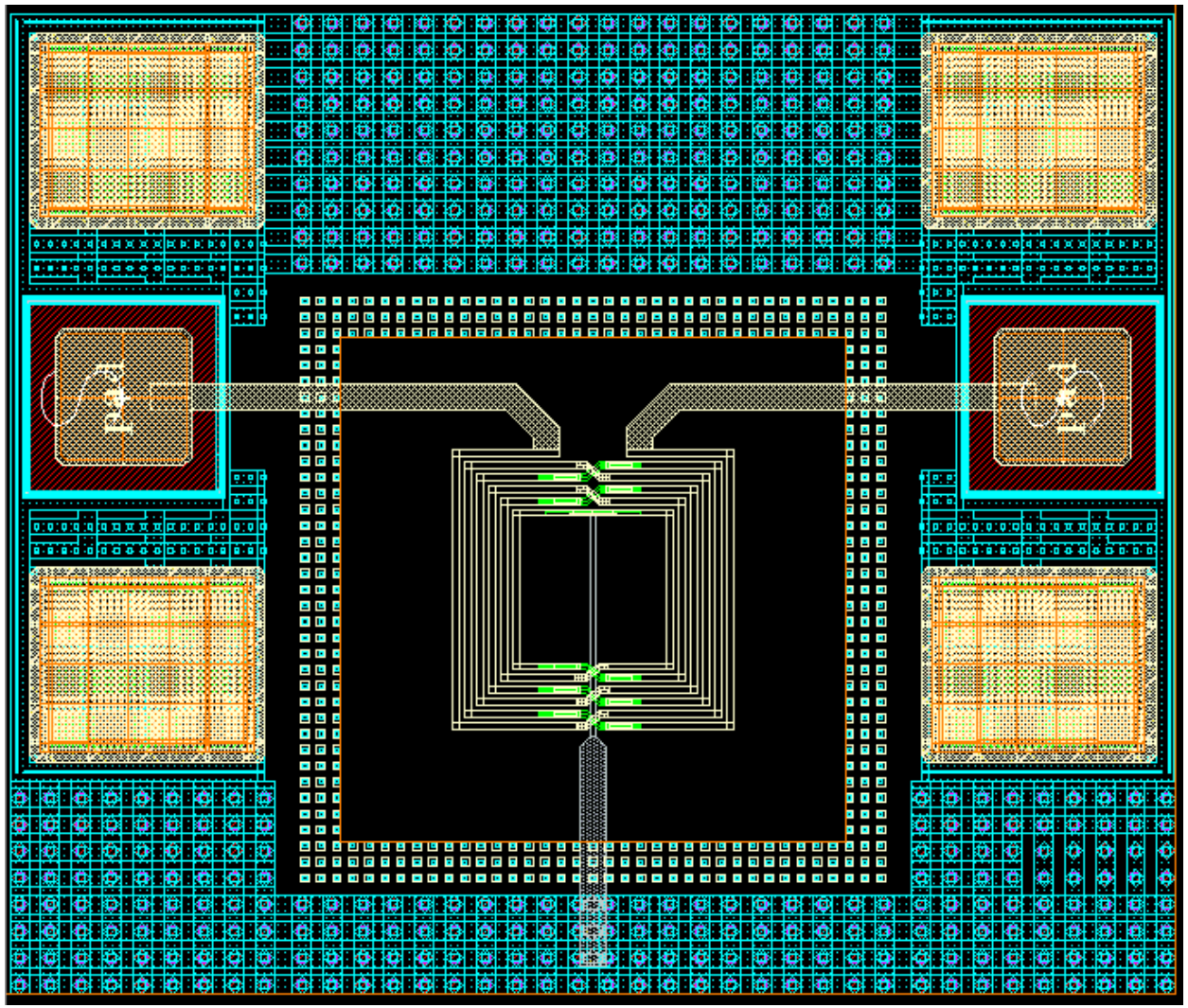
d = 29 μm, n = 2.25
S = 2 μm, W = 2 μm

t = 3 μm

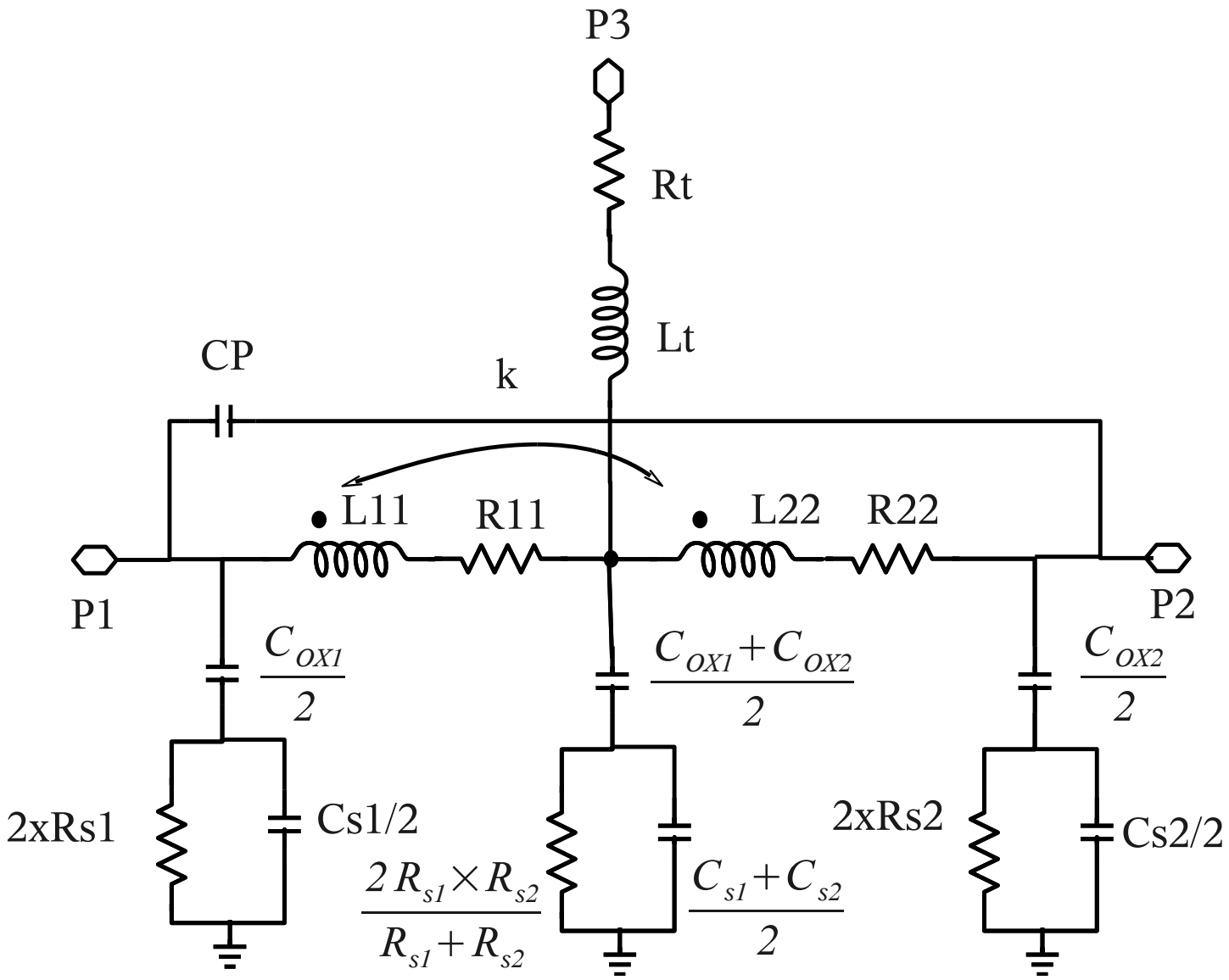


Measured vs. ASITIC simulated L_{eff} and Q_{eff}

3-terminal inductor layout



3-terminal inductor equivalent circuit



Model parameter extraction

$$L_{11}=\frac{\Im[Z_{11}]}{\omega} \qquad L_{22}=\frac{\Im[Z_{22}]}{\omega} \qquad R_{11}=\Re[Z_{11}] \qquad R_{22}=\Re[Z_{22}]$$

$$M=\frac{-\Im[Z_{12}]}{\omega}=\frac{-\Im[Z_{21}]}{\omega} \qquad R_t=\Re[Z_{12}]=\Re[Z_{21}]$$

$$L_{diff}=\frac{\Im[Z_{11}+Z_{22}-Z_{12}-Z_{21}]}{\omega} \qquad Q_{diff}=\frac{\Im[Z_{11}+Z_{22}-Z_{12}-Z_{21}]}{\Re[Z_{11}+Z_{22}-Z_{12}-Z_{21}]}$$

$$k=\frac{M}{\sqrt{L_{11}\times L_{22}}}$$

C_{oxi}, R_{subi}, C_{si} are extracted from the 2-terminal equivalent.

Single-ended vs. diff.-mode inductance

$$L_{diff} = L_{11} + L_{22} + 2M = 2.2\,nH$$

$$L_{single} = L_{11} = L_{22} = 0.67nH$$

- Strong mismatch can occur in either differential mode or single-ended/common-mode if tight coupling in 3-term inductors exists.
- Use 3-terminal inductors only inside the chip, not in output buffer.
- Watch out for sign of M! L_{diff} should be larger than $2L_{11}$.

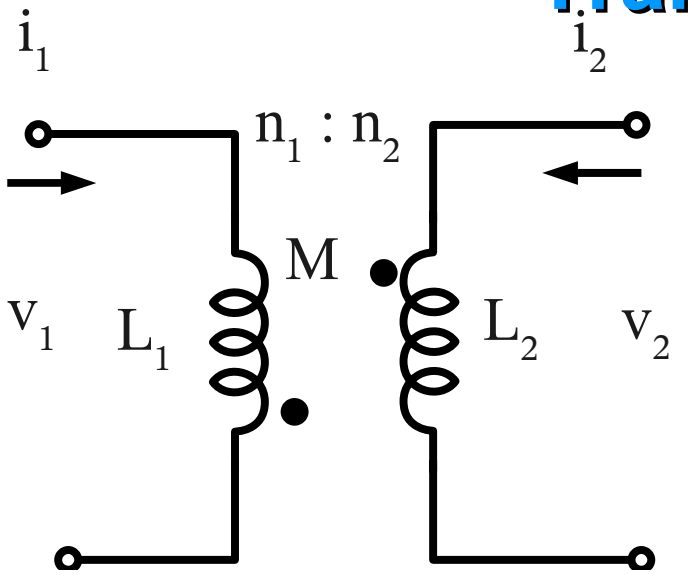
HF inductor layout design

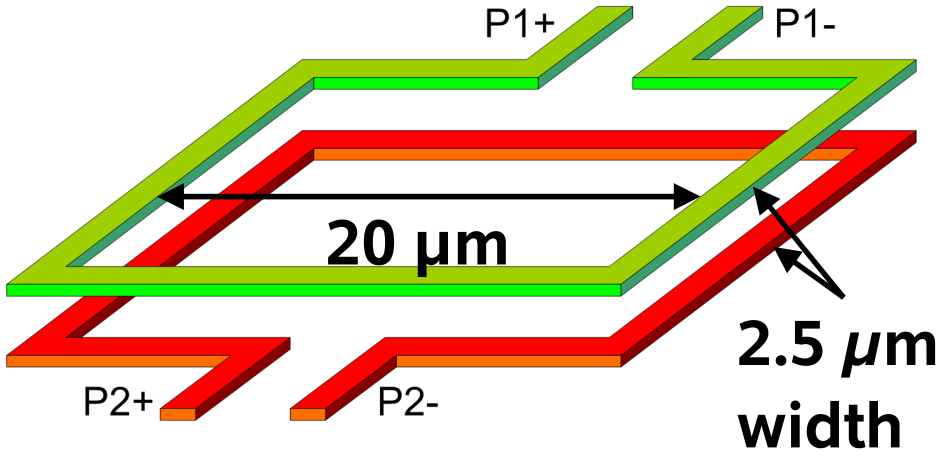
- High SRF: narrow metal, wide spacing, minimum diameter
- High Q : wide, thick metal, shunted metal layers
- Large L/ area and SRF: large diameter, narrow metal, stacked, series-connected metal layers
- Substrate p-taps in 25-50 μm proximity
- Minimize size in differential ckts.: use one center-tapped differential inductor, rather than two inductors (but lower overall SRF)

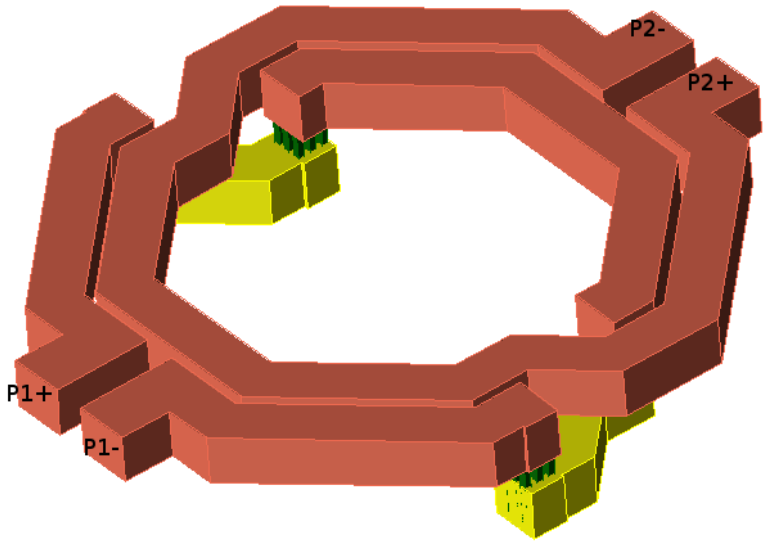
High Q & high SRF inductor design tips

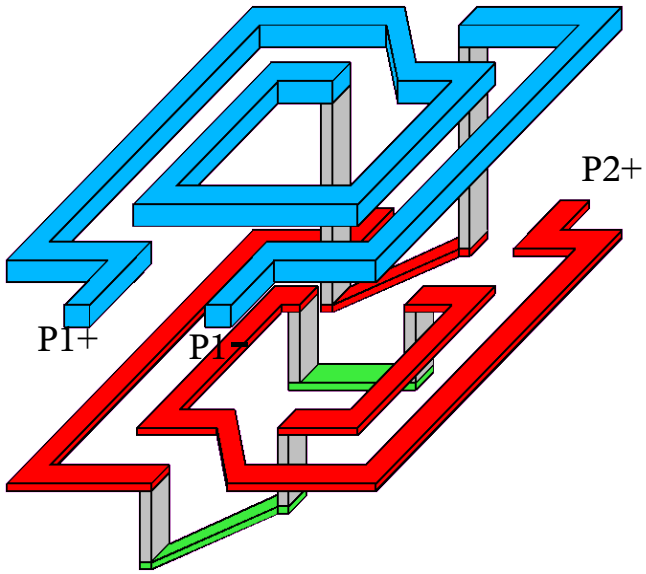
- Small diameter
- Narrow (narrower in inner turns), (W)
- thick, (T)
- widely spaced (S)
- top metal -only (stacked structure for peaking inductors)
- windings on
- thick dielectric (h)
- with low permittivity (ε_{ox})

Transformers



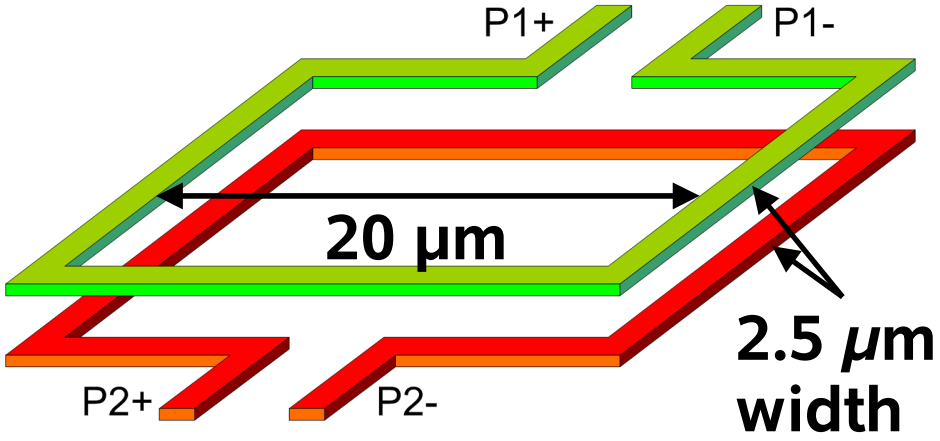


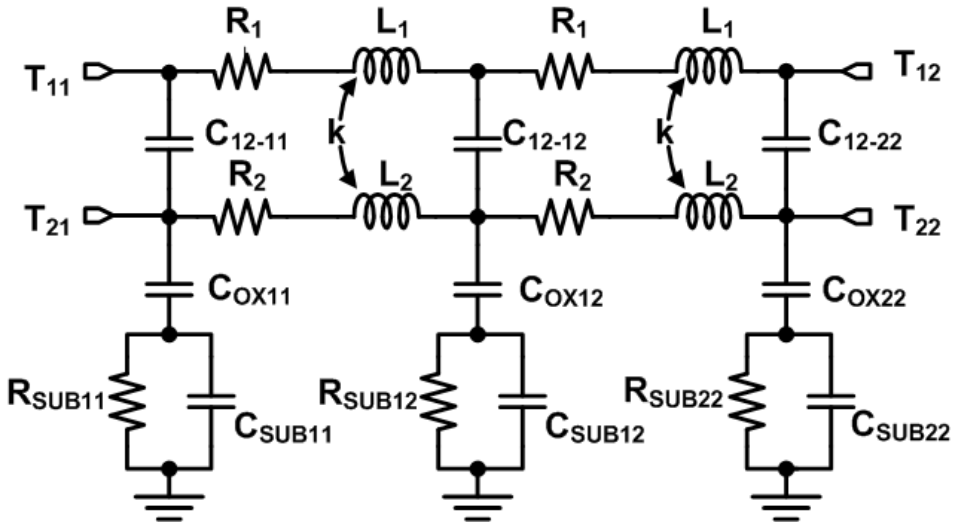




3-D stacked transformer modelling

- ASITIC modeling procedure
  1. Use “pix” on bottom coil alone to find C_{OX}, C_{SUB}, R_{SUB}, R_2, L_2
  2. Calculate C_{SUB}
  3. Use “pix” on top coil alone to find R_1 and L_1
  4. Use “pix” on top coil with bottom coil grounded to get C_{12}
  5. Use “k” command on both coils together to find coupling.

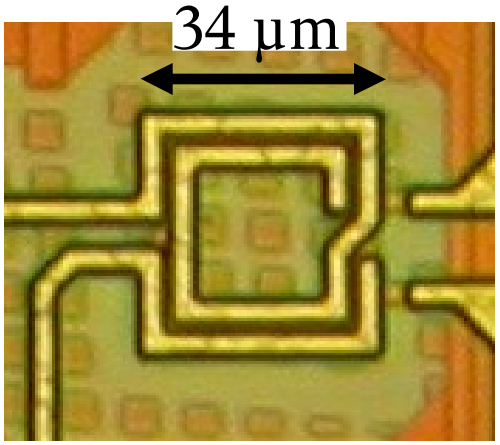




Transformers in SiGe BiCMOS and 90nm CMOS

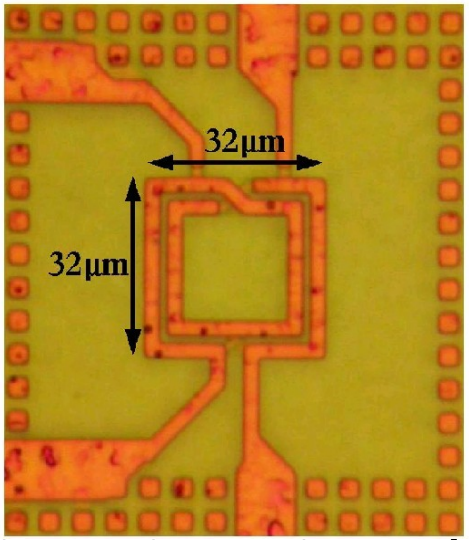
1:1 vertically stacked SiGe BiCMOS transformer

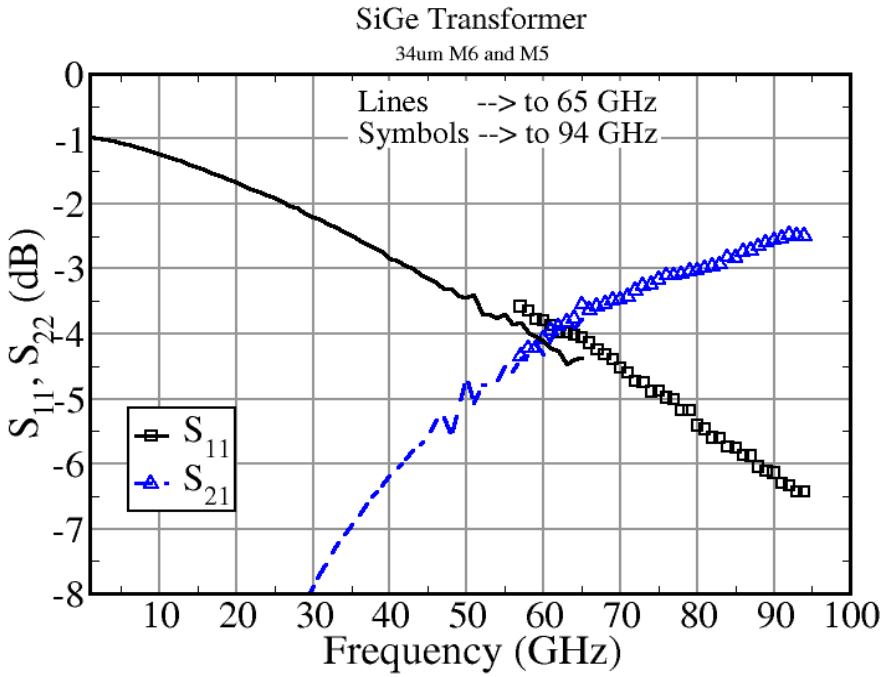
n=2, t=3µm

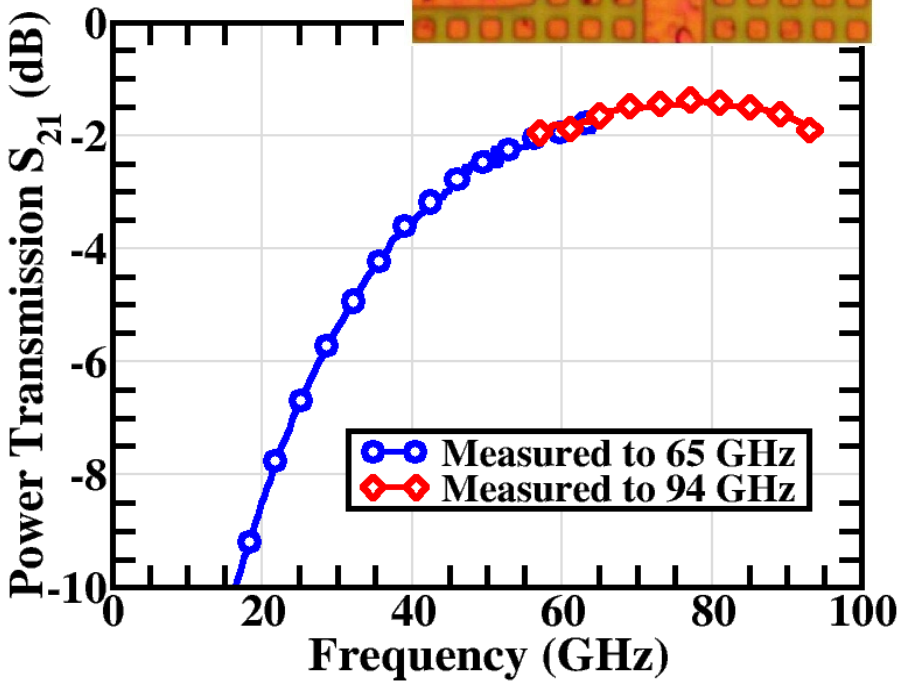


1:1 vertically stacked transformer in 90-nm CMOS

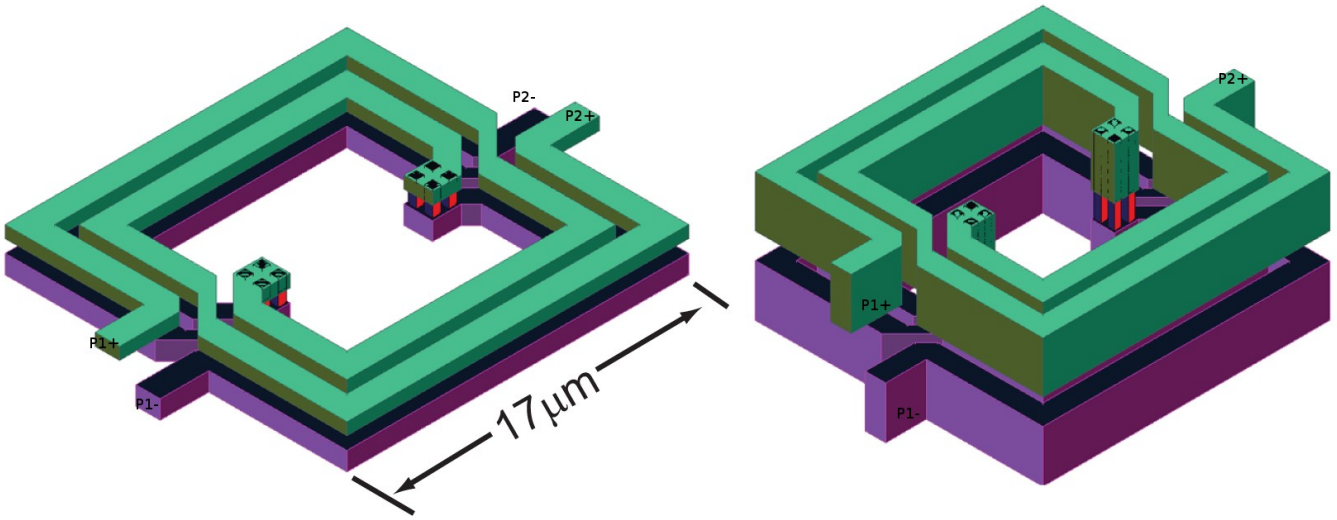
n=2, W= 2µm, S=2µm, t=3µm

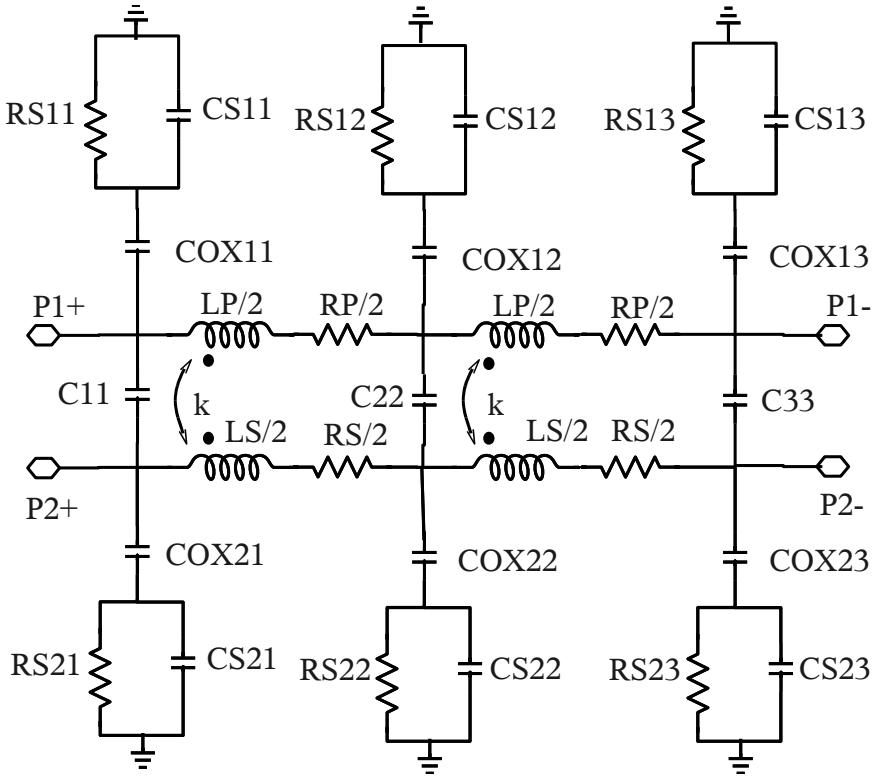






Baluns (symmetrical transformers)





Outline

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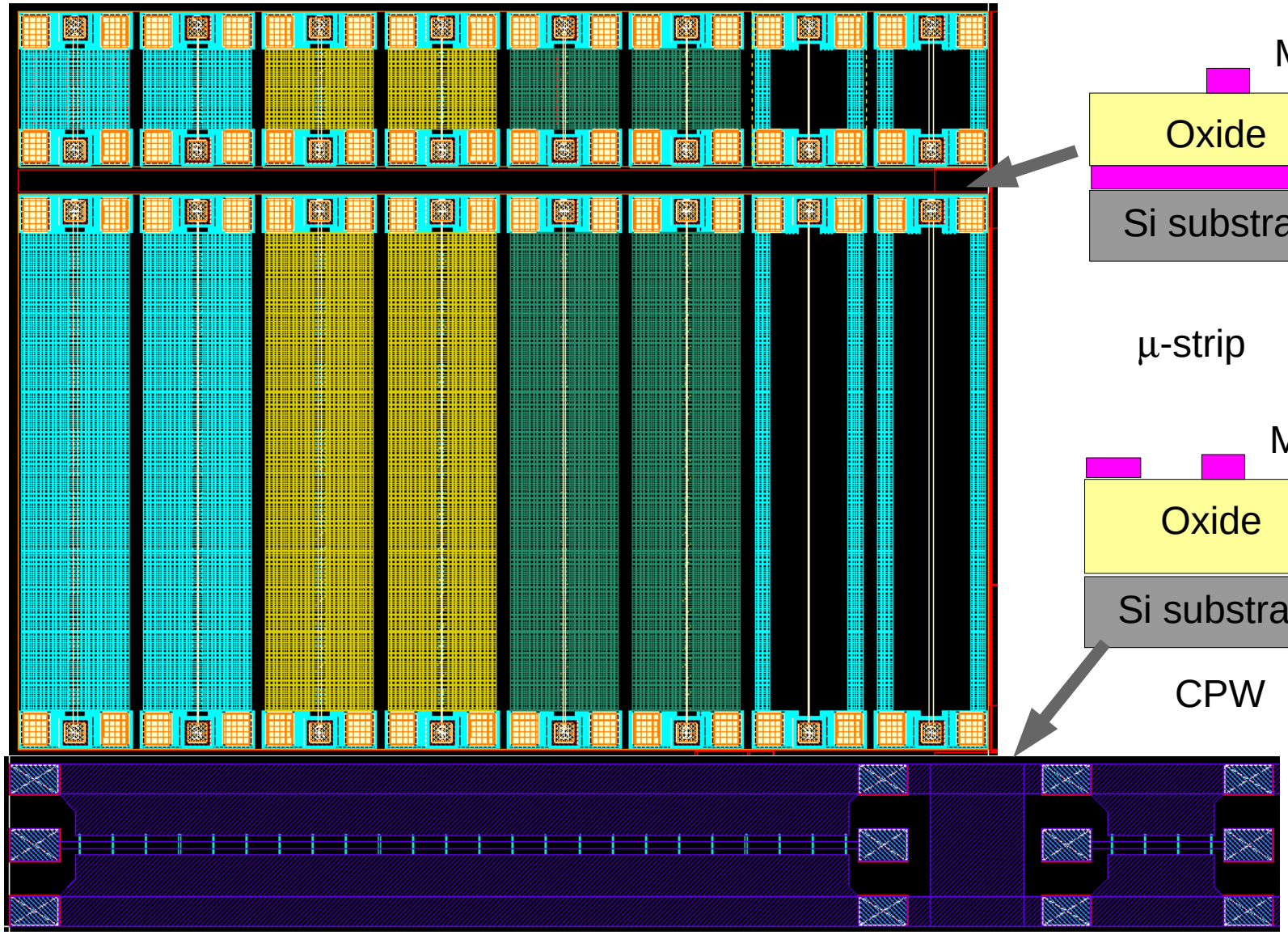
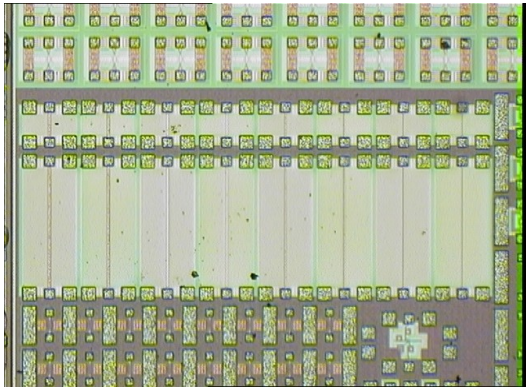
- MIM Capacitors
- Resistors

Transmission lines

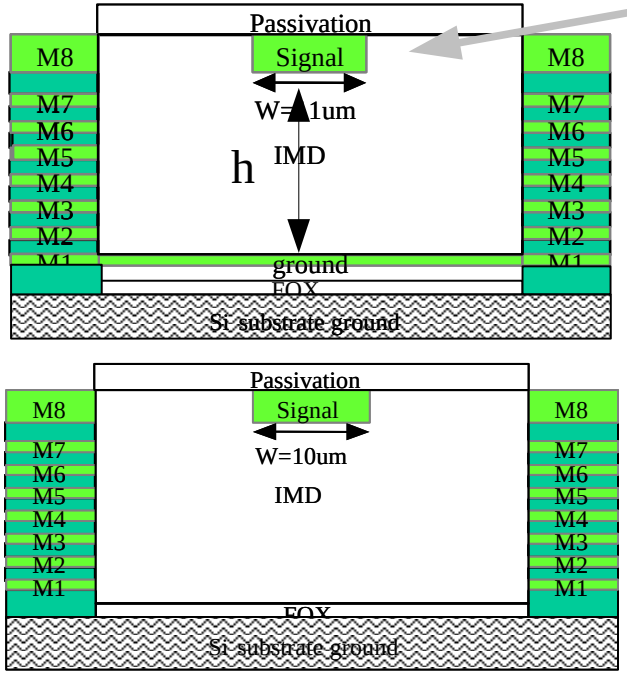


Interconnect as Transmission Lines



Layout-view of T-line test structures

$$L_{s1}+L_{s2}=l\frac{\mu_0}{2\pi}\ln\left(\frac{8h}{W}+\frac{W}{4h}\right)$$



X-section of T-line w/i and w/o gnd metal

Transmission lines

- Show up in ICs:
  - by design: as circuit matching elements (preferably as Metal-Oxide-Metal – MOM lines), or
  - inevitably, as interconnect (as Metal-Oxide-Silicon lines)
- In Si ICs, μ-strip or GCPW have lower loss than CPW
- Use M1, M2 or M1+M2, M1+M2+M3 ground planes
- Loss mechanisms similar to inductors (no proximity effect)

Transmission line params and models

- Most important HF performance parameters:
  - Characteristic impedance: Z_0
  - Attenuation (/mm): α
  - Group delay (/mm): τ
- Use simulator built-in models for GaAs, InP, Si M-O-M μstrip lines (ADS > Hspice > Spectre)
- Use lumped scalable RLC model for Metal-Over-Silicon lines
- Can be extracted from measurements or EM simulations

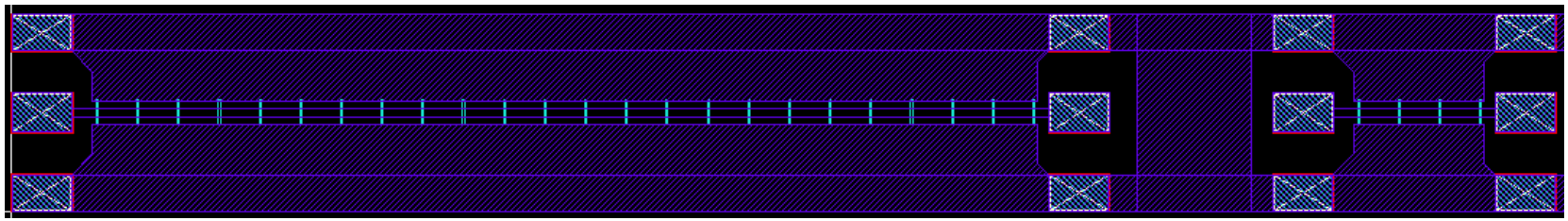
T-line de-embedding technique

Goal: Remove impact of pad parasitics

Test structures: long (1.2/0.6 mm) and short (200/100 μm) lines

How? 1-step de-embedding based on ABCD and Y matrices

Outcome: Determine Z_C, γ, α, τ_G, ε_{eff} of intrinsic line from ABCD matrix.



T-line param. extraction from ABCD matrix

Impedance of line of characteristic impedance Z_0 terminated on Z_L

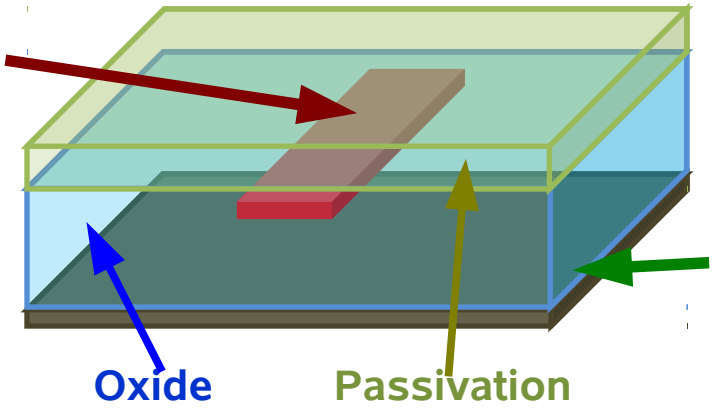
$$Z_{in} = Z_O \frac{Z_L + j Z_O \tan(\gamma d)}{Z_O + j Z_L \tan(\gamma d)} \quad \text{where } \gamma = \alpha + j\beta$$

$$\begin{vmatrix} A & B \\ C & D \end{vmatrix} = \begin{vmatrix} \cosh(\gamma d) & Z_O \sinh(\gamma d) \\ \frac{\sinh(\gamma d)}{Z_O} & \cosh(\gamma d) \end{vmatrix} \qquad \begin{vmatrix} v_1 \\ i_1 \end{vmatrix} = \begin{vmatrix} \cosh(\gamma d) & Z_O \sinh(\gamma d) \\ \frac{\sinh(\gamma d)}{Z_O} & \cosh(\gamma d) \end{vmatrix} \times \begin{vmatrix} v_2 \\ -i_2 \end{vmatrix}$$

$$Z_O = \sqrt{\frac{B}{C}} \qquad \gamma = \frac{\operatorname{acosh}(A)}{d} \text{ or } \gamma = \frac{\operatorname{asinh}(\sqrt{BC})}{d} \text{ where d = 1 mm}$$

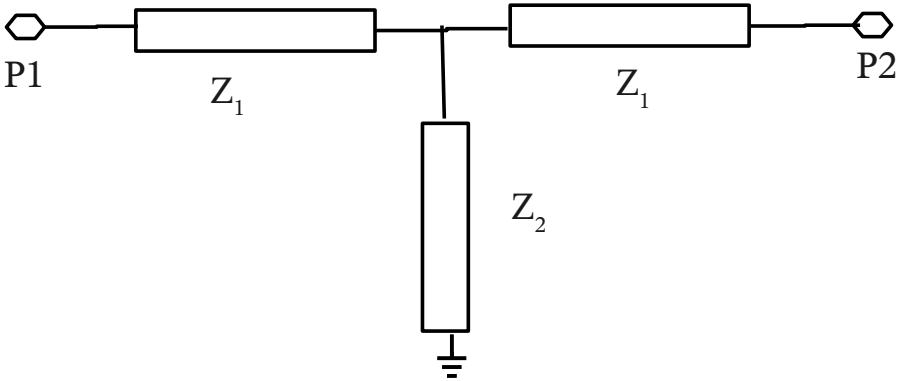
$$\alpha(\text{in dB}) = 8.688\,\Re(\gamma) \qquad \tau = \frac{\partial \beta}{\partial \omega} \times d \qquad \epsilon_{reff} = \left(\frac{\tau c}{d}\right)^2 \quad \text{where } c = 3 \times 10^8 \frac{m}{s}$$

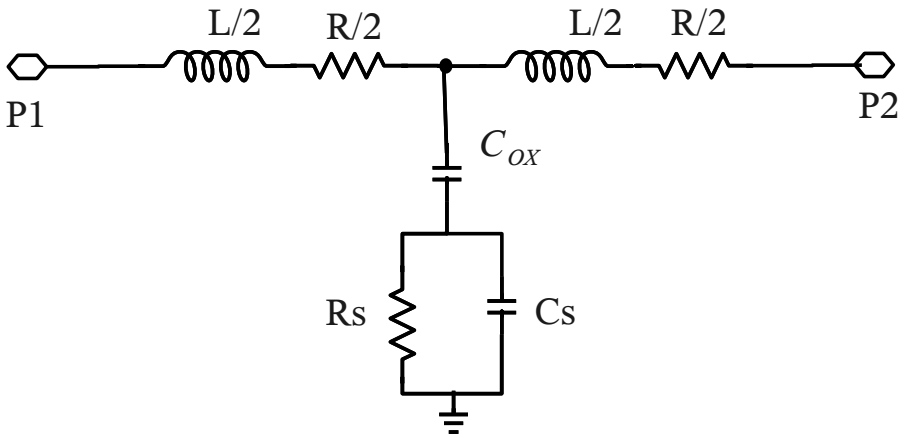
Simple lumped ckt. model without skin effect

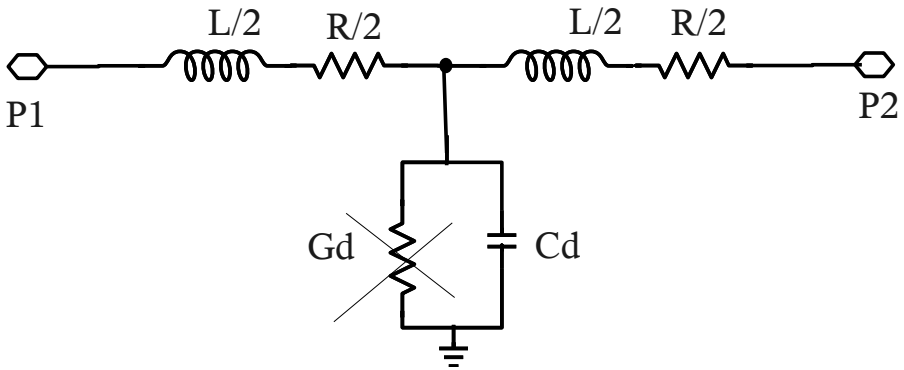


$$\frac{L}{C} = \frac{\mathbf{B}}{\mathbf{C}}$$

$$LC \approx \frac{-1}{\omega^2}\left(\frac{\cosh^{-1}(\mathbf{A})}{\ell}\right)^2$$

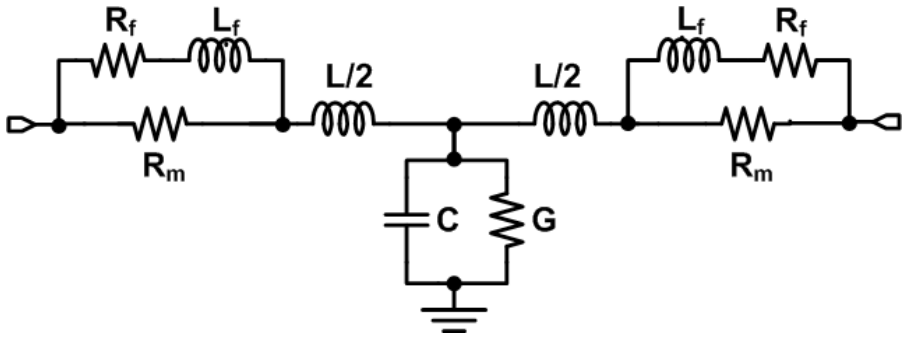






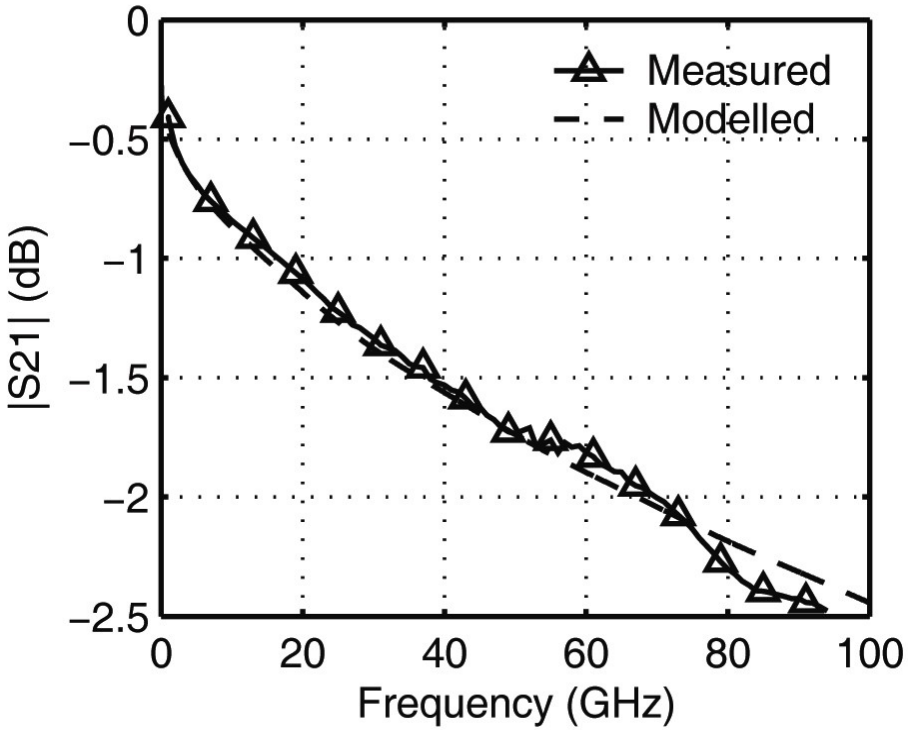
Extracting the lumped circuit parameters

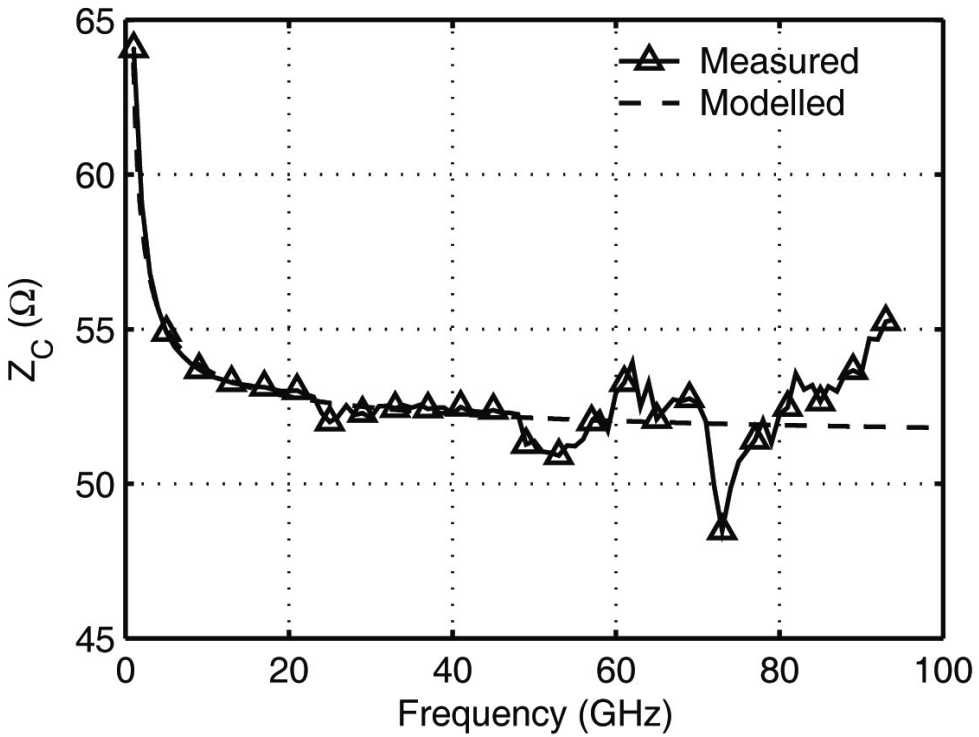
- Simulate (in HFSS) a line with *l*>=10μm to find ABCD params.
- Find L/C and LC (high freq.)
- G may be considered negligible
- Optimize L_f,R_f, & R_m (skin) to fit α & γ of model to HFSS simulation or measurements



- Compare simulations of 100μm or longer lines to verify scalability

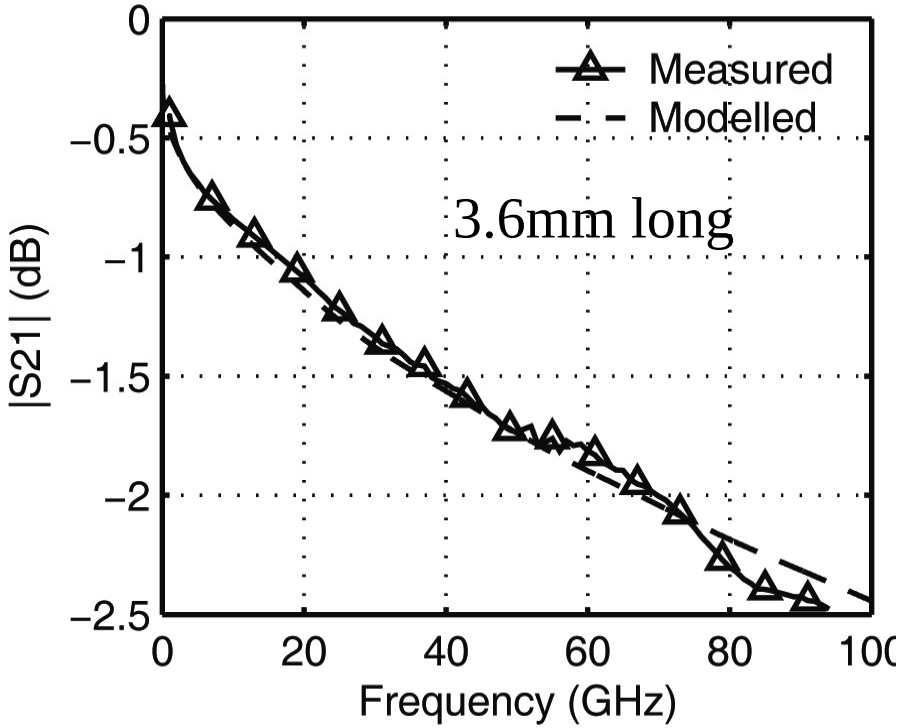
Example: Modelled vs. mea. 3.6-mm μstrip line

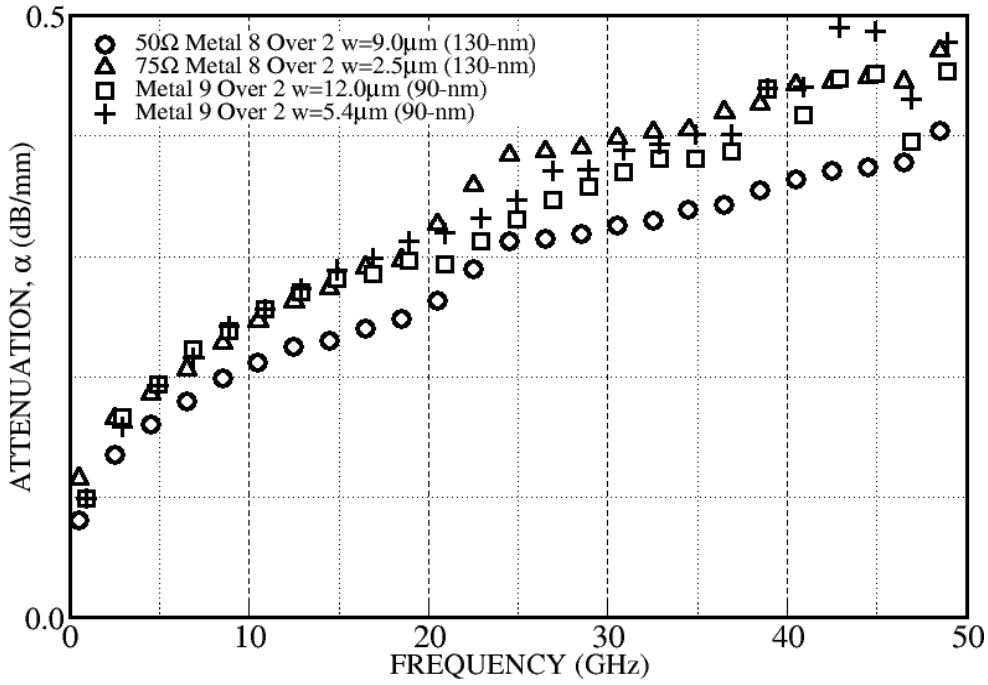




- Fitted RLGC model

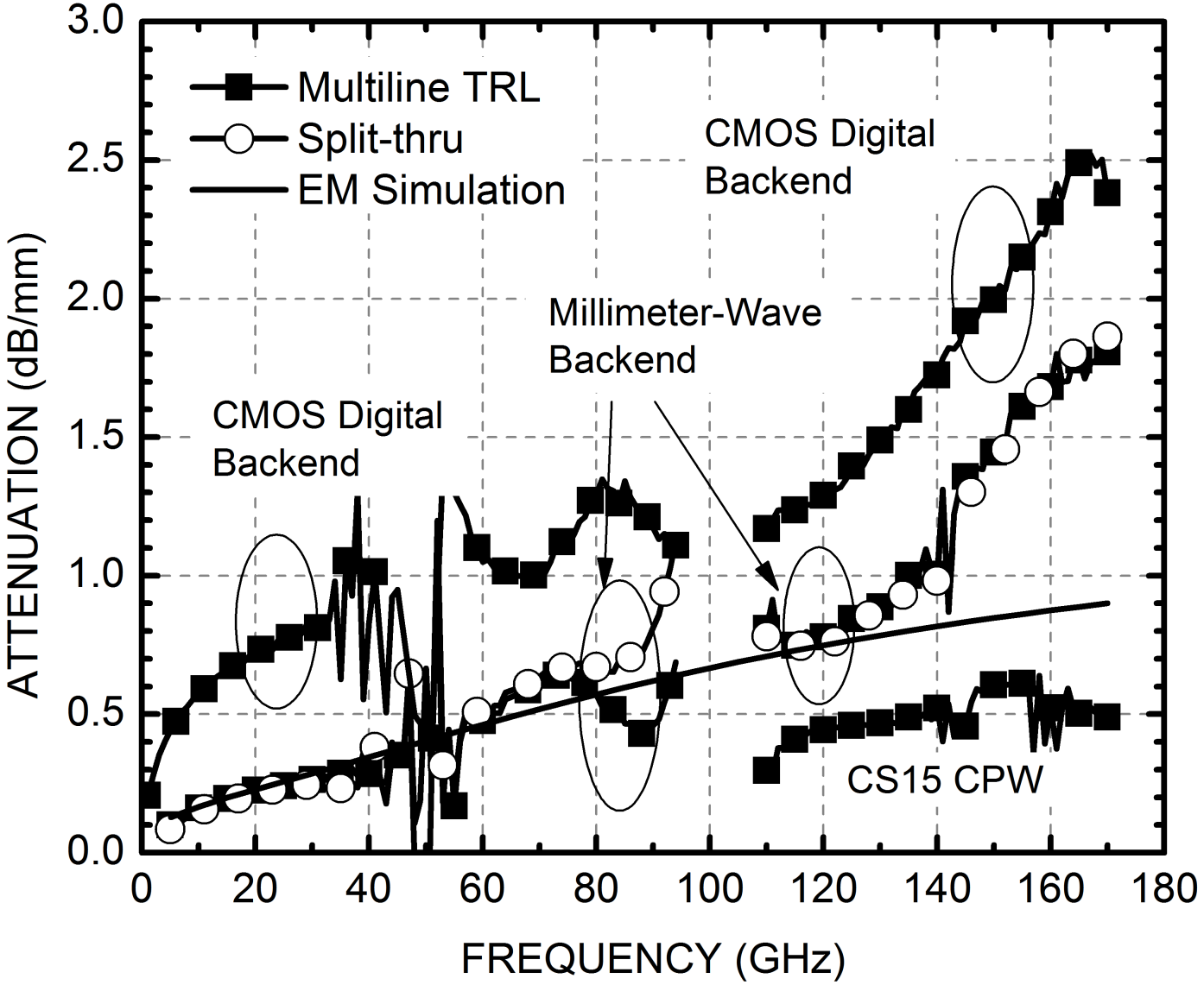
Comparable SiGe vs. CMOS µstrip lines





- CMOS-line attenuation getting slightly worse in new nodes
- 0.4 dB/mm @50GHz, 0.5 dB/mm@ 65GHz, 0.66 dB/mm@ 94GHz,

T-line loss in thin and thick metal BEOLs



Outline

- Inductors
- Transmission lines
- Varactors
- MIM Capacitors
- Resistors

Variable capacitance devices: Varactors

Figures of merit

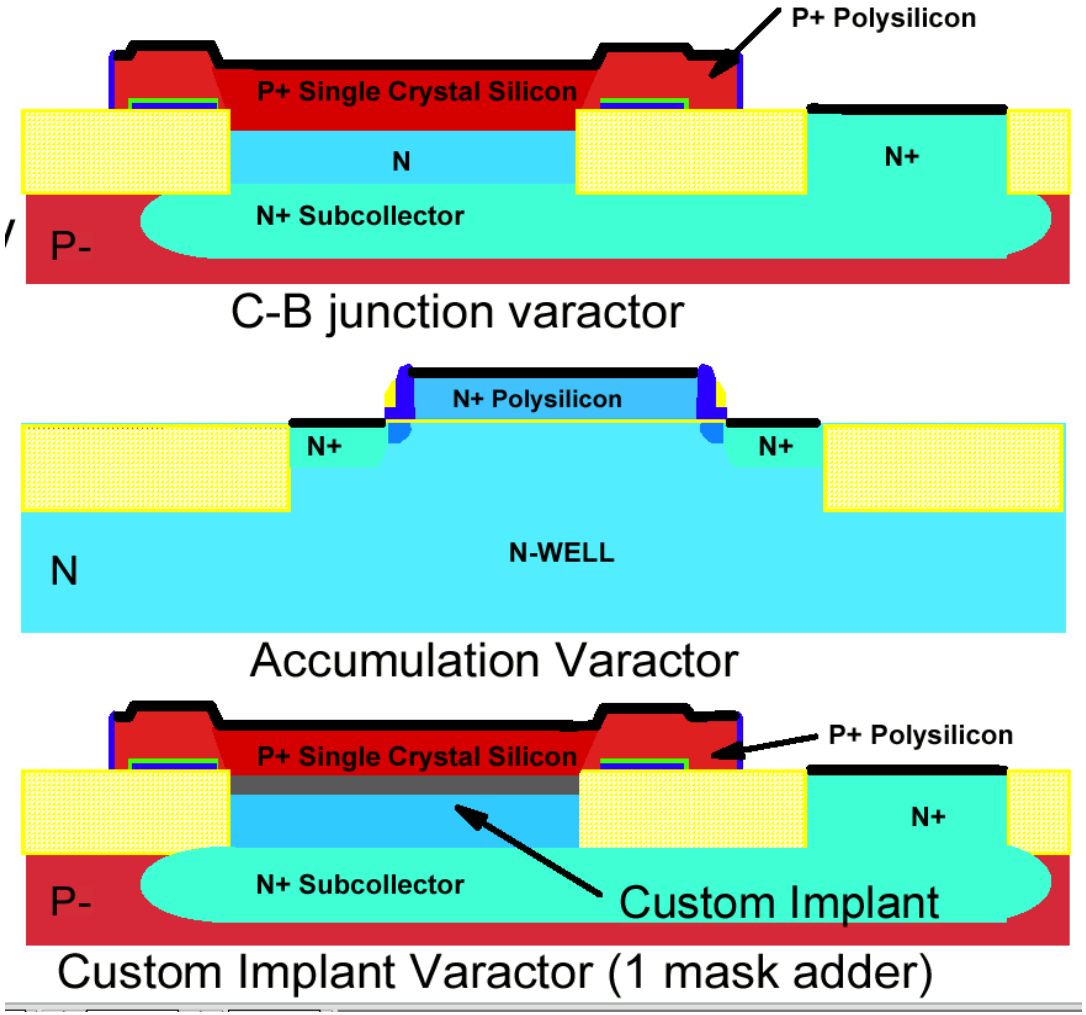
- capacitance ratio: C_{MAX}/C_{MIN}
- quality factor Q
- linearity

Applications

- VCO

Implementation

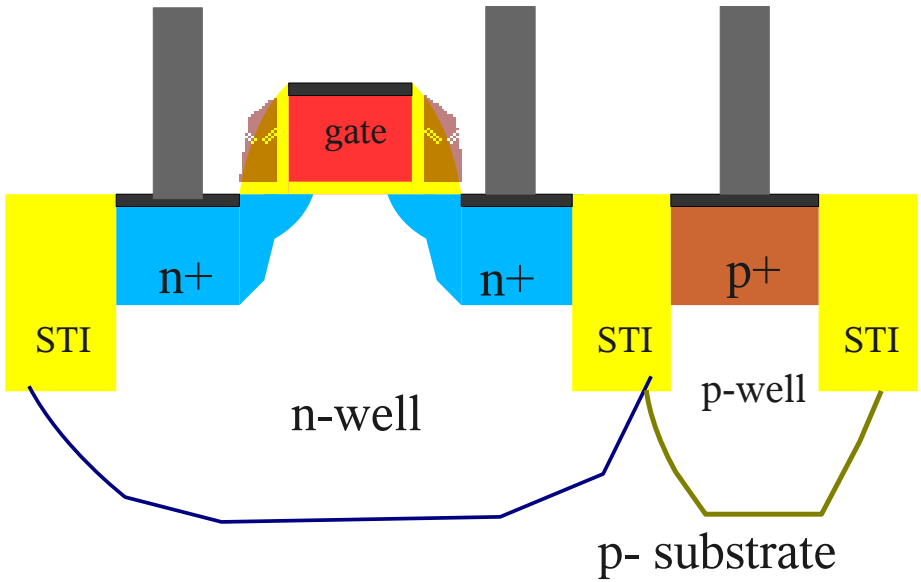
- p-n junction
- accumulation-mode MOS capacitor

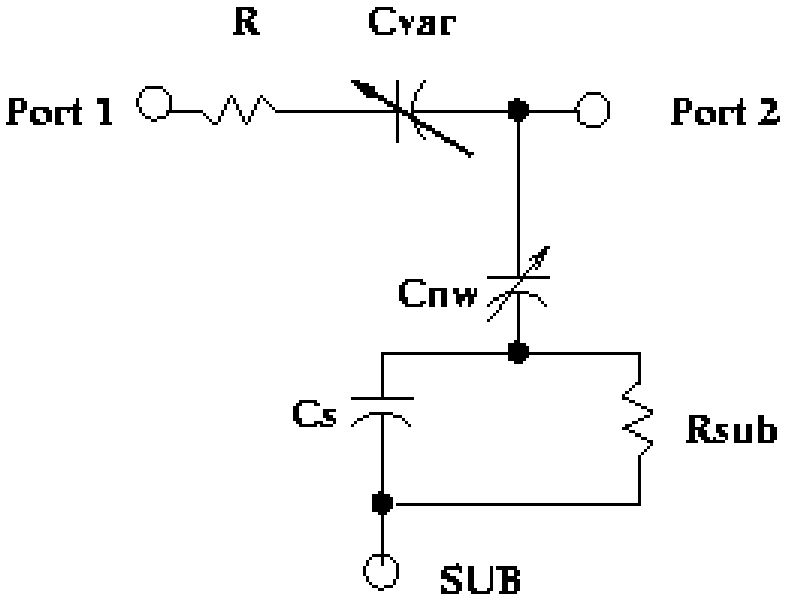


Common-sense rules

- Accumulation-mode MOS (AMOS) varactors have higher Q and larger tuning range than pn junction varactors
- If varactor model is not available, build a rudimentary model:
  - use MOSFET with S/D tied together
  - Add gate resistance externally, as for MOSFET
  - Calculate $C_{MAX} = C_{OX} \times W \times L + 2C_{ov}$
  - $C_{MIN} = C_{MAX}/2$
- Smaller varactors (W and W_f) have higher Q's at a given frequency

Extraction of simplified equivalent circuit





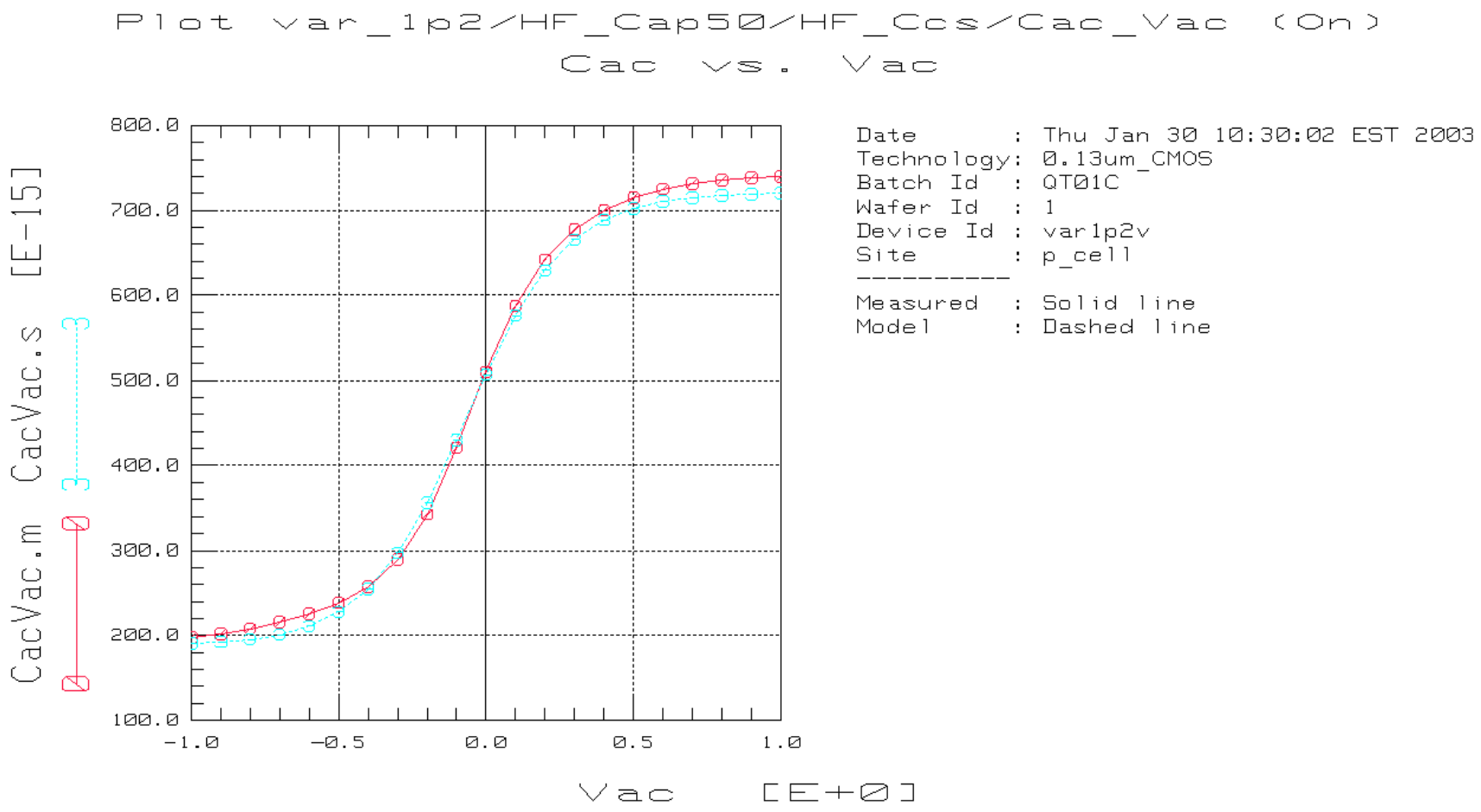
$$C_{var} = \frac{\left[\Im\left[-Y_{12}^{-1}\right]\right]^{-1}}{\omega}$$

$$C_{nw} = \frac{\left[\Im\left(Z_{21}\right)\right]^{-1}}{\omega}$$

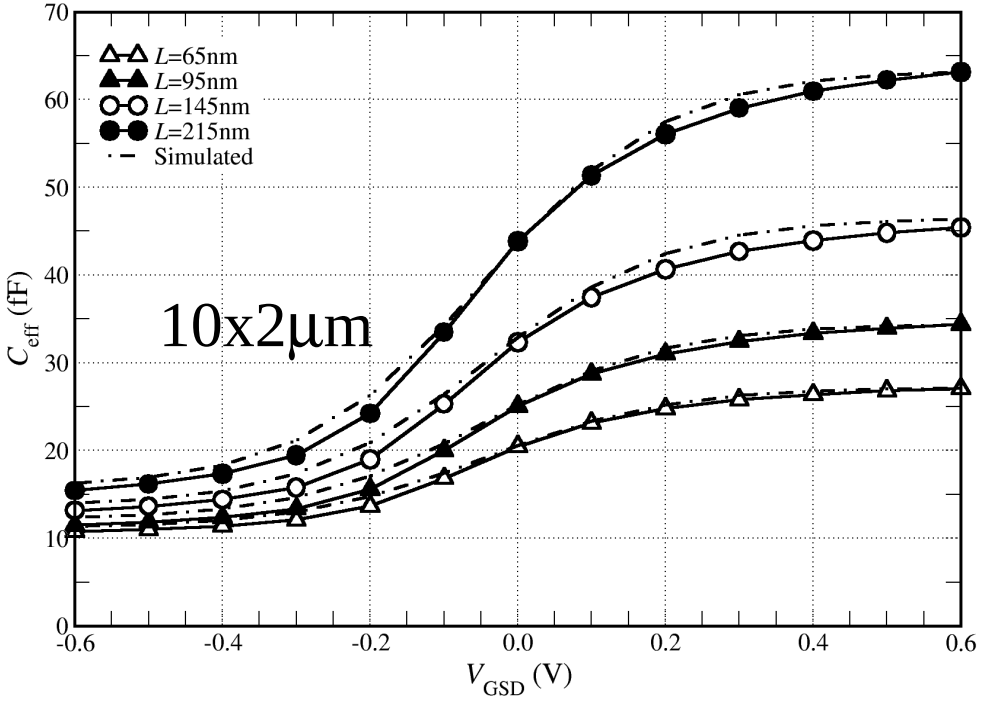
$$R = R_G + R_{CH} = \Re\left(Z_{11} + Z_{22} - Z_{12} - Z_{21}\right)$$

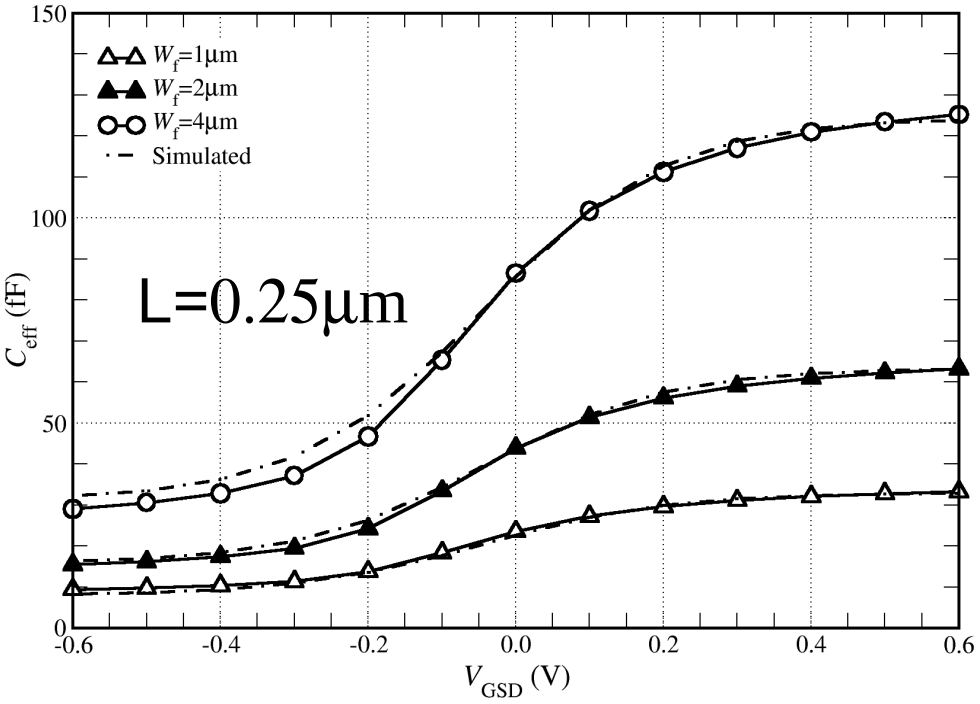
$$R_{sub} = \Re\left(Z_{21}\right)$$

Meas. vs. sim. C_{var}(V) for 1.2V, 130nm device



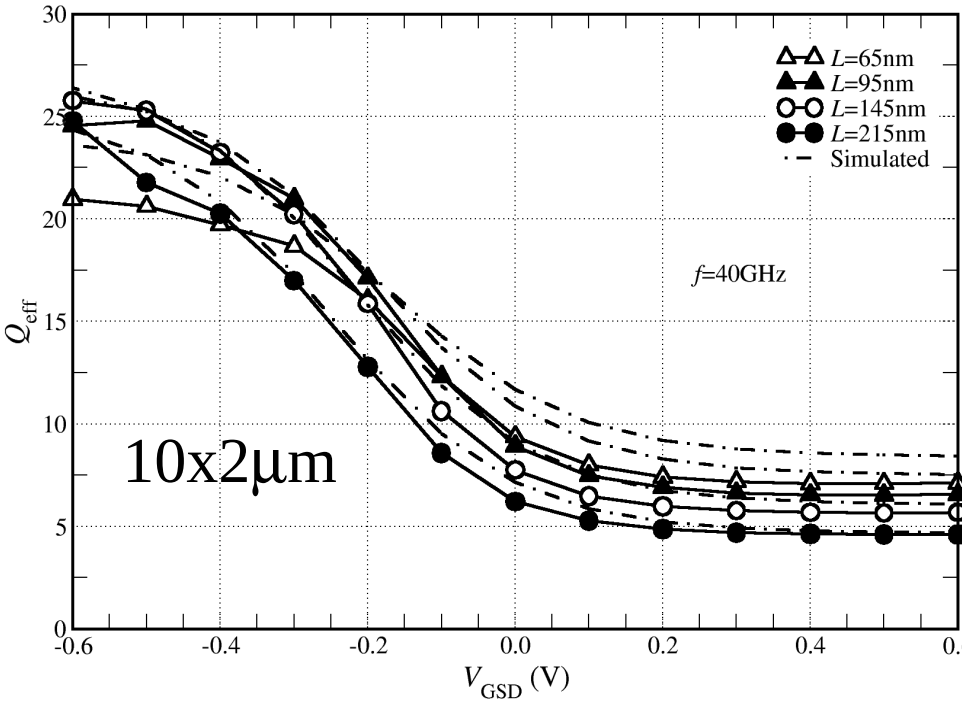
90nm AMOS varactors: C_{eff}

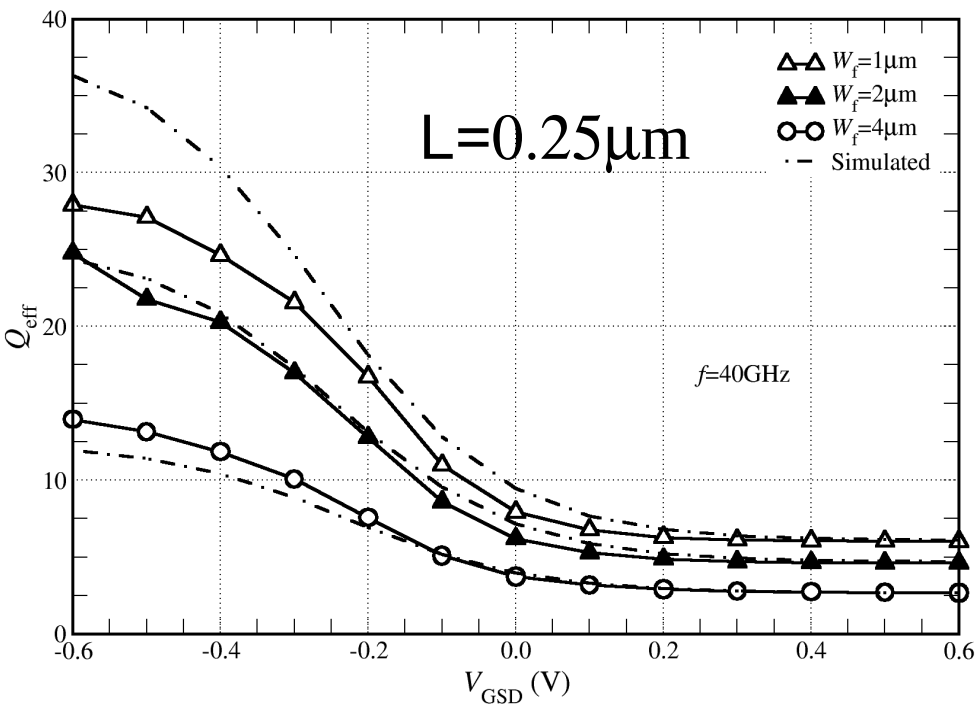




- Scales well with W_f and L.
- Physical model matches measurements of C_{eff} well:
  - Captures dependence on W_f and L.
  - Captures bias dependence.

90-nm AMOS varactors: $Q_{eff} \propto 1/(C_{eff} R_{eff})$





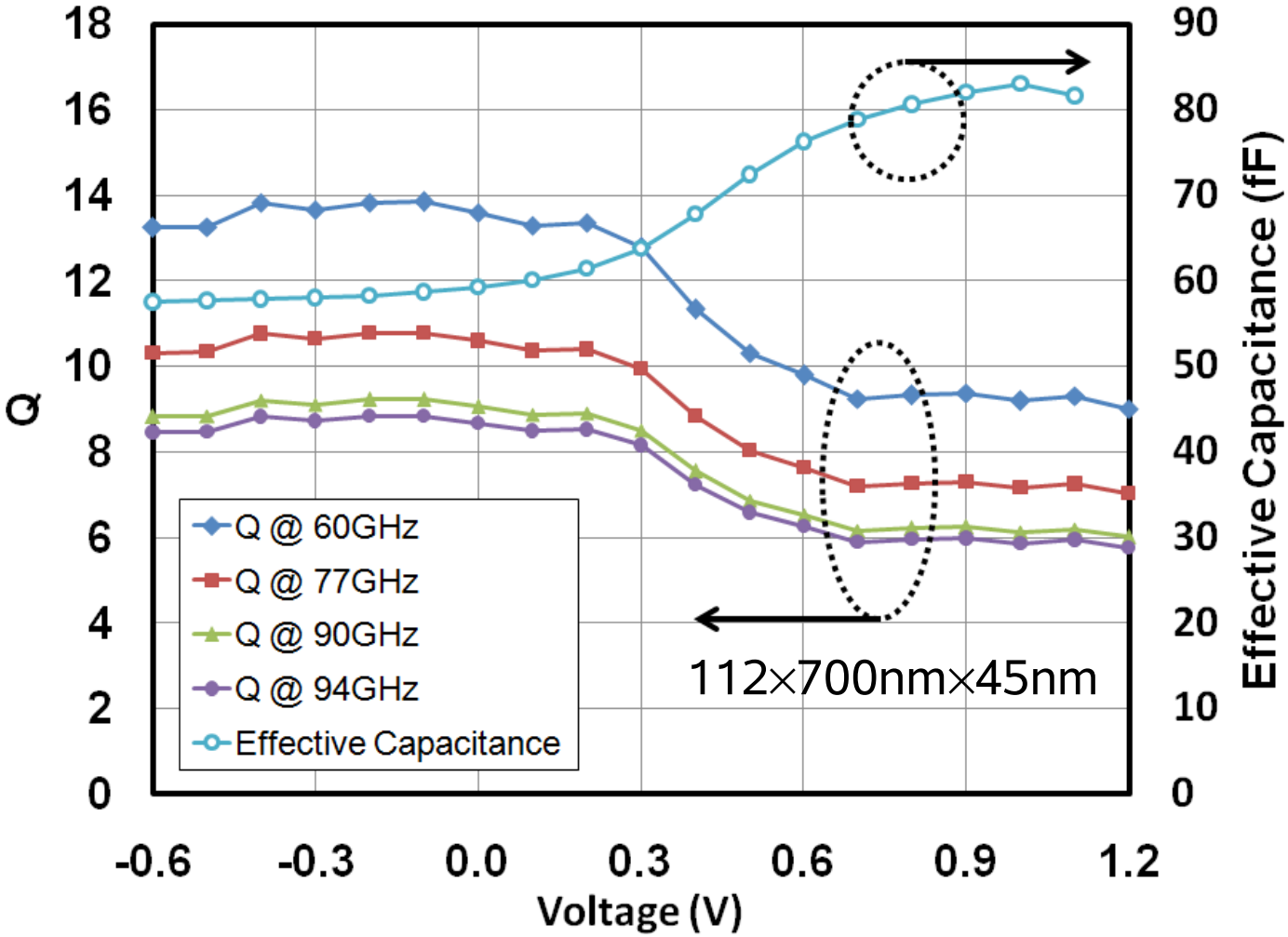
- Decreases with W_f.
- Decreases with L (due to L-indep. R term).
- Extracted model limited by measurement accuracy (R_{ch}).

Meas. 65-nm GP AMOS varactor at 94 GHz

Double-sided gate

- L_{drawn}=60nm, W_f=0.55µm, W_{total}=27.5µm, C_{VAR}=1.53fF/µm
- C variation: 25fF – 42fF, Q: 6 – 8 at 94 GHz

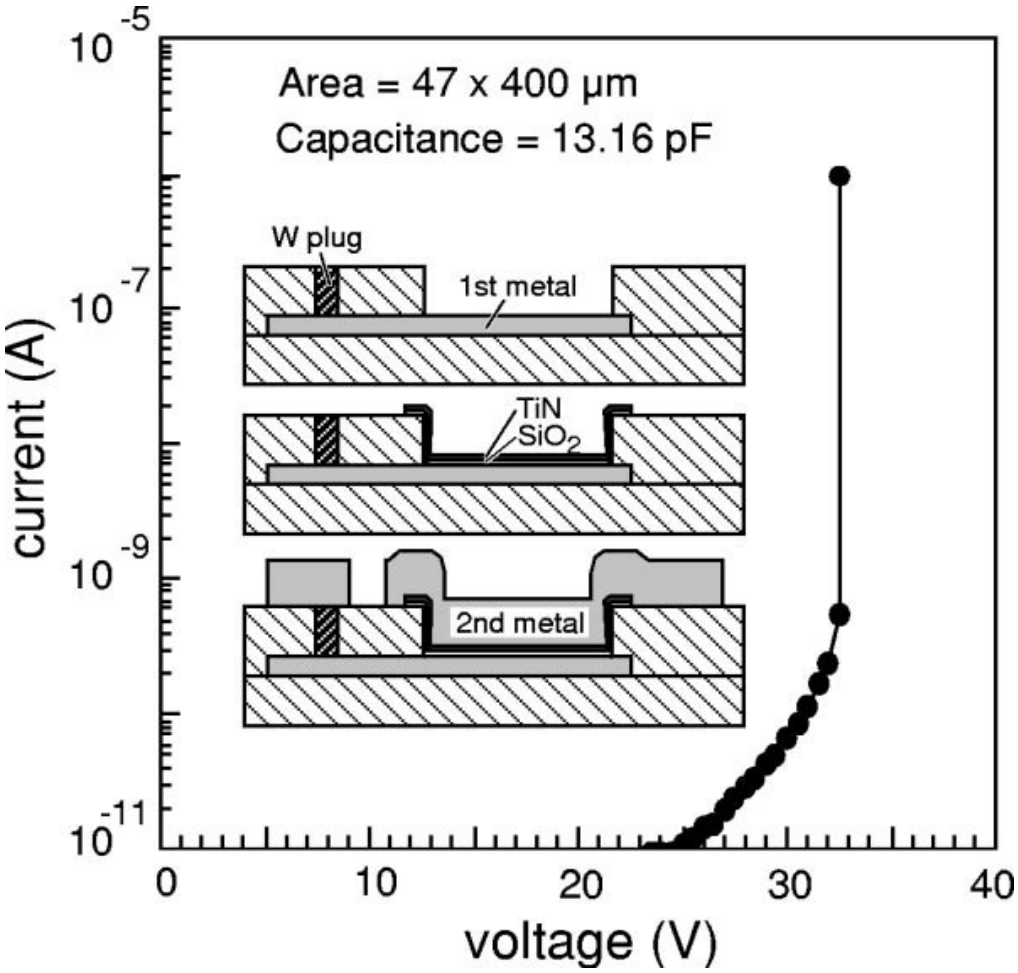
45-nm LP CMOS AMOS n-well varactor



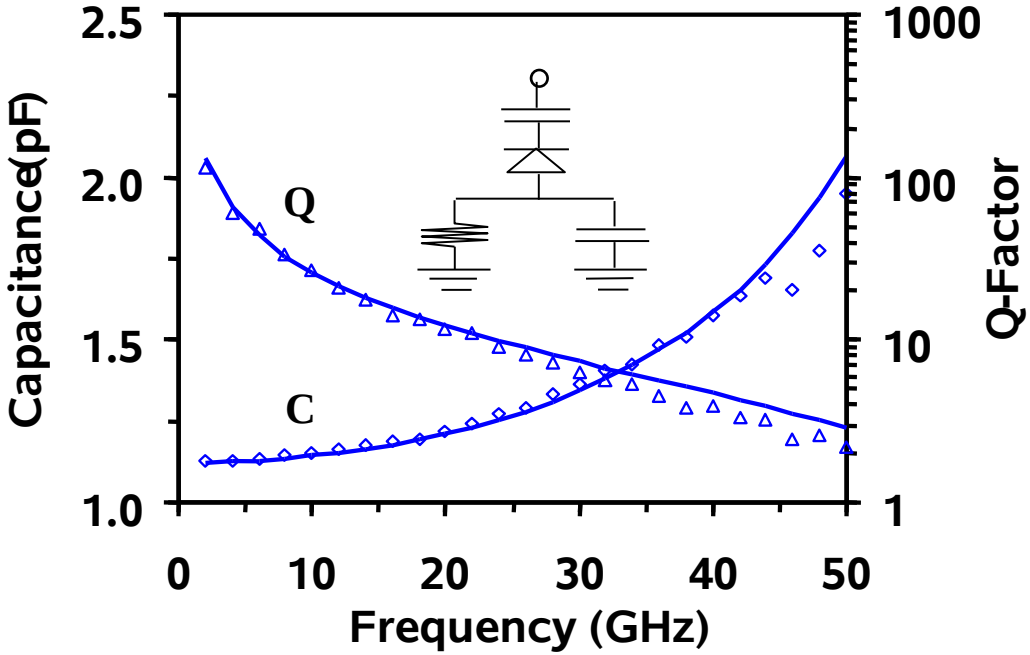
- L_{drawn}=45nm, W_f=0.7µm, W_{total}=78.4µm, C_{VAR}=1.07fF/µm
- C variation: 58fF – 84fF, Q= 6-8.5 at 94 GHz

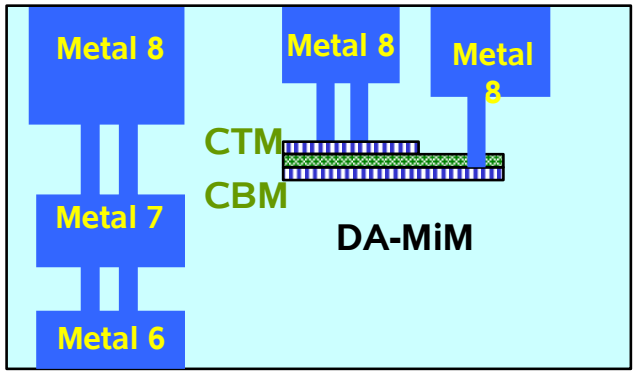
MIM Capacitor

- Figures of merit
  - Capacitance per area
  - Quality factor Q
  - Capacitance to substrate
- Issues with reliability
- Very good linearity
- Applications
  - VCOs
  - Low-noise amplifiers
  - mixers

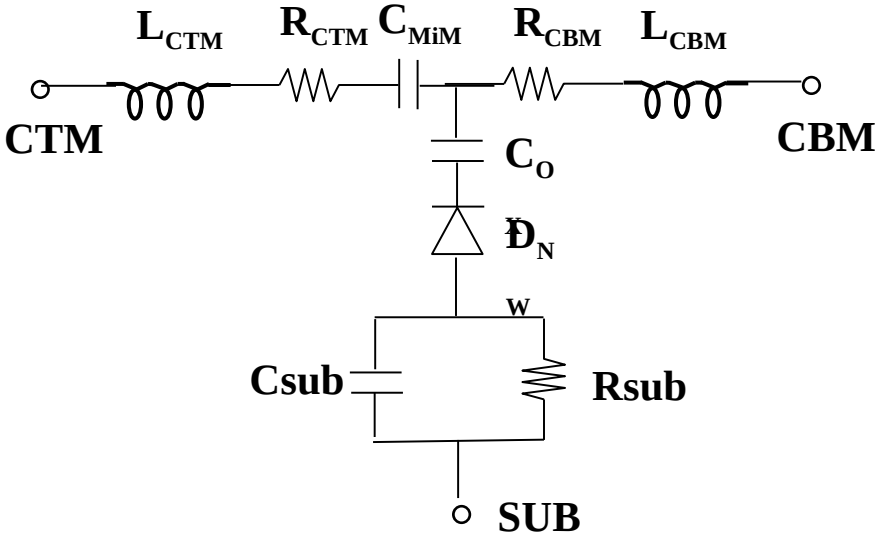


Measured vs. Modelled Characteristics





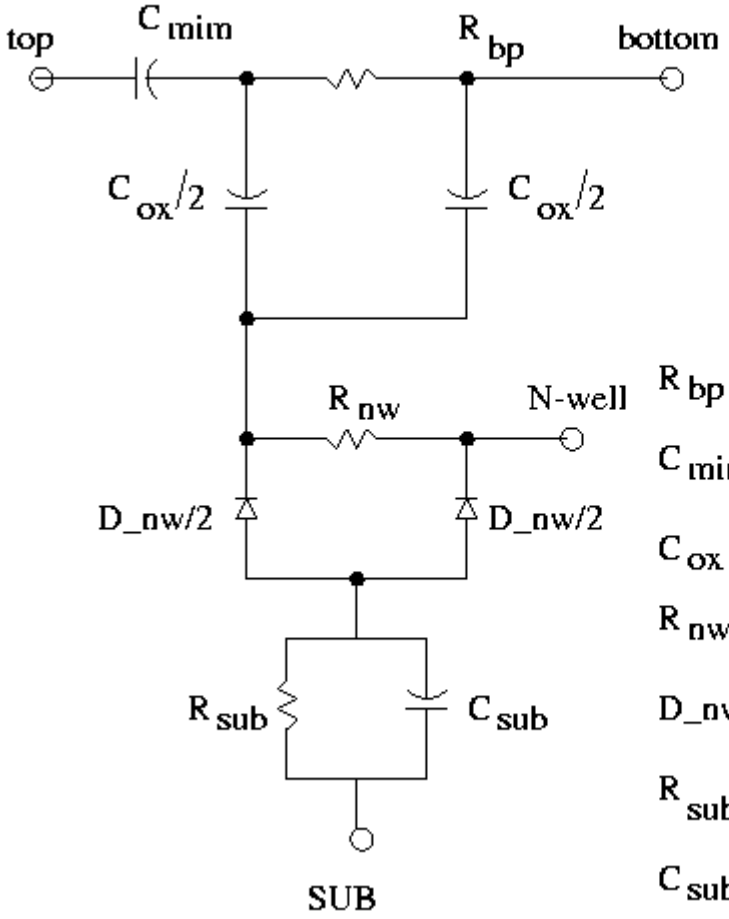
Cross-sectional view of DA MiM_Cap



Equivalent circuit used for MiM_Cap model

HF MIM capacitor equiv. ckt.

- use reversed biased n-well for good substrate isolation



R_{bp} - bottom plate resistance

C_{mim} - MIM capacitance

C_{ox} - oxide capacitance

R_{nw} - N-well resistance

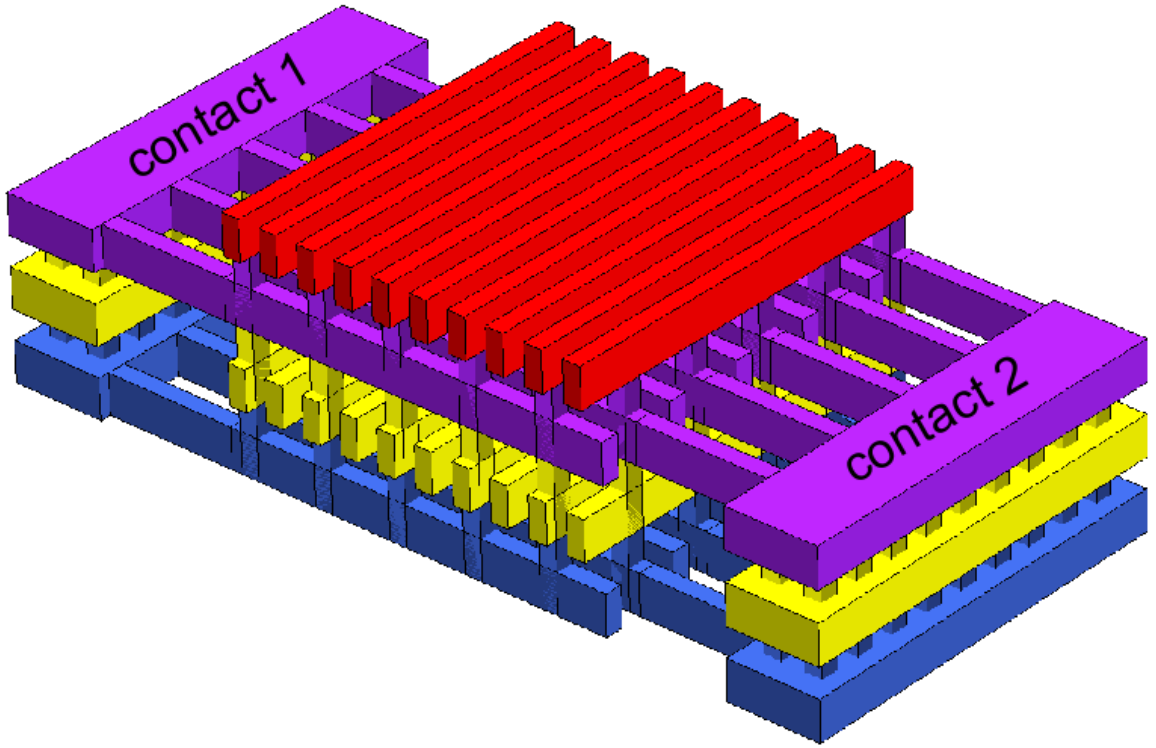
D_nw - N-well/P-sub junction

R_{sub} - substrate resistance

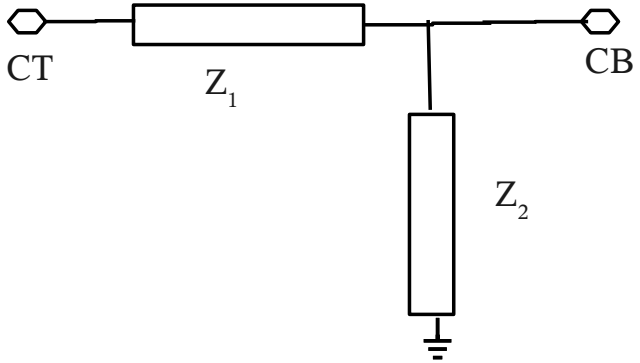
C_{sub} - substrate capacitance

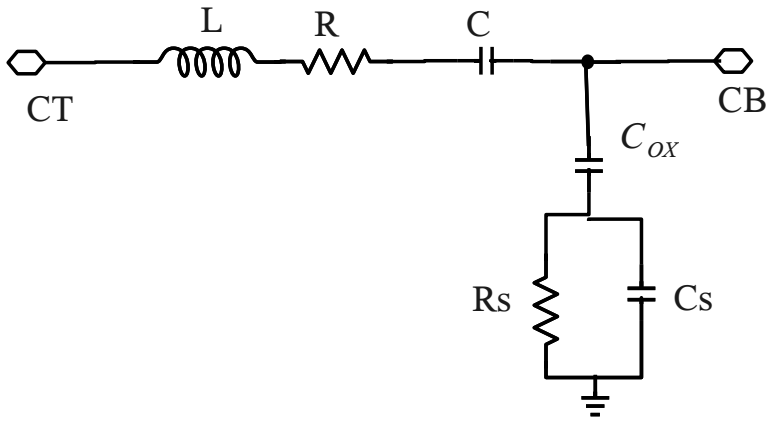
MOM capacitor

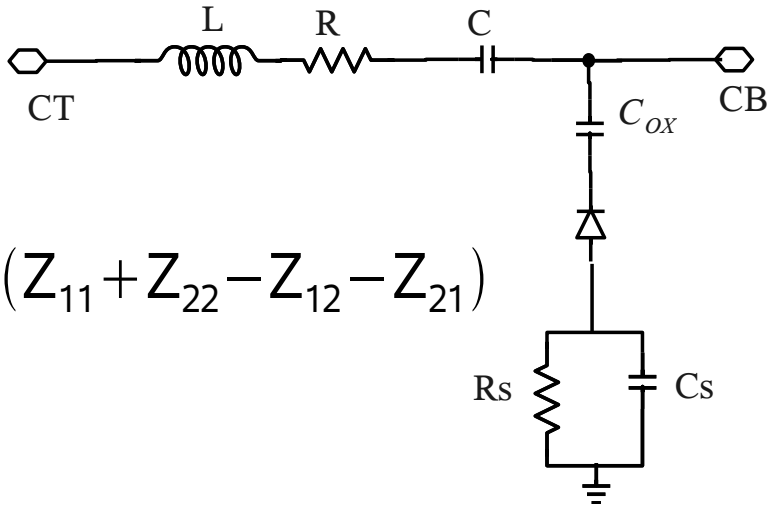
- Uses the fringing capacitance between dense metals
- Requires no additional process option (comes for “free”)
- Lower Q than a MIM capacitor



Extraction of simplified ckt. for MIM/MOM cap







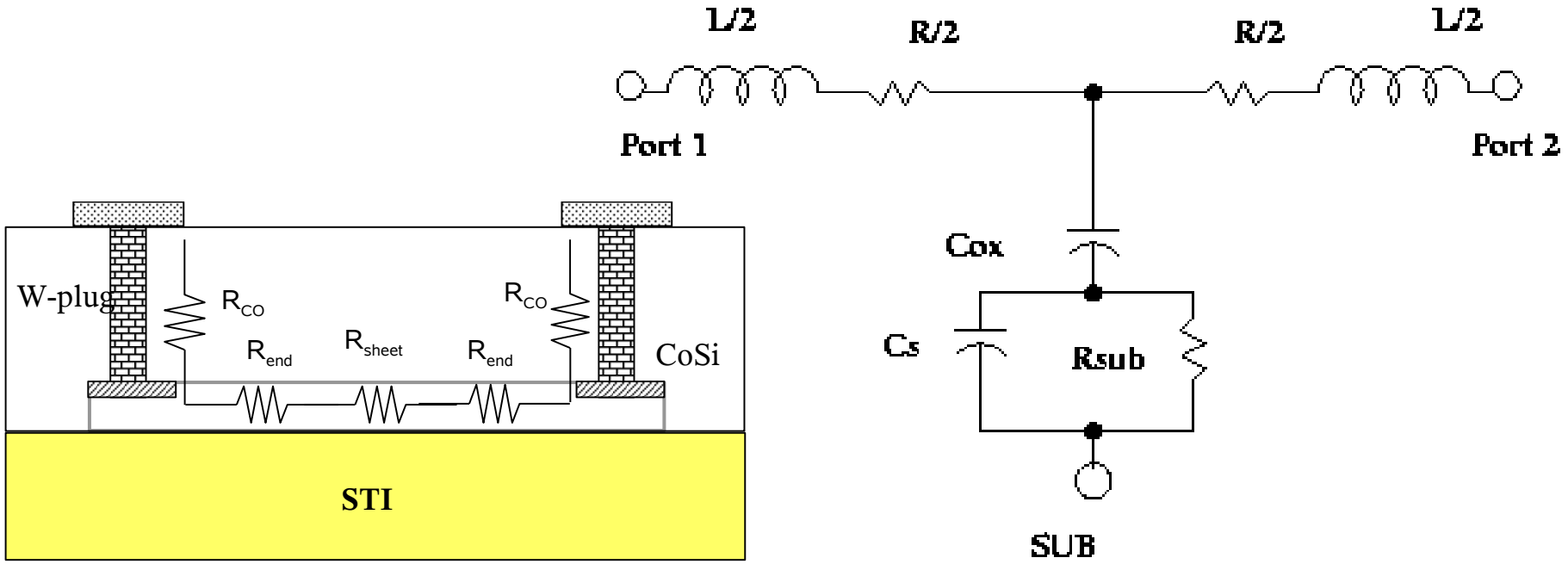
$$C_{mim} = \frac{\left[\Im\left[-Y_{12}^{-1}\right]\right]^{-1}}{\omega}$$

$$R = R_{TOP} + R_{BO} = \Re\left(Z_{11} + Z_{22} - Z_{12} - Z_{21}\right)$$

$$C_{OX} = \frac{\left[\Im\left(Z_{21}\right)\right]^{-1}}{\omega}$$

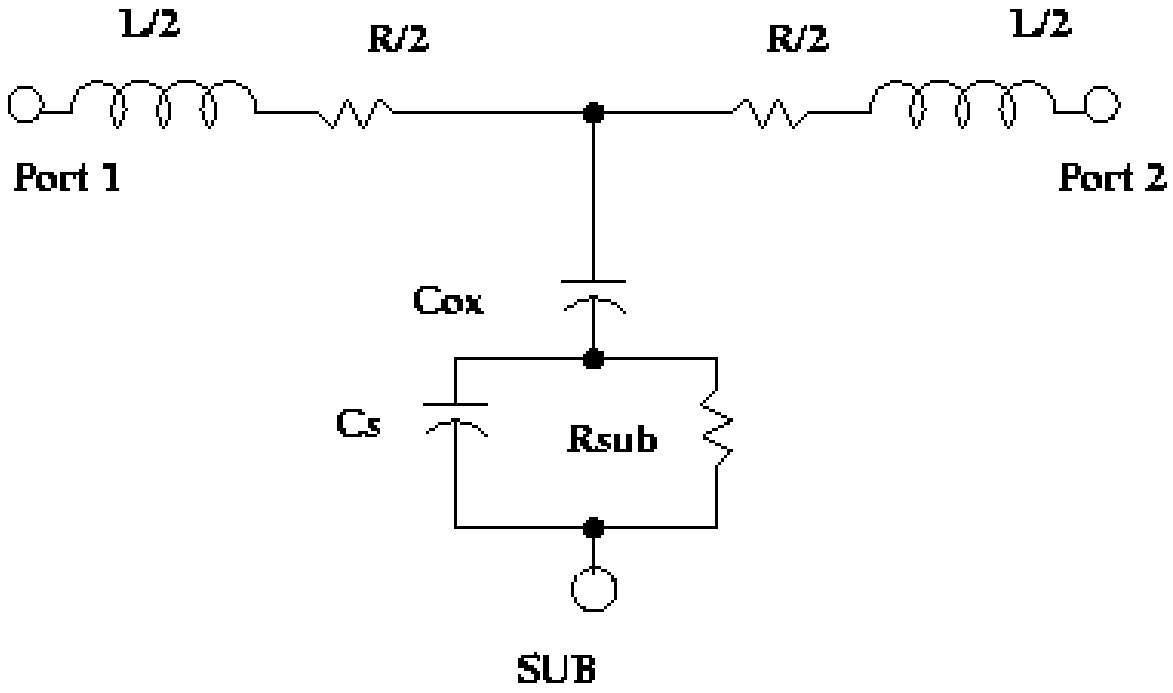
$$R_{sub} = \Re\left(Z_{21}\right)$$

HF resistor equivalent circuit



- T-circuit imposes use of Z parameters.
- 2π-circuit is more accurate for long resistors but is in most cases not necessary.

HF resistor equivalent circuit extraction



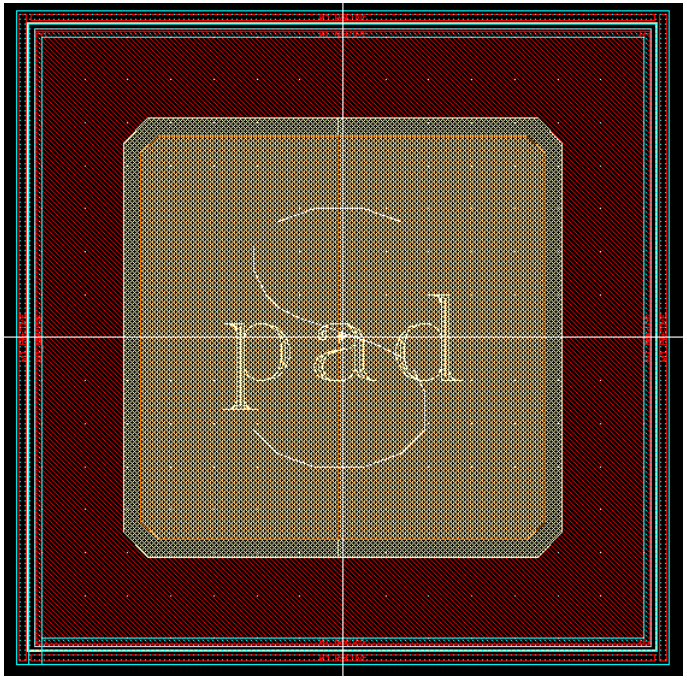
$$L = \frac{\Im(Z_{11} + Z_{22} - Z_{12} - Z_{21})}{\omega}$$

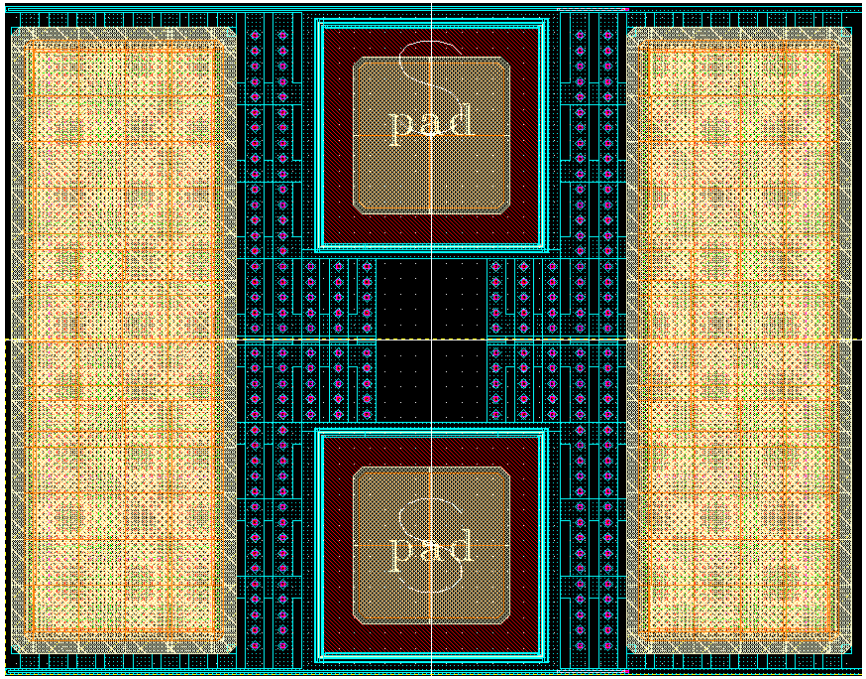
$$R = \Re(Z_{11} + Z_{22} - Z_{12} - Z_{21})$$

$$C_{OX} = \frac{[\Im(Z_{21})]^{-1}}{\omega}$$

$$R_{sub} = \Re(Z_{21})$$

RF pads





- Top metal only
- Reversed-biased salicided n-well or metal-1 grounded n-well

Using ASITIC to calculate HF equiv. ckt. parasitic elements of passive components

- MIM caps, poly resistors, varactors have identical substrate network (R_{sub}, C_{sub})
  - Use ASITIC to π–model the substrate network for a metal line of similar width and length,
- MIM caps and poly resistors are realized in the oxide, above the silicon substrate
  - Use ASITIC to π–model C_{ox}, L, R for a metal line of similar width and length and located at the same distance from the substrate as the MIM cap or poly resistor

Summary

- Inductors and transformers: main design components available to HF circuit designers
- Unlike transistors, they are almost insensitive to process variation
- Inductors and transformers are scalable to at least 200 GHz
- Modelling of passives as critical as the transistor model
- In Si HF ICs t-line matching should be avoided < 100 GHz because of large area
- Varactors, capacitors and resistors have RLC parasitics which must be accurately modelled at HF