4.6.7. Wide-band LNAs, "noise signal feedback" and "noise cancellation"

Another approach to the LNAs different from the conventional amplifiers tuned to a certain frequency at the output, is to design a wide-band amplifier and to define the operating frequency at the input with a suitable passive band-pass filter or directly using the tuned behavior of the antenna. With this approach it is possible to use a wide-band amplifier for any frequency, certainly in the band of the amplifier, only by changing the input filter or the antenna. Another advantage of this approach is reduced neighboring channel interferance.

From the basic noise theory (4.6.3.1) it is known that the thermal noise generated in a resitor can be characterized with its r.m.s. voltage or current as

$$\overline{v}_n = \sqrt{4kTB \times R}$$

$$\overline{i}_n = \sqrt{4kTB / R}$$

These are the r.m.s. values of the noise voltage or the noise current that are randomly varying "noise signals".

Similarly, the r.m.s. channel noise current generated in the inversion channel resistance of a MOS transistor is

$$\overline{i}_{n-ch} = \sqrt{4kTB / R_{ch}}$$

It can be theoretically shown that the channel resistace for a non velocity saturated transistor is equal to $2/g_m$ and hence the mean square channel noise current becomes

$$\overline{i}^2_{n-ch} = 4kTB \times \frac{1}{2} g_m$$

But it has been experimentally deduced that it is more realistic to write the expression as

$$\overline{i}^2_{n-ch} = 4kTB \times \gamma \times g_m \qquad (4.153)$$

where γ is a parameter[1]. The numerical value of γ usually varies from 0.5 to 0.8, and it is at the high end of this interval for velocity saturated transistors.

It must not be overlooked that the noise voltages and currents of the resistors and transistors in a circuit are processed (amplified, fed-back, mixed, etc.) as other signals in the circuit, until they reach the output circuit. Then their contribution to the total noise power at the output must be calculated and added-on to find the total noise power. The r.m.s. values are necessary at this stage. However, calculating the noise r.m.s values *in advance* will mask some important effects; such as "noise feedback" that has been known since the early days of electronics[2] , and the "noise cancellation" techniques that appeared in several recent publications.

This fact will be exemplified on several basic circuits below.

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[1] A.J. Scholten et al. "Accurate Thermal Noise Model for Deep-Submicron CMOS", IEDM 1999.

[2] For example: H.J. Reich, " Theory and Applications of Electron Tubes", p. 201, McGraw-Hill, 1944.

4.4.7.1. The common gate amplifier as a wide-band LNA

In a common gate amplifier given in Fig.4.59, there are three noisy components; the internal resistance of the input signal source, R_A, the MOS transistor and the load resistor, R_L .

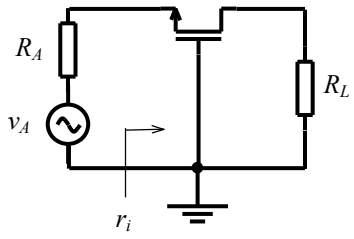


Figure 4.59 . The principal circuit diagram of a common gate amplifier

The contributions of these noise components to the output noise are as follows:

a) Contribution of R_A: The instantaneous value of the noise voltage of the source resistance (v_{nA}) is transferred to the input of the amplifier as

$$v_{ni} = \frac{r_i}{R_A + r_i} v_{nA}$$

and then amplified by the transistor with a voltage gain of $A_v \cong g_m R_L$. Provided that the amplifier can be considered as linear for this signal level, the amplified noise voltage at the output is a replica of the noise voltage at the input and the r.m.s value of this voltage is equal to

$$\overline{v}_{nAo} = A_v \times \overline{v}_{ni} = A_v \times \frac{r_i}{R_A + r_i} \overline{v}_{nA} \qquad (4.154)$$

and if the input is matched, i.e. $r_i = R_A$

$$\overline{v}_{nAo} = A_v \times \frac{1}{2} \overline{v}_{nA} = \frac{1}{2} g_m R_L \sqrt{4kTBR_A} \qquad (4.154\text{-a})$$

Since $R_A = r_i \cong 1/g_m$ for a common gate amplifier,

$$\overline{v}_{nAo} = \frac{1}{2} g_m R_L \sqrt{4kTB/g_m} \qquad (4.154\text{-b})$$

Hence the noise power dissipated on the load resistance owing to the noise of the source resistance becomes

$$P_{nAo} = \frac{\overline{v}_{nAo}^2}{R_L} = kTBg_m R_L \qquad (4.155)$$

b) Contribution of the channel noise: The channel noise current of the transistor $\overline{i}_{n-ch} = \sqrt{4kTB\gamma g_m}$ flows through the load resistor R_L as well as the internal resistance of the input signal source, R_A. The noise current flowing through R_A produces a voltage drop v_{ni} which provokes a channel noise current equal to $(v_{ni} \times g_m)$. This "feedback noise component" is in opposite direction with $i_{n\text{-}ch}$ and

therefore reduces it. This qualitative explanation can be developed with the inclusion of the effect of the internal resistance of the transistor as shown in the equivalent circuit in Fig. 4.60(b) from which the resulting output noise current can be calculated as

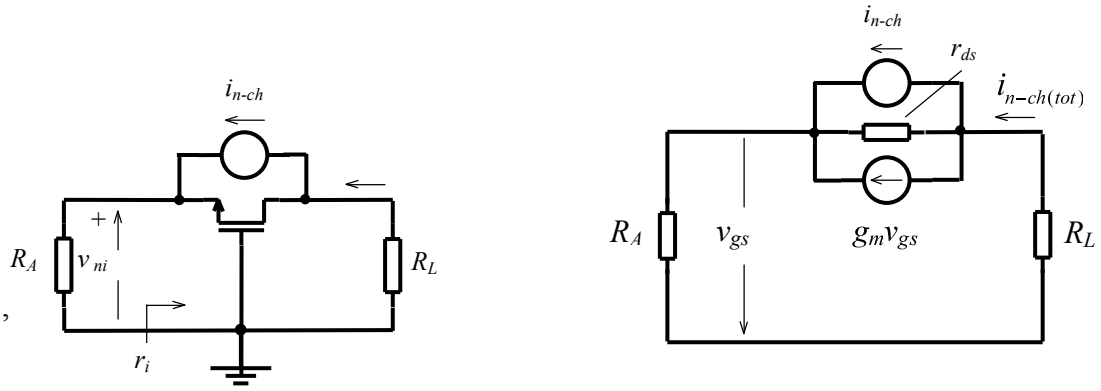


Figure 4.60(a). The channel noise current, (b) the equivalent circuit to calculate the internal feedback effect of this current.

$$i_{n-ch(tot)} = i_{n-ch}\frac{r_{ds}}{2r_{ds}+R_A+R_L} = i_{n-ch}\times\delta \qquad (4.156)$$

where δ is the noise reduction parameter that approaches to ½ for

$$(R_A+R_L) \ll 2r_{ds}$$

The r.m.s. value of this noise current

$$\overline{i}_{n-ch(tot)} = \delta\,\overline{i}_{n-ch} = \delta\sqrt{4kTB\gamma\, g_m} \qquad (4.156\text{-a})$$

The contribution of the channel noise on the output power now can be calculated as

$$P_{n-cho} = \overline{i}^{\,2}_{n-ch(tot)} \times R_L = \delta^2(4kTB\gamma\, g_m R_L) \qquad (4.156\text{-b})$$

c) The contribution of the load resistance noise on the total output noise is simply

$$P_{n-RL} = 4kTB \qquad (4.157)$$

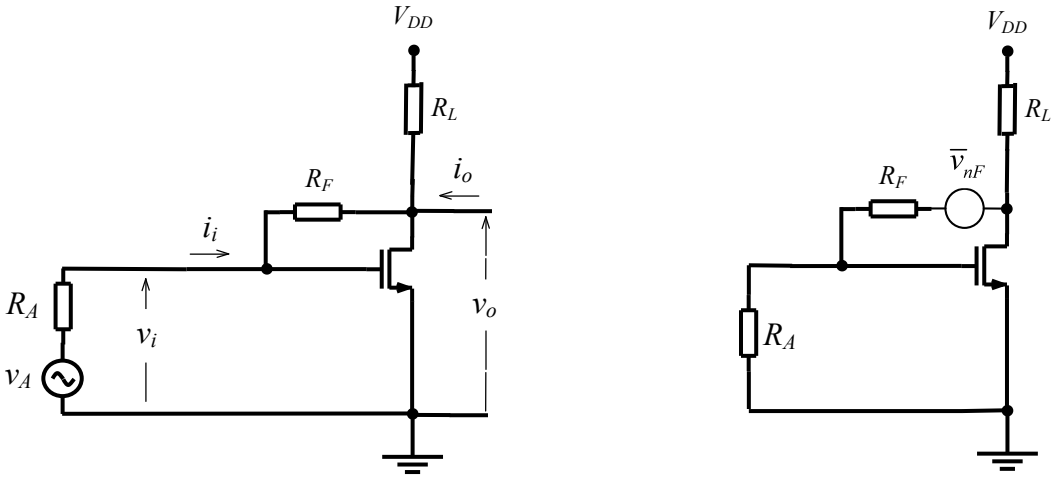
Now the noise factor of a common gate amplifier can be written as

$$F = 1+\frac{P_{n-cho}+P_{n-RL}}{P_{n-Ao}} = 1+\frac{\delta^2(4kTB\gamma\, g_m R_L)+4kTB}{kTBg_m R_L}$$
$$F = 1+4\left(\delta^2\gamma+\frac{1}{g_m R_L}\right) = 1+4\left(\delta^2\gamma+\frac{1}{|A_v|}\right) \qquad (4.158)$$

As an example for R_A = 50 ohm, g_m = 20 mS, R_L = 500 ohm, r_{ds} = 1 kohm and γ = 0.7 the noise factor is F = 1.83 that corresponds to a noise figure of NF = 2.6 dB

4.4.7.2. Parallel voltage feedback amplifier as wide-band LNA

A resistance loaded common source amplifier, with a parallel current feedback from the output voltage, which is a trans-impedance amplifier in nature, is shown in Fig.3-a. It is known that low frequency values of the trans-impedance, the voltage gain and the input and output impedances are[3]



(a) (b)

Figure 4.61(a) The principal circuit diagram of a self-biased common source feedback amplifier. (b) Schematic to calculate the effect of the noise of R_F.

$$Z_m(0) = \frac{v_o}{i_i} = -R_L \frac{g_m R_F - 1}{g_m R_L + 1} \cong -R_F \tag{4.159}$$

$$A_v(0) = \frac{v_o}{v_i} = \frac{Z_m(0)}{r_i} \cong -R_F g_m \tag{4.160}$$

$$A_{vA}(0) = \frac{v_o}{v_A} = \frac{r_i}{(r_i + R_A)} A_v(0) \tag{4.160-a}$$

$$Z_i(0) = r_i = \frac{v_i}{i_i} = \frac{R_F + r_p}{1 + g_m r_p} \cong \frac{1}{g_m} \tag{4.161}$$

$$Z_o(0) = r_o = \frac{v_o}{i_o} = \frac{r_p}{1 + g_m r_p} \cong \frac{1}{g_m} \tag{4.162}$$

where r_p is the parallel equivalent of R_L and r_{ds} . These expressions can be approximated as mentioned, only if g_m, R_F and r_{ds} are sufficiently high.

The input matching condition can be written for $r_p \cong R_L$ from (4.161) as

$$R_A = \frac{R_F + R_L}{1 + g_m R_L} \tag{4.163}$$

[3] Effects of the reactive components and parasitics will be discussed later on.

and with (4.163) , (4.159) and (4.160) can be arranged as

$$|Z_m| = (R_F - R_A) \tag{4.164}$$

$$|A_v| = \frac{(R_F - R_A)}{R_A} \ , \qquad |A_{vA}| = \frac{1}{2}\frac{(R_F - R_A)}{R_A} \tag{4.165}$$

Problem 4.11.

Derive expression (4.164).

The noisy components in this circuit are the internal resistance of the input signal source, R_A, the MOS transistor, the load resistor, R_L, and the feedback resistor, R_F.

The contributions of these noise components to the output noise are as follows:

a) The equivalent noise voltage of the signal source internal resistance, v_{nA} is transferred to the input of the amplifier as

$$v_{nAi} = v_{nA}\frac{R_A}{R_A + r_i} \tag{4.166}$$

where r_i is the input resistance of the amplifier. Provided that the input is matched (i.e. $R_A = r_i$, the resulting output noise voltage signal

$$v_{nAo} = \frac{v_{nA}}{2} \times A_v$$

its RMS value

$$\overline{v}_{nAo} = \frac{\overline{v}_{nA}}{2}|A_v| \tag{4.167}$$

and the corresponding noise power at the output

$$P_{nAo} = \frac{\overline{v}^2_{nAo}}{R_L} = \overline{v}^2_{nA}\frac{1}{4}\frac{|A_v|^2}{R_L}$$

Since $\overline{v}_{nA} = \sqrt{4kTR_A}$

$$P_{nAo} = kT\frac{R_A}{R_L}|A_v|^2 \tag{4.168}$$

b) The output noise power component related to the channel noise current of the transistor is

$$P_{n-cho} = \overline{i}^2_{n-ch}R_L = 4kT\gamma g_m R_L \tag{4.169}$$

c) The noise power of the load resistor R_L itself is simply

$$P_{nLo} = 4kT \tag{4.170}$$

d) The contribution of R_F on the output noise is two-fold; owing to the noise of itself and the negative feedback effect over R_F.

Noise of R_F is represented with a noise voltage source, $\overline{v}_{nF}$ in Fig. 4.61(b). This source provokes a noise current along R_L, R_F and R_A:

$$\overline{i}_{nF} = \frac{\overline{v}_{nF}}{(R_L^{'} + R_F + R_A)} \tag{4.171}$$

where $R_L^{'} = R_L // r_{ds} \cong R_L$.

The contribution of this current on the output noise power can be calculated as

$$\begin{aligned} P_{nFo} = \overline{i}_{nF}^2 R_L &= \left[\frac{\overline{v}_{nF}}{(R_L^{'} + R_F + R_A)}\right]^2 R_L \\ &\cong 4kTR_F \frac{R_L}{(R_L + R_F + R_A)^2} \end{aligned} \tag{4.172}$$

Hence the total noise power dissipating on the load resistor owing to the noisy components of the amplifier becomes

$$\begin{aligned} P_{no} &= P_{n-cho} + P_{nFo} + P_{nL} \\ &= 4kT\left(\gamma g_m R_L + \frac{R_L R_F}{(R_L + R_F + R_A)^2} + 1\right) \end{aligned} \tag{4.173}$$

that corresponds to an RMS output noise voltage of

$$\overline{v}_{no} = \sqrt{P_{no} R_L} \tag{4.174}$$

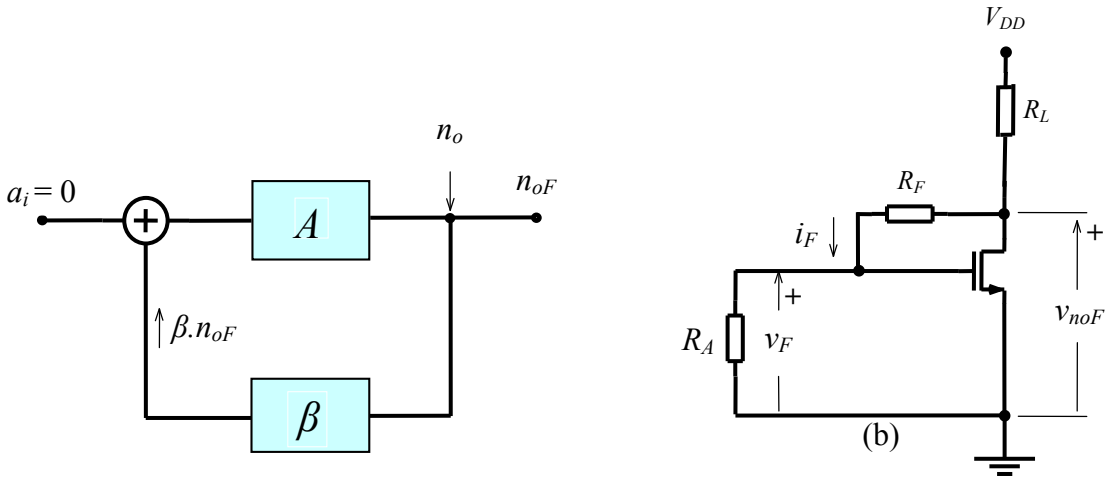


Figure 4.62(a). The block diagram of a feedback amplifier with the output noise feedback. (b) Application to the parallel voltage feedback amplifier.

The noise feedback effect of a negative feedback amplifier can be modelled using the block diagram shown in Fig. 4.62(a), which is applicaple to all single-loop feedback amplifiers. The input signal (a_i) is assumed to be zero. The noise signal at

the output node of the amplifier originating from the components of the amplifier is shown as n_o. The total noise output signal n_{oF} is the sum of n_o and the feed-back noise signal:

$$n_{oF} = n_o + \beta A \times n_{oF}$$

that yields

$$n_{oF} = \frac{n_o}{(1 - \beta A)}$$

This expression shows that if either β or A is negative (i.e. the feedback is negative) the noise signal at the output node becomes $(1 - \beta A)$ times smaller than the original noise.

For the amplifier shown in Fig. 4.62(b) the voltage feedback factor and the voltage gain are

$$\beta = \frac{v_F}{v_{noF}} = \frac{R_A}{R_F + R_A} \quad , \qquad A_v = -\frac{|Z_m|}{r_i} = -\frac{|Z_m|}{R_A} \tag{4.175}$$

$$v_{noF} = v_{no} \frac{1}{1 + \beta \dfrac{|Z_m|}{R_A}} = \frac{1}{1 + \dfrac{(R_F - R_A)}{(R_F + R_A)}} \tag{4.176}$$

$$\delta = \frac{v_{noF}}{v_{no}} = \frac{1}{1 + \dfrac{(R_F - R_A)}{(R_F + R_A)}} = \frac{(R_F + R_A)}{2R_F} \tag{4.177}$$

where δ is the output noise voltage reduction factor owing to the feedback and is always smaller than unity. The corresponding noise power reduction factor is δ^2 . Hence the output noise power and the noise factor with feedback become

$$P_{noF} = \delta^2 \times P_{no} \tag{4.178}$$

$$F \cong 1 + \frac{P_{noF}}{P_{nAo}} = 1 + \frac{4\delta^2 \left(\gamma g_m R_L + \dfrac{R_L R_F}{(R_L + R_F + R_A)^2} + 1 \right)}{\dfrac{R_A}{R_L} |A_v|^2} \tag{4.179}$$

Note that the noise factor increases with g_m, strongly increases with R_L and decreases with gain.

Now a design flow for an input matched self biasing parallel voltage feedback amplifier can be defined using (4.164), (4.165) and the D.C. operating conditions of the transistor:

The basic D.C. condition for the circuit is

$$V_{DS} = V_{GS} = V_{DD} - I_D R_L \tag{4.180}$$

The drain current for a non-velocity saturated transistor

$$I_D \cong \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS}-V_T)^2 = \frac{1}{2}g_m(V_{GS}-V_T) \tag{4.181}$$

and for a velocity saturated transistor

$$I_D \cong kC_{ox}W(V_{GS}-V_T) = g_m(V_{GS}-V_T) \tag{4.182}$$

Since the amplifier to be designed is a wide-band circuit, a velocity-saturated (small geometry) transistor must be preferred to extend the cut-off frequency. Therefore the design flow must be based on (4.164). These expressions lead to

$$R_F = \left(|A_v|+1\right)R_A \tag{4.183}$$

$$g_m = \frac{1}{R_L}\left(\frac{R_F+R_L-R_A}{R_A}\right) \tag{4.184}$$

and

$$I_D = \frac{(V_{DD}-V_T)}{R_L+\dfrac{1}{g_m}} \tag{4.185}$$

(4.183) directly gives the value of R_F corresponding to any source resistance and gain. (4.184) and (4.185) help to calculate the transconductance and the drain D.C. current corresponding to any anticipated load resistor that determines the -3dB frequency together with the load capacitance and the output node parasitics.

On the other hand, from (4.179) it can be seen that the noise factor increases linearly with g_m, quadratically with R_L and decreases quadratically with A_v . Moreover, the power consumption linearly decreases with the increase of the load resistor. The bandwidth depends on the load resistance and the transistor geometry that affects the corner frequencies of the output as well as the input node. Therefore, there is a trade-off among noise, power consumption and bandwidth.

Example 4.11.

An input matched wide band LNA as shown in Fig. (4.61-a) will be designed. 0.18 micron UMC CMOS technology will be used where L =0.18 μm, V_T = 0.3V, C_{ox} = 8.2×10^{-7} F/cm^2 and V_{DD} = 2V. The internal resistance of the input signal source is R_A = 50 ohm and the load capacitance is 100 fF. The required voltage gain from the source is 10 dB ($|A_v| = 3.2$), which corresponds to a voltage gain from the input node of 16 dB ($|A_v| = 6.4$). The -3dB frequency and the noise figure at 1 GHz must be higher then 3 GHz and 3 dB, respectively. It will be assumed that the transistor is operating in the velocity saturated mode, that must be checked at the end of the design. The r_{ds} of the transistor will be assumed considerably higher than the drain load resistance.

(4.165) imposes the value of the feedback resistors

$$R_F = \left(|A_v| + 1\right) R_A = 370 \text{ ohm}$$

The g_m and I_D values calculated from (4.184) and (4.185), and NF from (4.179) corresponding to different R_L values are given in the table below. The -3 dB frequencies obtained from the SPICE simulations are also given. From this table it can be seen that R_L = 200 ohm is the appropriate choice. The noise figure can be decreased to smaller values to the expense of a higher D.C. power consumption and higher transistor widths that impairs the band width.

R_L (ohm)	g_m (mS)	I_D (mA)	NF (dB)	BW (GHz) (simulation)
100	84	15	1.55	3.25
150	62.7	10.2	2.33	3.75
200	52	7.75	2.8	3.83
250	45.6	6.25	3.2	3.85
300	41.3	5.28	4.5	3.70

In Fig.4.63 the SPICE simulation results corresponding to R_L = 200 ohm is shown. The width of the transistor is optimized to obtain a good input matching, i.e. $r_i = R_A$ = 50 ohm. From these results it can be seen that;

- The voltage gain is 3.17, very close to the target value.
- The bandwidth is 3.83 GHz.
- The noise reduction factor (δ) and the noise factor calculated from (4.177) and (4.179) with these circuit parameters found as δ = 0.567 and $F \cong 1.91$ that corresponds to $NF = 2.8$ dB.

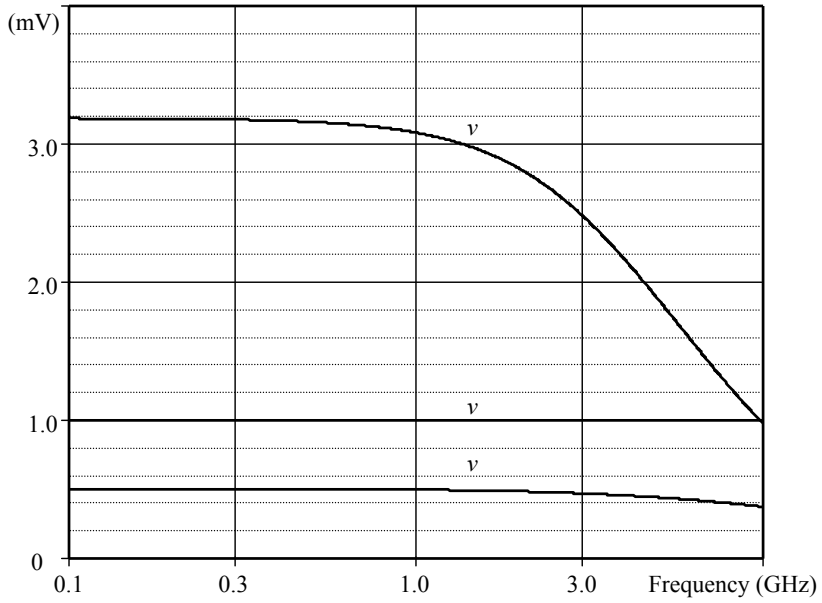


Figure 4.63, Simulation results for R_F = 370 ohm and R_L = 200 ohm.

- The input matching is maintained perfectly up to 1 GHz and reasonably up to 3 GHz. The slight decrease of v_{in} at higher frequencies indicate a phase shift due to the input capacitance that impairs the noise feedback and results in a frequency dependent increase of δ and consequent increase of the noise figure.

To proof the calculations about the noise reduction effect of the feedback a simulation was performed emulating the total noise current originating from the amplifier with a sinusoidal 1 μA current source in parallel to the load and the total output noise voltage simulated for $R_A = 0$ (that corresponds to no feedback) and $R_A =$ 50 ohm (that corresponds to the case of feedback). The corresponding noise voltages at the output shown in Fig. 4.64 indicates a 0.57 noise voltage reduction owing to the feedback that is in a very good agreement with the calculated value.

There is an obvious drawback of the self biased amplifier shown in Fig. 4.61; the position of the D.C. operating point. Since $V_{DS} = V_{GS}$, the negative swing range of the output voltage is smaller than the positive swing range. This asymmetric and limited output dynamic range impairs the linearity.

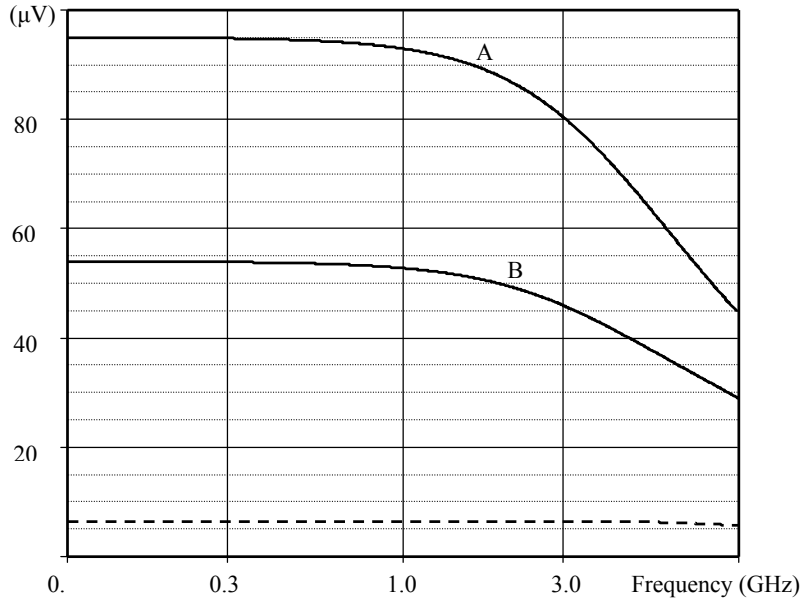


Figure 4.64. Simulation results showing the output noise voltage (A) feedback effect eliminated, (B) with feedback for a 1μA output noise current. The dotted curve shows the feedback voltage on R_A.

The symmetrical version of this circuit shown in Fig. 4.65 is an effective solution to increase the symmetrical output dynamic range. This circuit is nothing but a CMOS inverter. The rail-to-rail symmetrical output swing capability of the circuit guarantees a very high linearity around the operating point, situated in the middle of the output voltage swing range. The small signal equivalent of this circuit is exactly the same as the circuit given in Fig. 4.65, where g_m and r_{ds} are the sum of the transconductances and internal resistances of M1 and M2 and all expressions derived for the original circuit are valid for the symmetrical version (See Part 2.2).

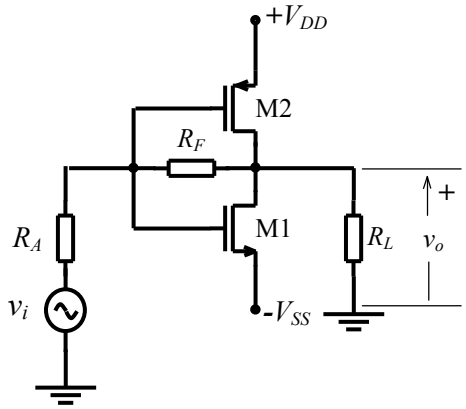


Figure 4.65. Symmetrical version of the parallel voltage feedback amplifier.

4.4.7.3. Noise cancelletion in wide-band amplifiers

Noise cancellation, in a broader sense, intends to obtain a negative replica of the noise signal at the output of a system and add to the original output signal. Since the total signal at the output is the sum of the intentional output signal and the non-intentional output noise, the generated negative replica cancels out the noise at the output.

This concept is applied to reduce the noise of a wide-band amplifier by F. Bruccoleri et.al.[4] The amplifier of which the output noise is intended to be cancelled is a self-biased common source feedback amplifier. The circuit is re-drawn with the cancellation mechanism in Fig. 4.66. From 4.4.7.2 we know that the v_o output voltage is composed of two components; the normal output signal which is equal to ($v_i \times A_v$) and the noise voltage signal at the output, v_{no}. A replica of this noise voltage, that is divided from v_{no} by R_F and R_A appears at the input node:

$$v_{noi} = v_{no} \frac{R_A}{R_A + R_F}$$

Note that although the noise voltages at the input and output nodes changes in parallel in time, the original signal voltage at the output is in opposite phase with the signal at the input node.

The voltage gain (a_{v2}) of the amplifier marked with A2 in Fig.4.66 is a positive number and low in magnitude, that can be smaller or larger than or equal to unity. Now it can be seen that if the voltage gain of A3 is negative and equal to

$$A_{v3} = -\left(\frac{R_A + R_F}{R_A} \times a_{v2} \right) \tag{4.186}$$

the noise voltages reaching to the summing node becomes equal in magnitude but opposite in sign, therefore cancel out each other.

$$v_{noNC} = v_{no} \left(a_{v2} + \frac{R_A}{R_A + R_F} A_{v3} \right) = 0 \tag{4.187}$$

[4] F. Bruccoleri, E. A. M. Klumpering, B. Nauta, " Wide-Band CMOS Low-Noise Amplifier Exploiting Thermal Noise Cancelling", IEEE JSSC, Feb. 2004, pp. 275-282.

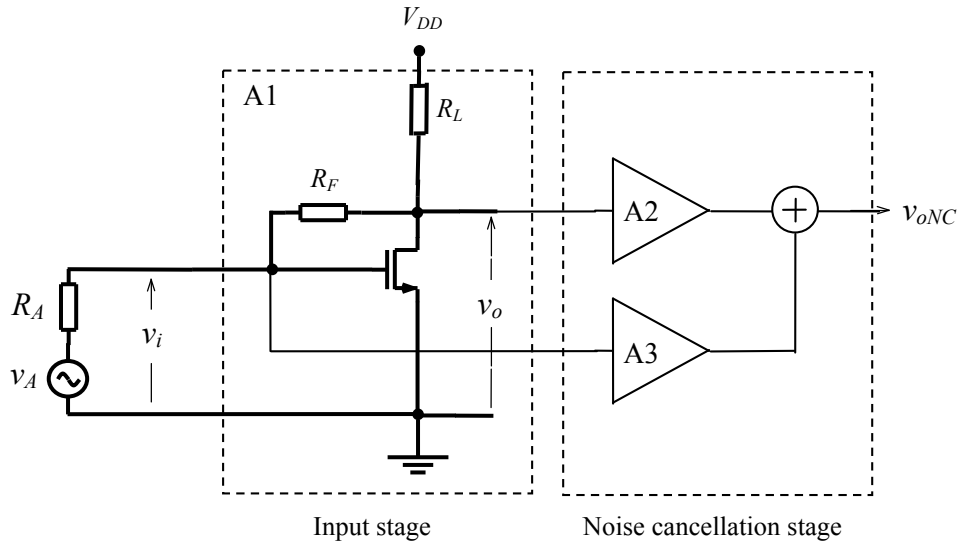


Figure 4.66. Principal circuit diagram of a wide-band LNA with noise cancellation feature.

On the other hand, the signal voltages reaching to the summing point are in-phase and the summed noise compansated output voltage becomes

$$v_{oNC} = v_i(A_{v1}a_{v2} + A_{v3}) \tag{4.188}$$

that is almost twice as high as the voltage at the output of A1.

It must be noted that there are two facts affecting the noise cancellation advantage of the approach:

- For a perfect cancellation of the output noise of A1, the delay (or phase) characteristics of A2 and A3 must be identical along the bandwidth of the amplifier.
- The noises of A2 and A3 are out of the cancellation process and appear at the output of the summing circuit.

Example 4.12.

The circuit diagram of a noise cancelled wide-band LNA is designed with UMC 018 technology is given in Fig. 4.67. M1 is the feedback amplifier analyzed in Example 4.11 to provide a low input impedance for matching. M3 is a common source amplifier to provide the necessary voltage gain from the input node to the summing node. M2 is a grounded gate amplifier to provide a positive, low voltage gain. R_{L3} is shared by M2 and M3 and serves to sum the output voltages of M2 and M3. Since the voltage gain of M2 is low (around unity) it is a low transconductance, low current and relatively high input resistance circuit. The gate bias voltage of M2 helps to fine-tune the gain of this stage to obtain a perfect cancellation and minimum noise factor. The simulation results for the voltage gain of the amplifier from v_i is 10.66 (20.5 dB), the bandwidth 2.25 GHz and the power consumption is 25.2 mW.

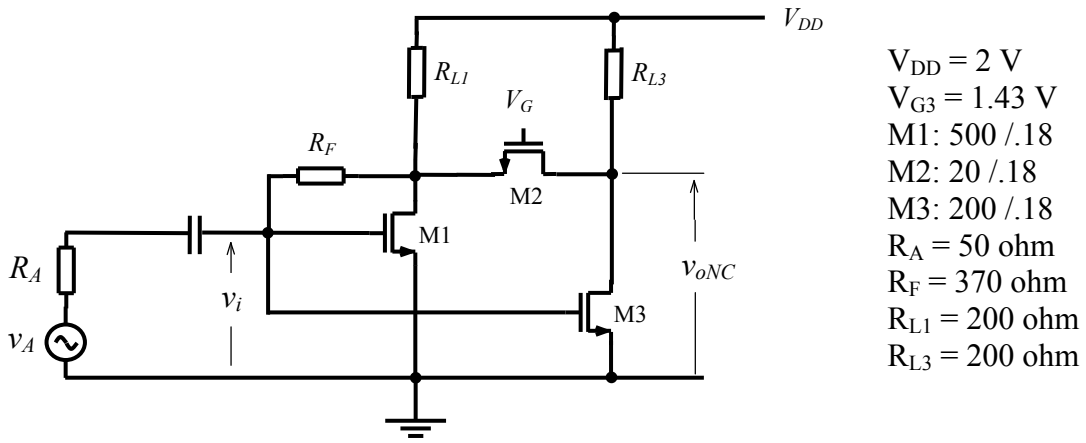


Figure 4.67. The circuit diagram of the wide-band LNA with noise cancellation feature.

The results of a SPICE simulation to observe the noise cancellation is given in Fig. 4.68. For this purpose the total noise current generated in A1 is emulated with a 1μA, 100 MHz sinusoidal current. (a) is the noise voltage at the output of M1 while (c) is the noise voltage at the output of the circuit that indicates a perfect noise cancellation.

But it can be seen that the cancellation process is very sensitive of the bias voltage (and gain) of M2 and permits a spread of the bias voltage in the order of only few tens of millivolts.

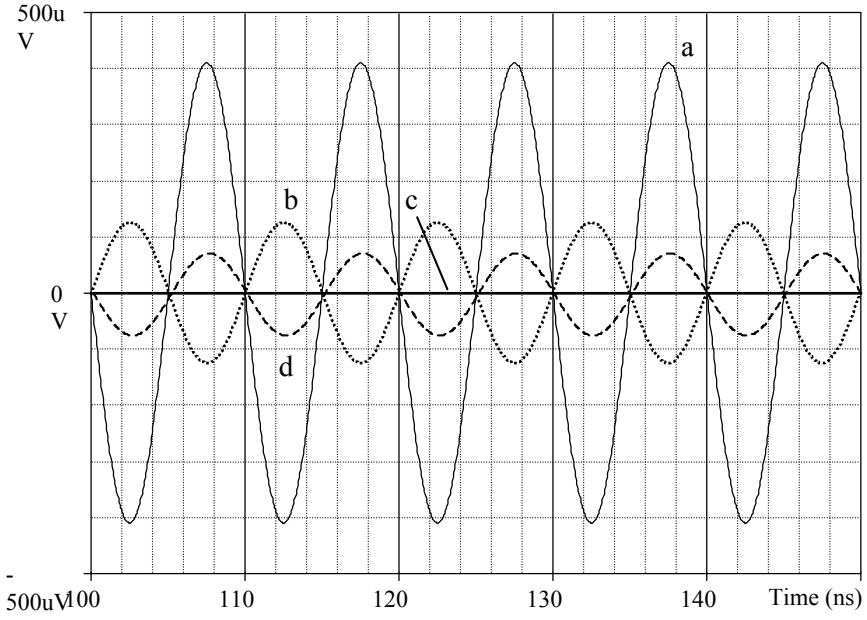


Figure 4.68. (a) The emulated noise voltage at the output of M1, corresponding to a 1 μA noise current on R_{L1}. (b) The noise voltage at the output of the amplifier for V_{GS2} = 1.335 V (the phase relation with (a) indicates an unsatisfactory gain of the A1-A2 chain. (c) The noise voltage at the output of the amplifier for V_{GS2} = 1.435 V that corresponds to a perfect noise cancellation. (d) Corresponds to V_{GS2} = 1.535 V. Note the phase reversal owing to the over- increased gain of M2.

The simulation results given in Fig. 4.69 shows the variations of the noise voltage at the output of M1, at the input of M1 and at the output of the amplifier, corresponding to a 1 μA sinusoidal noise current parallel to R_{L1}. As seen from curve (c) the noise at the output is fully cancelled out along the frequency band of the amplifier. This indicates that the signal delays of M2 and M3 are matched. The slight increase of the noise at the high end of the band indicates increased discrepency of the delays with frequency.

As mentioned before, the cancellation process cancels out the noise component at the output port originating from M1. The noises of M2 and M3 appear at the output and determine the noise figure of the amplifier.

Now let us calculate the noise originating from M2 and M3 for this example and find the *NF* of the amplifier. The transconductances of M2 and M3 are 3.37 mS and 31.47 mS, respectively and they share the same load resistor, R_{L3}. The total noise power at the output originating from these components is

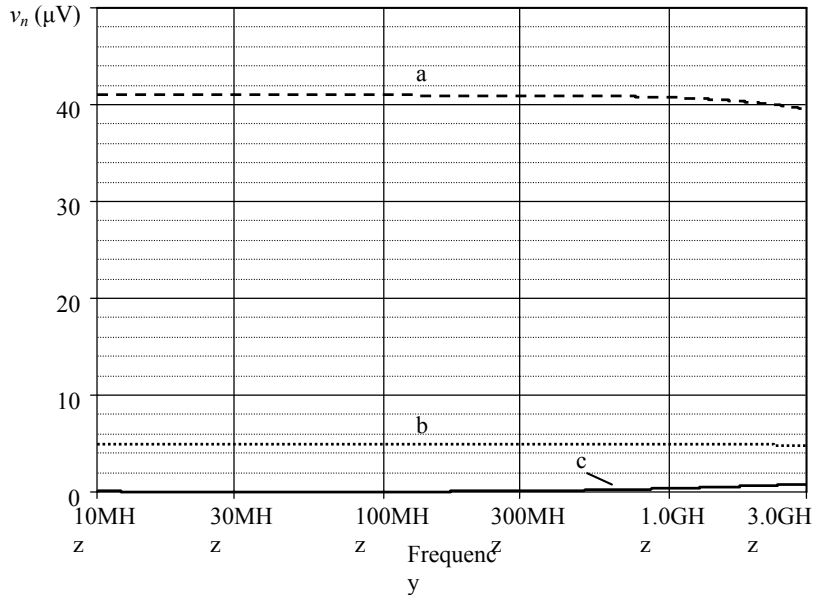


Figure 4.69. Variation of the emulated noise originaring from the first stage: (a) at the output of M1, (b) at the input of M1 fed-back over R_F , (c) the cancelled noise at the output of the amplifier.

$$P_{no2,3} = 4kT\gamma(g_{m2} + g_{m3})R_L + 4kT$$

The noise voltage at the output owing to the signal source;

$$v_{nAo} = \frac{1}{2}v_{nA}(A_{v1} \cdot a_{v2}) = \frac{1}{2}v_{nA}A_{v3}$$

The noise power at the output owing to the signal source;

$$P_{nAo} = \frac{v_{nAo}^2}{R_L} = kTA_{v3}^2 \frac{R_A}{R_L}$$

Hence the noise factor becomes

$$F = 1 + \frac{4kT\left(\gamma(g_{m2} + g_{m3})R_{L3} + 1\right)}{kTA_{v3}^2 \frac{R_A}{R_L}} = 1.83$$

that corresponds to NF = 2.6 dB.

These results show that;

- The noise cancellation of the input transistor works effectively.
- In addition, the voltage gain approximately doubles.

But;

- Although the noise of the input stage is cancelled out at the output, the noise of the noise cancellation stage (for the proposed circuit the noises of M2 and M3) adds a noise comparable with the noise of the input transistor. With a good design of the cancellation stage the overall noise can be reduced.
- For the design of the second stage, signal delays of the paths subject to be added have prime importance for wide-band noise cancellation.
- As a more important fact the cancellation process is very sensitive to the operating points and needs fine-tuning.
- Another disadvantage is the increase of power consumption. But the first stage can be designed for lower power consumption and higher inherent noise that is subject to cancellation.