7. Low-Noise Amplifier Design

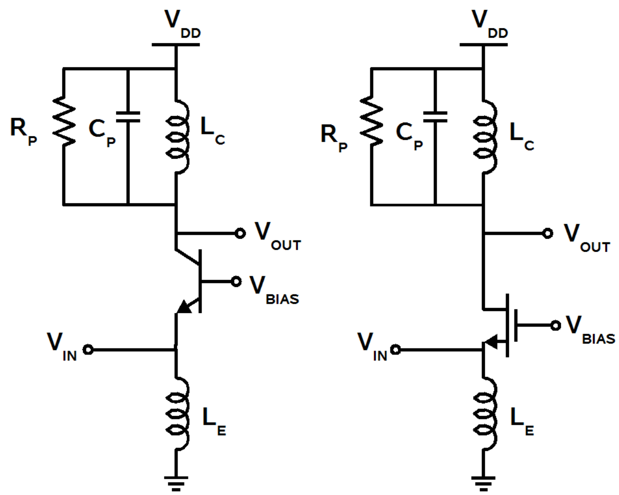
Outline

- Low noise amplifier overview
- Tuned LNA design methodology
- Tuned LNA frequency scaling and porting
- Broadband low noise amplifier design methodology

7.1 LNA overview

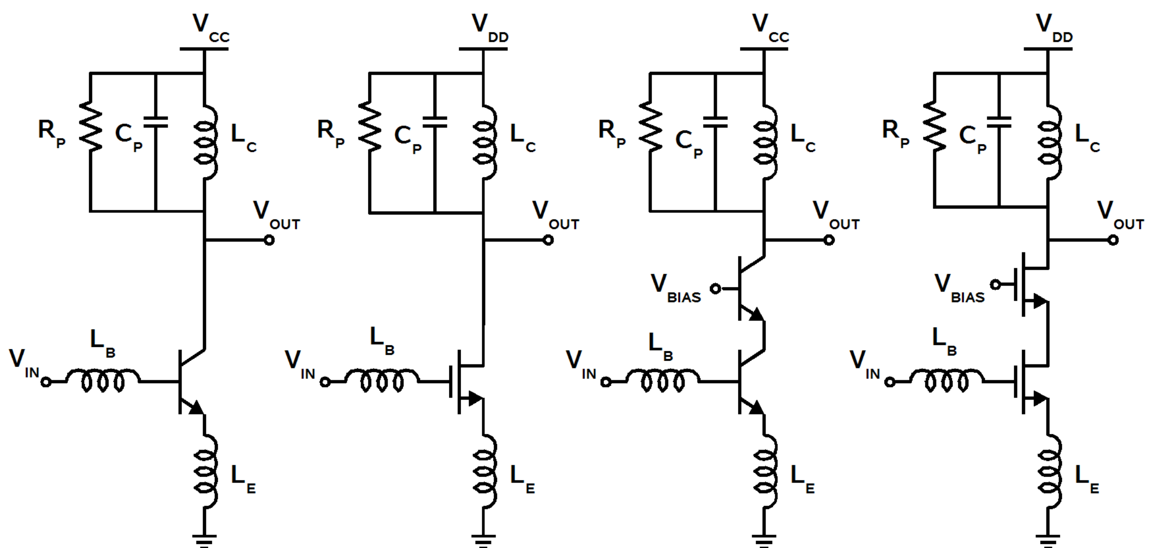
Tuned LNA topologies

CB/CG (no feedback)



Cascode (L or xfmr feedback)

CS/CE (L or xfmr feedback)



Design goal

- Minimize the noise of the amplifier for a given signal source impedance to approach transistor minimum noise figure/factor NF_{MIN}/F_{MIN}

$$F = F_{MIN} + \frac{R_n}{G_s}\left|Y_s - Y_{sopt}\right|^2$$

- Input and output matching to source and load.
- Maximize gain (***G***) and linearity (***IIP3***)
- Reduce DC power P_{DC} => conflict with ***F*** and ***IIP3***

$$FoM_{LNA} = \frac{G \times IIP3 \times f}{(F-1)P_{DC}}$$

Design philosophy

- Take advantage of what silicon does best: transistors.
- Use Si passives only sparingly:
  - Q is fairly low and undermines overall noise figure
  - Inductors are (significantly) larger than transistors, hence expensive.
- Make transistor sizing part of the noise matching step.
- Use only reactive (loss-less) feedback or minimize the noise contribution of resistive feedback components.
- Avoid active loads if at all possible.

LNA design fundamentals

- Device noise fundamentals:
  - $Re\{Z_{sopt}\} <> Re\{Z_{IN}\}$ and $Im\{Z_{sopt}\}$ approx. $Im\ \{Z_{IN}\}$ (within 15%)
  - $Re\{Z_{sopt}\} = k\ f_T/(fg_m)$
  - F_{MIN} is invariant to number of gate fingers N_f, and number of transistors *m* connected in parallel, but depends on W_f.
- Reactive (lossless) feedback does not affect F_{MIN} and $Re\{Z_{sopt}\}$
- Power is dictated by noise impedance matching ($V_{DD} \times J_{OPT} \times f_T / g'_m$)
- Saving power comes with the price of compromising noise and linearity!

Tuned and broadband LNA design philosophy

- Active device for noise impedance
  - Find optimal W_f for given frequency
  - Bias for minimum NF_{MIN} and
  - sizing (N_f) for Re{Z_{sopt}} = 50 Ω

$$\frac{\partial F_{MIN}(W_f)}{\partial W_f} = 0$$

$$\frac{\partial F_{50}(N_f)}{\partial N_f} = 0$$

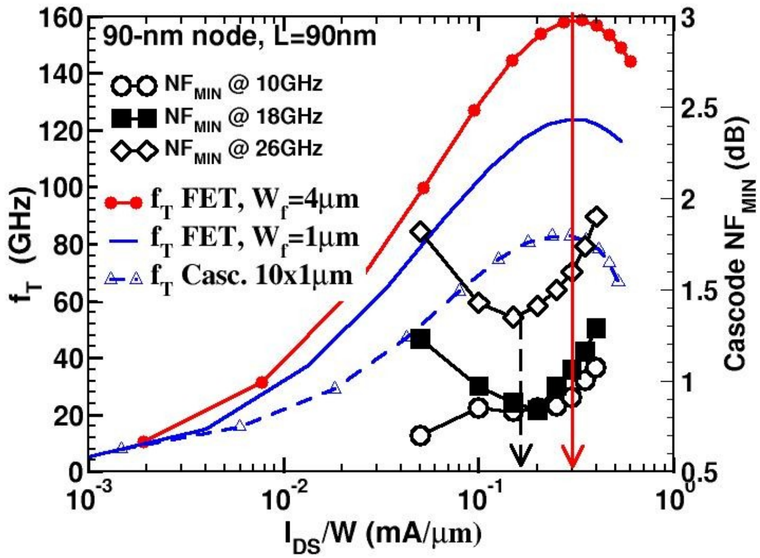
- (lossless) feedback for input impedance matching Z_{IN} and Im{Z_{sopt}}

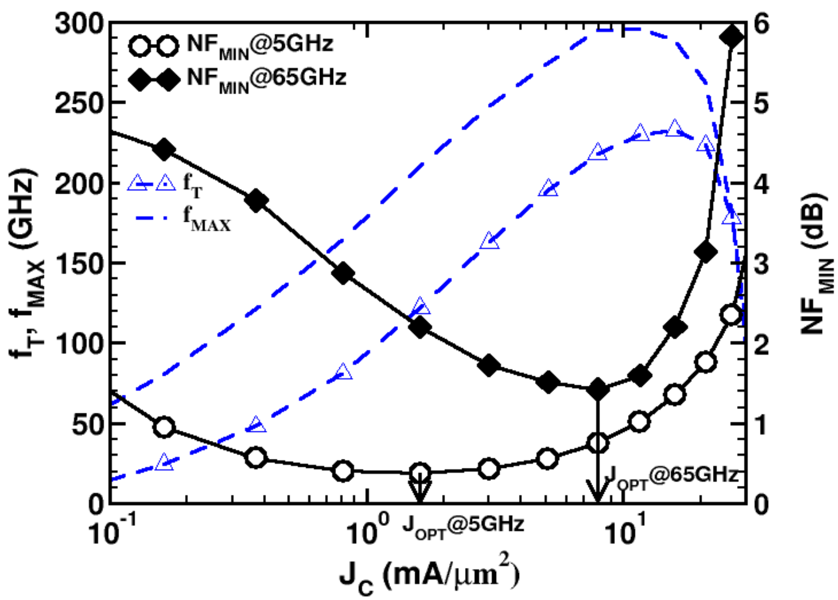
All lossless feedback configurations work:

- Series-series, shunt-series, series-shunt, shunt-shunt

Transimpedance feedback works best for broadband LNAs

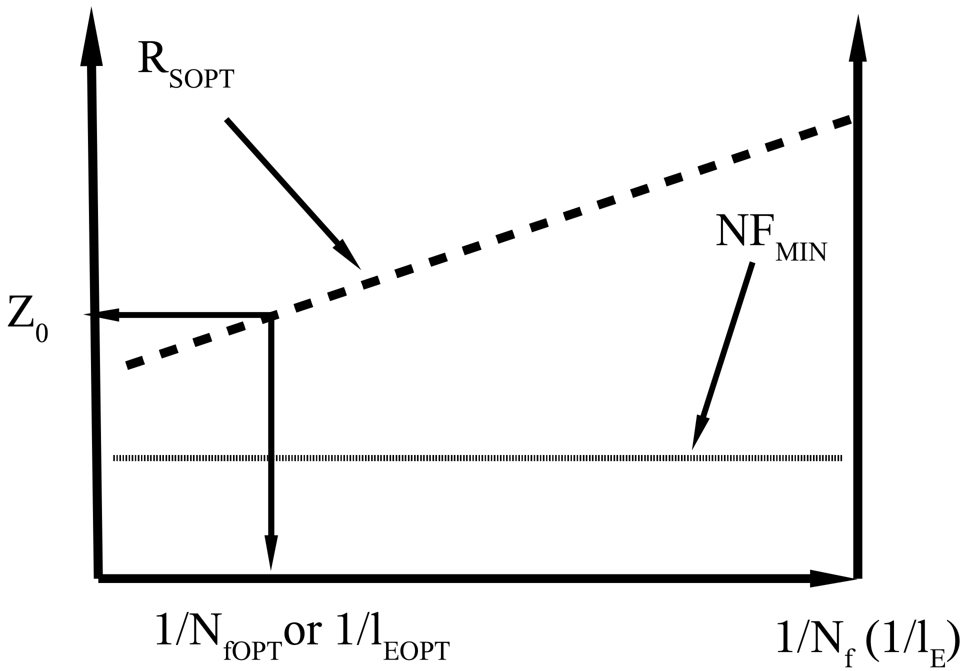
Biasing LNA topology for minimum noise





- MOSFET, cascode J_{OPT} = 0.15 mA/μm irrespective of W_f, node, and frequency
- Lowest current for optimally biased MOS-LNA is 150μA for single 1μm finger
- In HBTs J_{OPT} varies with frequency, topology, and technology node

Sizing the MOSFET/HBT (cascode) for R_{SOPT}



FET/HBT (casc) biased at J_{opt}

Noise parameters scale with $(l_E)N_f$ for fixed W_f.

$$\Re[Z_{sopt}(N_f, f)] = Z_0 \text{ coincides with } \frac{\partial F_{50}(N_f)}{\partial N_f} = 0$$

$$\Re[Z_{sopt}(l_E, f)] = Z_0 \text{ coincides with } \frac{\partial F_{50}(l_E)}{\partial l_E} = 0$$

Sizing the FET (cascode) for R_{SOPT}

$$R_n = \frac{R_{N,FET}}{N_f N} \qquad G_u = G_{N,FET}\,\omega^2 N_f N$$

$$G_{cor} = G_{C,FET}\,\omega N_f N \qquad B_{cor} = B_{FET}\,\omega N_f N$$

$$Y_{sopt} = \sqrt{G_{cor}^2 + \frac{G_u}{R_n}} - jB_{cor} = N N_f W_f \omega \left(\sqrt{G_{C,FET}^2 + \frac{G_{FET}}{R_{FET}}} - j B_{FET} \right)$$

$$Z_{sopt}(\mathrm{FET}) \approx \frac{f_{Teff}}{N \cdot N_f \cdot W_f \cdot f \cdot g'_{meff}} \left[\sqrt{\frac{g'_m \cdot R'_s + W_f \cdot g'_m \cdot R'_g(W_f)}{k_1}} + j \right] = Z_0 + j X_{sopt}$$

$$N N_f = \frac{f_{Teff}}{Z_0 \cdot W_f \cdot f \cdot g'_{meff}} \sqrt{\frac{g'_m \cdot R'_s + W_f \cdot g'_m \cdot R'_g(W_f)}{k_1}}$$

Sizing the HBT (cascode) for R_{SOPT}

$$R_n = \frac{R_{HBT}}{N I_E}$$

$$G_u = G_{HBT}\,\omega^2 N I_E$$

$$G_{cor} = G_{C,HBT}\,\omega N I_E$$

$$B_{cor} = B_{HBT}\,\omega N I_E$$

$$Y_{sopt} = \sqrt{G_{cor}^2 + \frac{G_u}{R_n}} - jB_{cor} = N I_E\,\omega\left(\sqrt{G_{C,HBT}^2 + \frac{G_{HBT}}{R_{HBT}}} - j B_{HBT}\right)$$

$$Z_{sopt}(\mathrm{HBT}) \approx \frac{f_{Teff}}{f \cdot N \cdot I_E \cdot g'_{meff}}\left[\sqrt{\frac{g'_m}{2}(r'_E + R'_b)} + j\right] = Z_0 + jX_{sopt}$$

$$N I_E = \frac{f_{Teff}}{Z_0 \cdot f \cdot g'_{meff}}\sqrt{\frac{g'_m}{2}(r'_E + R'_b)}$$

RF CMOS/HBT LNA design equations

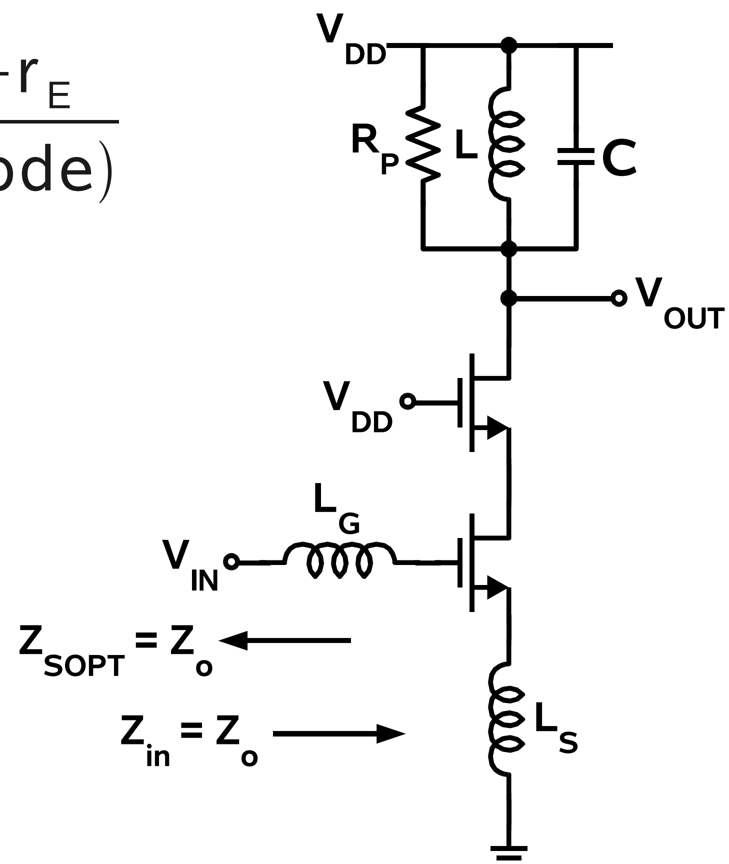
$$\Re\left[Z_{sopt}(N_f(I_E), f)\right] = Z_0 \text{ coincides with } \frac{\partial F_{50}(N_f(I_E))}{\partial N_f(I_E)} = 0$$

$$L_S = \frac{Z_0 - R_s - R_g}{\omega_T(\text{cascode})} \qquad L_S = \frac{Z_0 - R_b - r_E}{\omega_T(\text{cascode})}$$

$$Z_{IN} = \omega_T L_S + R_g + R_s + j\left[\omega(L_S + L_G) - \frac{f_T}{f\, g_m}\right]$$

$$Z_{IN} = \omega_T L_S + R_b + r_E + j\left[\omega(L_S + L_G) - \frac{f_T}{f\, g_m}\right]$$

$$L_G = \frac{f_T}{2\pi f^2 g_m} - L_S \qquad G \le \frac{1}{4} \frac{f_T^2}{f^2} \frac{R_P}{Z_0}$$



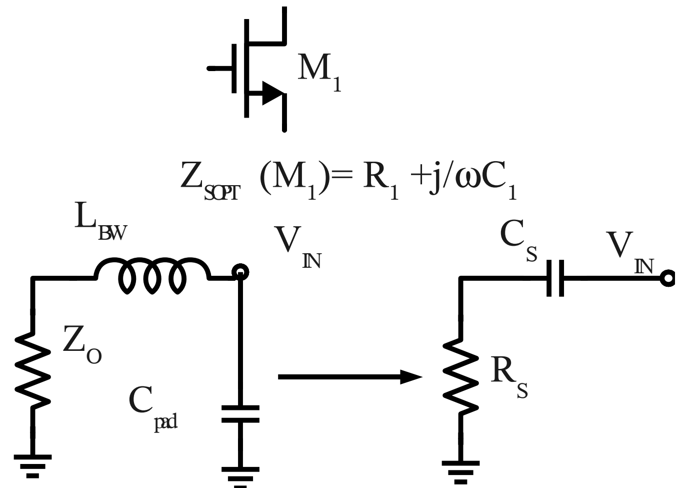
Refinements for mm-waves: S. Nicolson (CSICS-06)
(i) Source Impedance

- With bondwire

$$R_S = n \times Z_0;$$

$$R_s = \frac{Z_0}{(1-\omega^2 L_{BW} C_{PAD}) + \omega^2 Z_0^2 C_{PAD}^2}$$

$$X_s = j\omega \frac{[L_{BW}(1-\omega^2 L_{BW} C_{PAD}) - Z_0^2 C_{PAD}]}{(1-\omega^2 L_{BW} C_{PAD}) + \omega^2 Z_0^2 C_{PAD}^2}$$

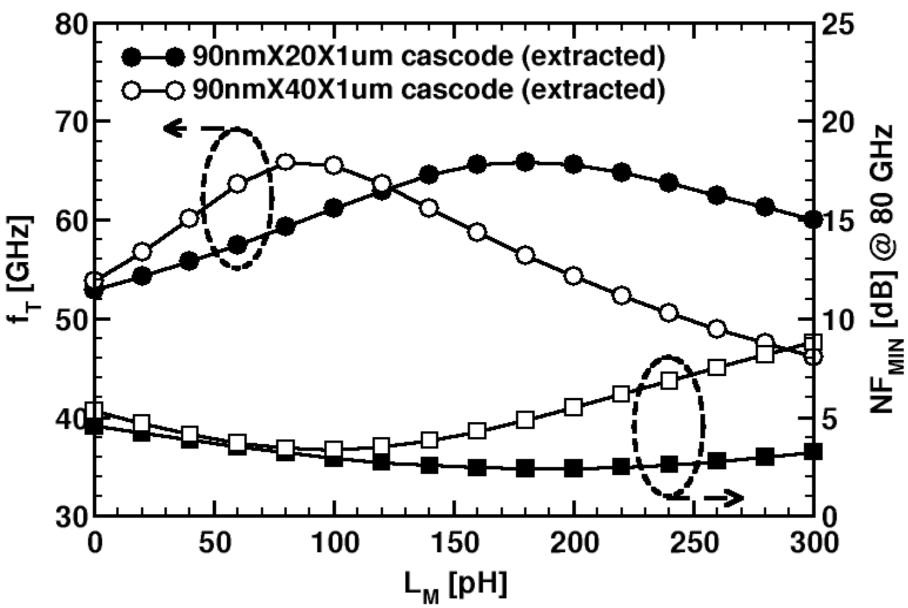


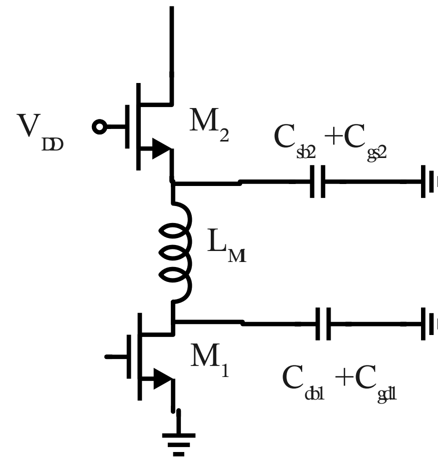
- Without bondwire

$$R_S = \frac{Z_0}{k} \qquad Z_S = \frac{Z_0}{k} - j\frac{\omega C_{PAD} Z_0^2}{k}$$

$$k = 1 + \omega^2 C_{PAD}^2 Z_0^2$$

Refinements for mm-wave CMOS LNAs: (ii) f_T of topology with L_M after extraction





$$f_T(\text{cascode}) = \frac{g_{m1}}{2\pi(C_{gs1} + 2C_{gd1})}$$

L_{M1} forms artificial t-line with parasitics of M_1 and M_2

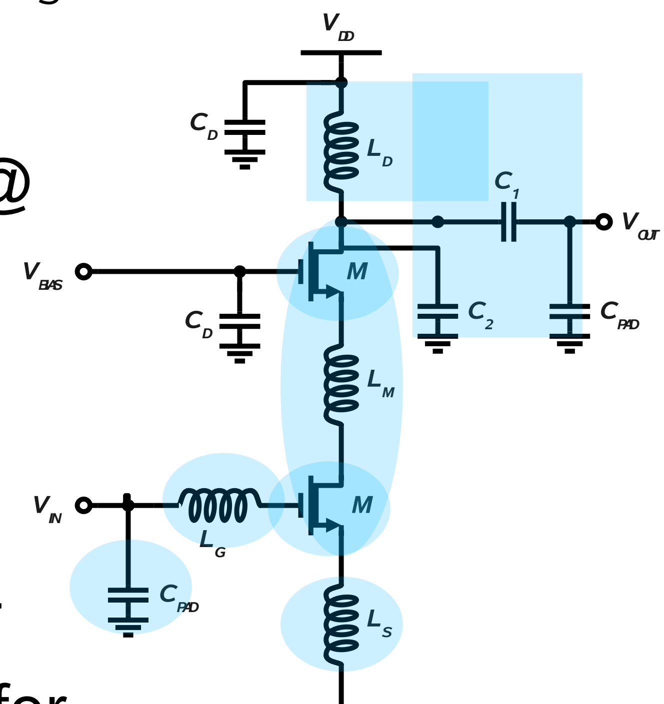
An optimal L_{M1} exists that maximized f_T.

$L_{M1} \sim W_1^{-1}$

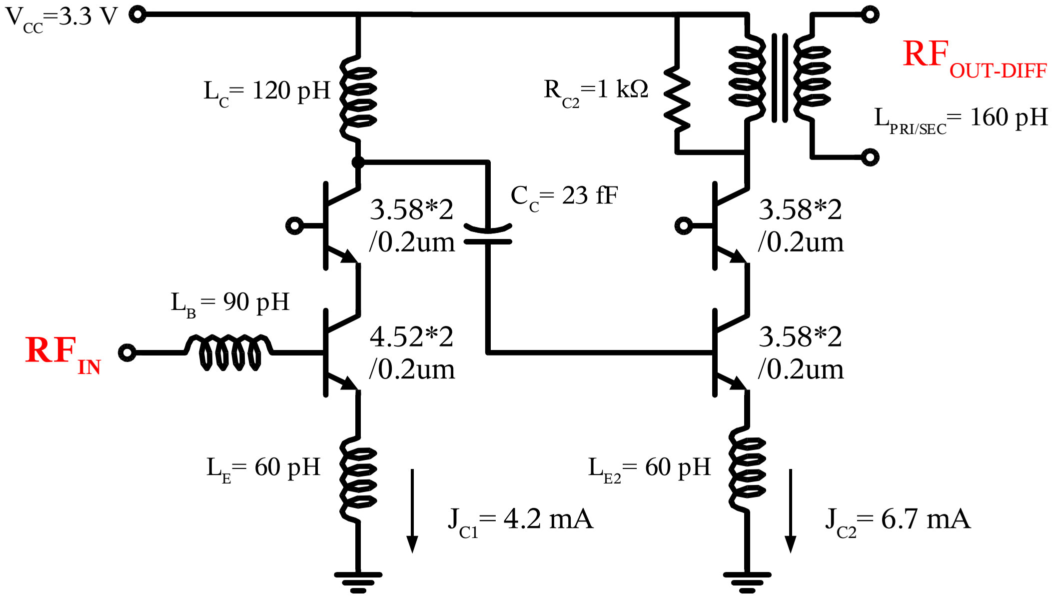
Both the gain and the noise figure are improved

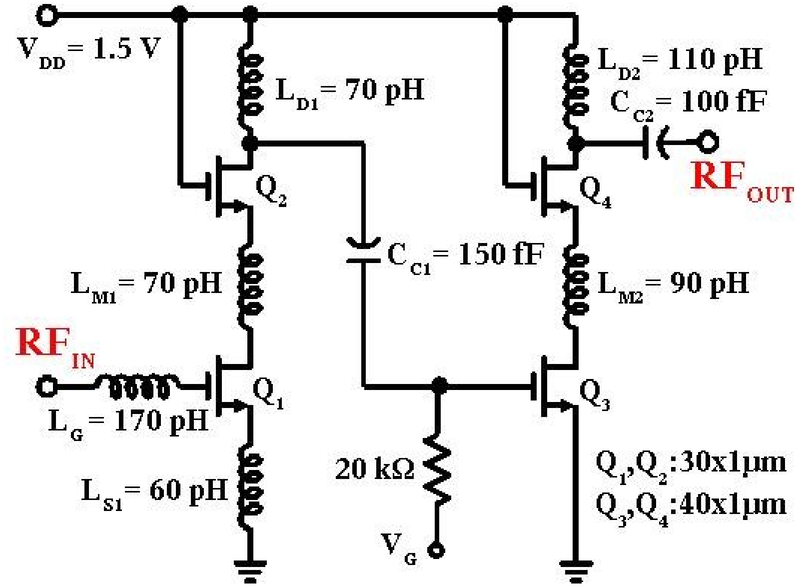
(mm-wave) CMOS/HBT LNA design methodology

- Calculate effective source imp. $Z_S = R + jX_S$
- Find optimal W_f (I_E) and bias at J_{OPT}
- Find L_{M1} which maximizes f_T of topology @ J_{OPT}
- Find N_f such that $R = Re(Z_{SOPT})$ @ J_{OPT}
- Find $L_S = R/\omega_T$ such that $R = Re\{Z_{IN}\}$
- Find L_G such $X_s = Imag\{Z_{IN}\} = Imag\{Z_{SOPT}\}$
- Design output matching network: L_D, C_D for maximum gain

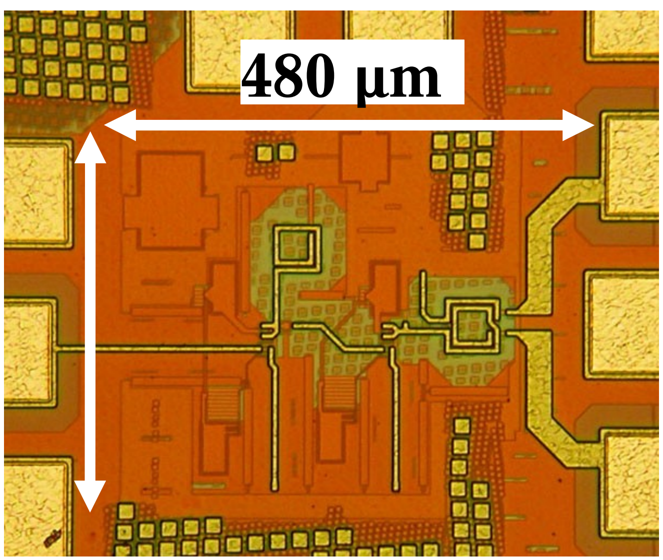


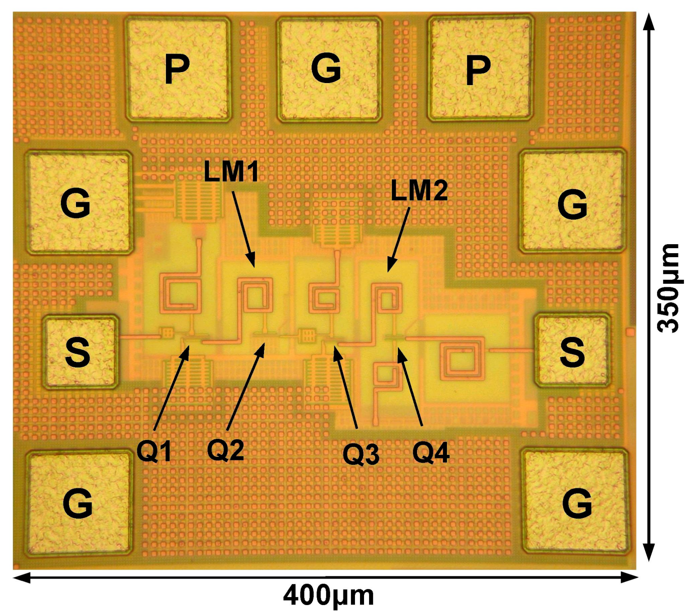
Examples: SiGe HBT vs. 90-nm CMOS Cascode LNAs



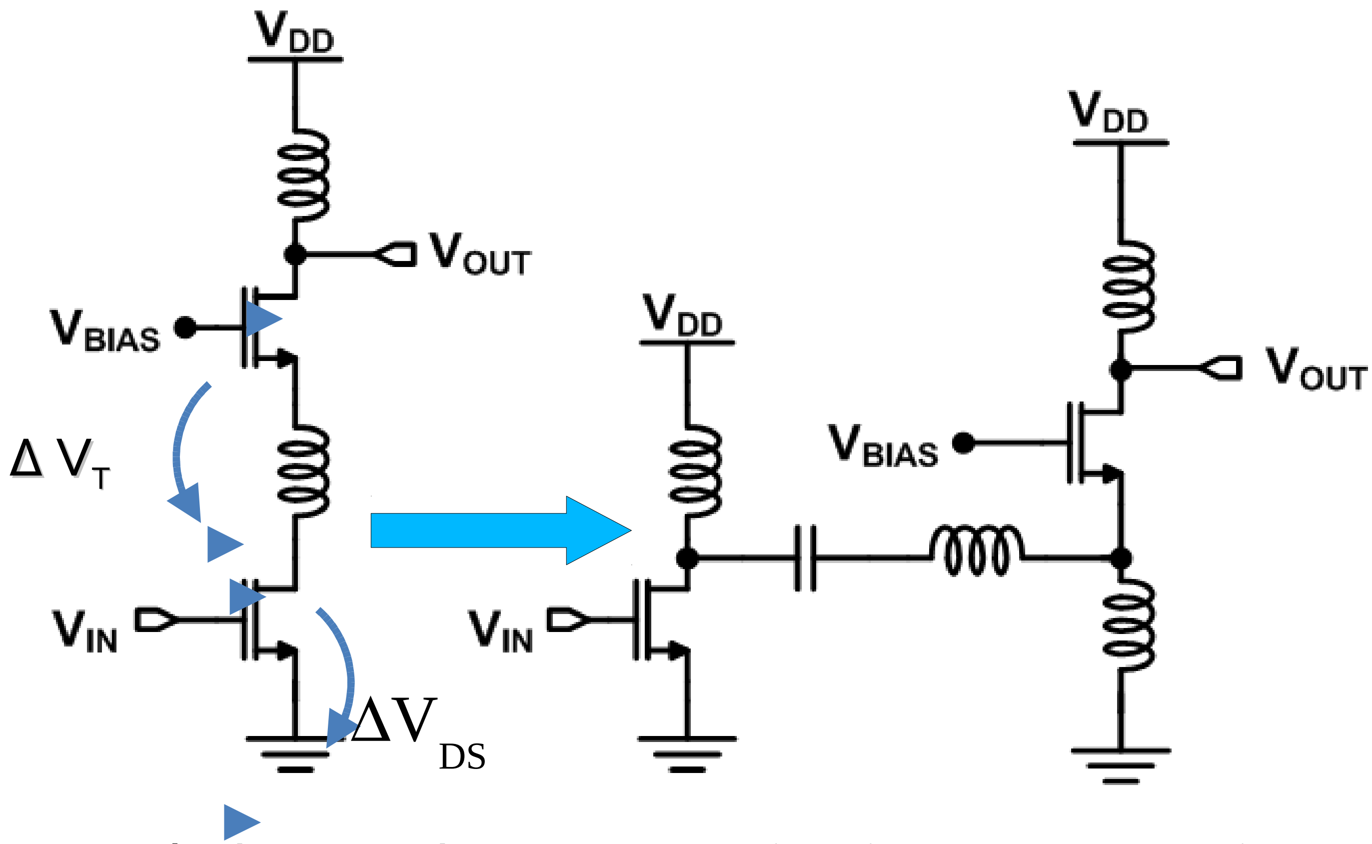


370 μm





Single-Transistor Stack Topologies



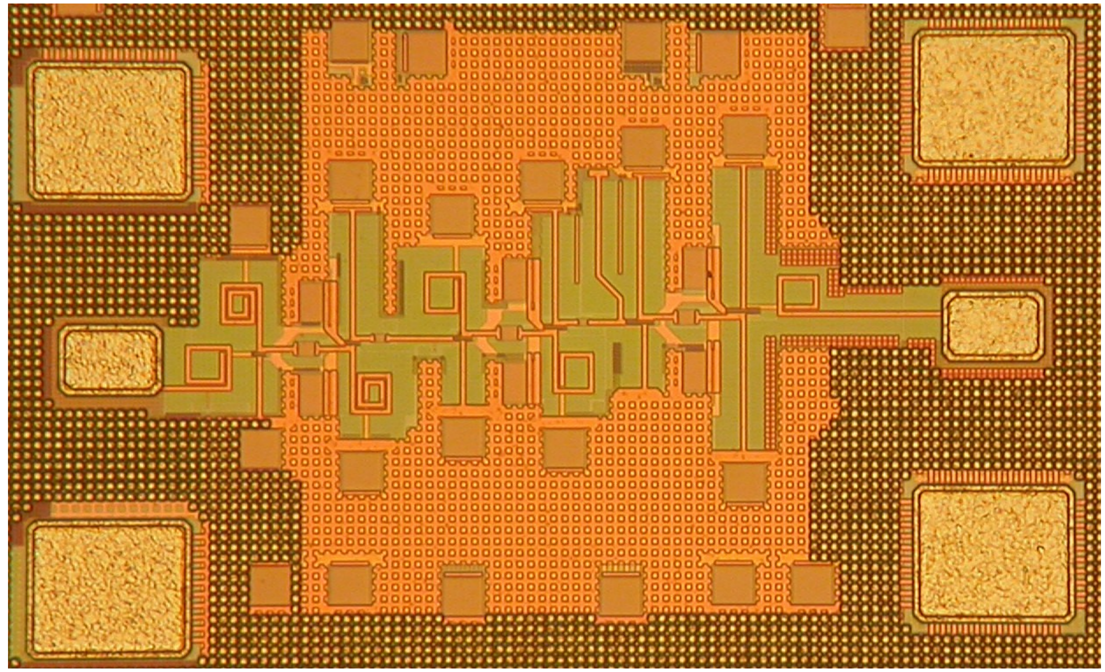
Ac-coupled cascode, 1V operation in GP CMOS, insensitive to V_T, yet:

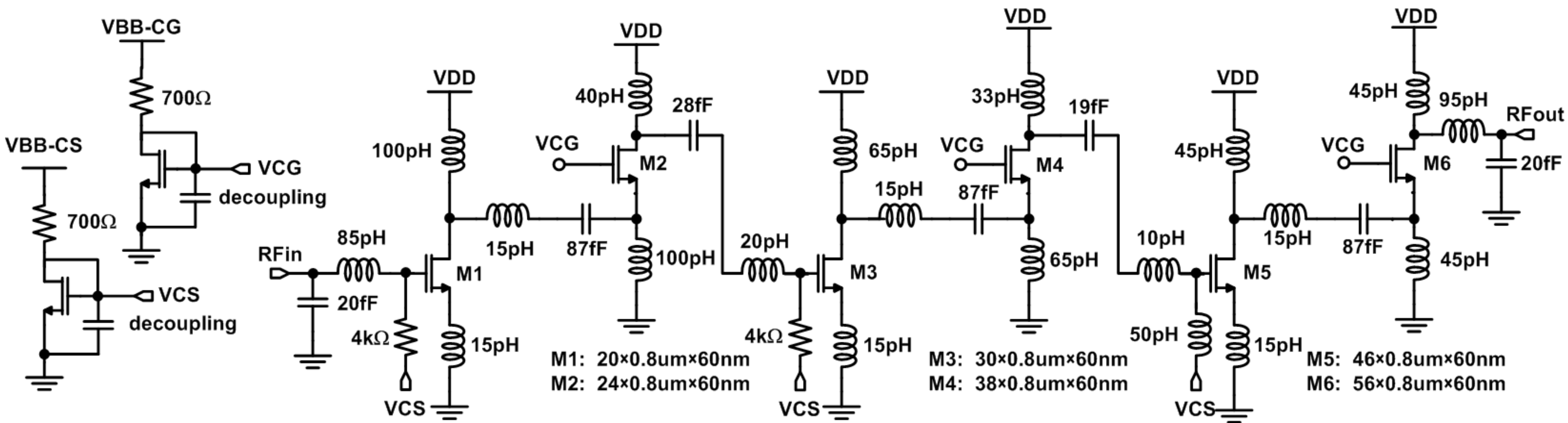
- 2x the DC current
- 2[nd] resonant tank reduces bandwidth,
- extra lossy inductor and MIM cap => higher loss, larger area

140-GHz 65-nm CMOS LNA

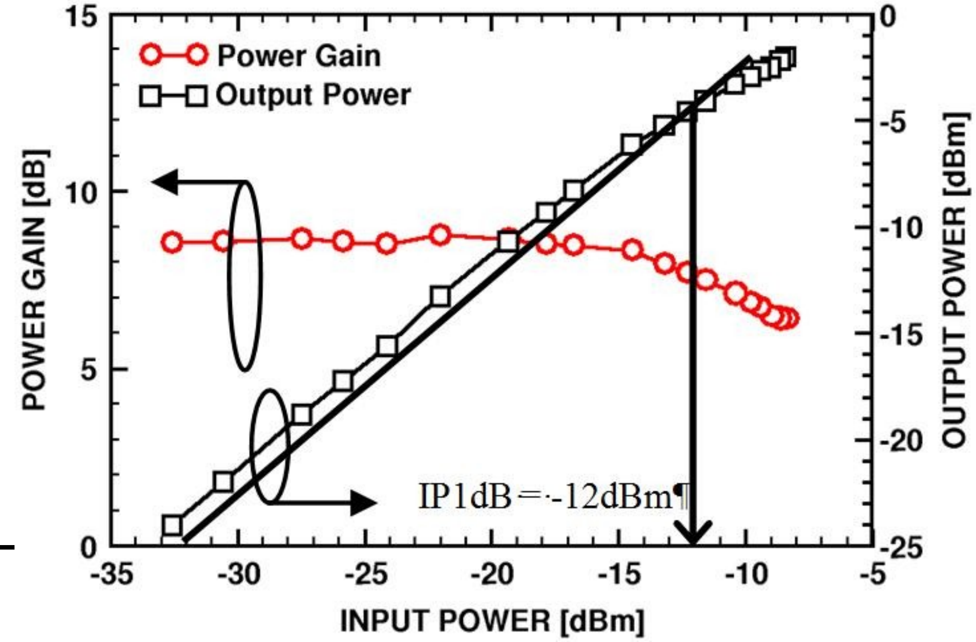
6-stage AC-coupled cascode amplifier
- 63 mW at 1.2V
- 20% stage scaling
- 300µm x 500µm inc. pads

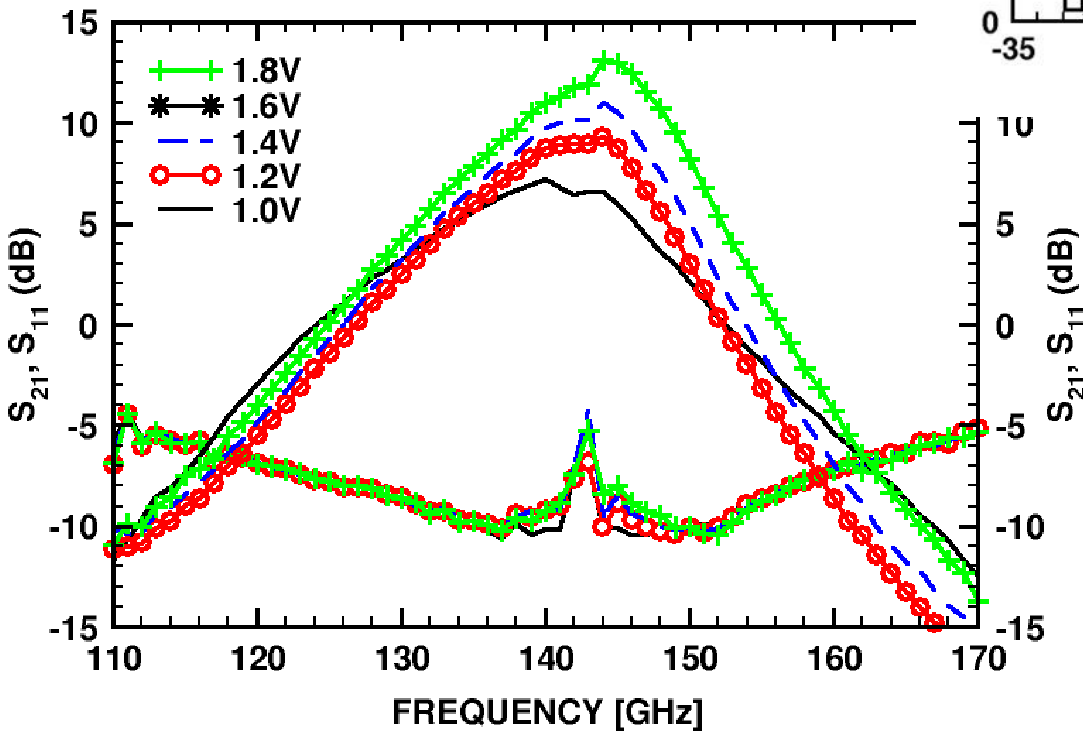
[S. Nicolson RFIC-08]





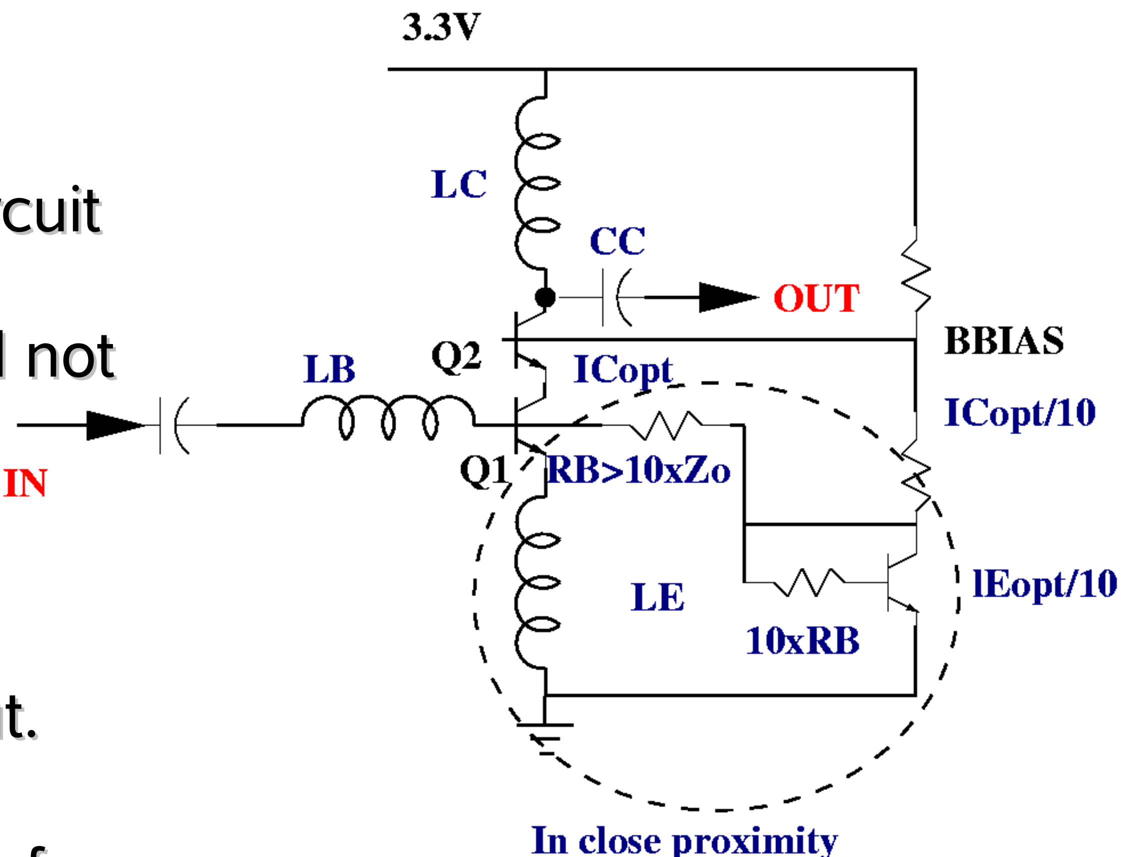
Measured S-params and linearity



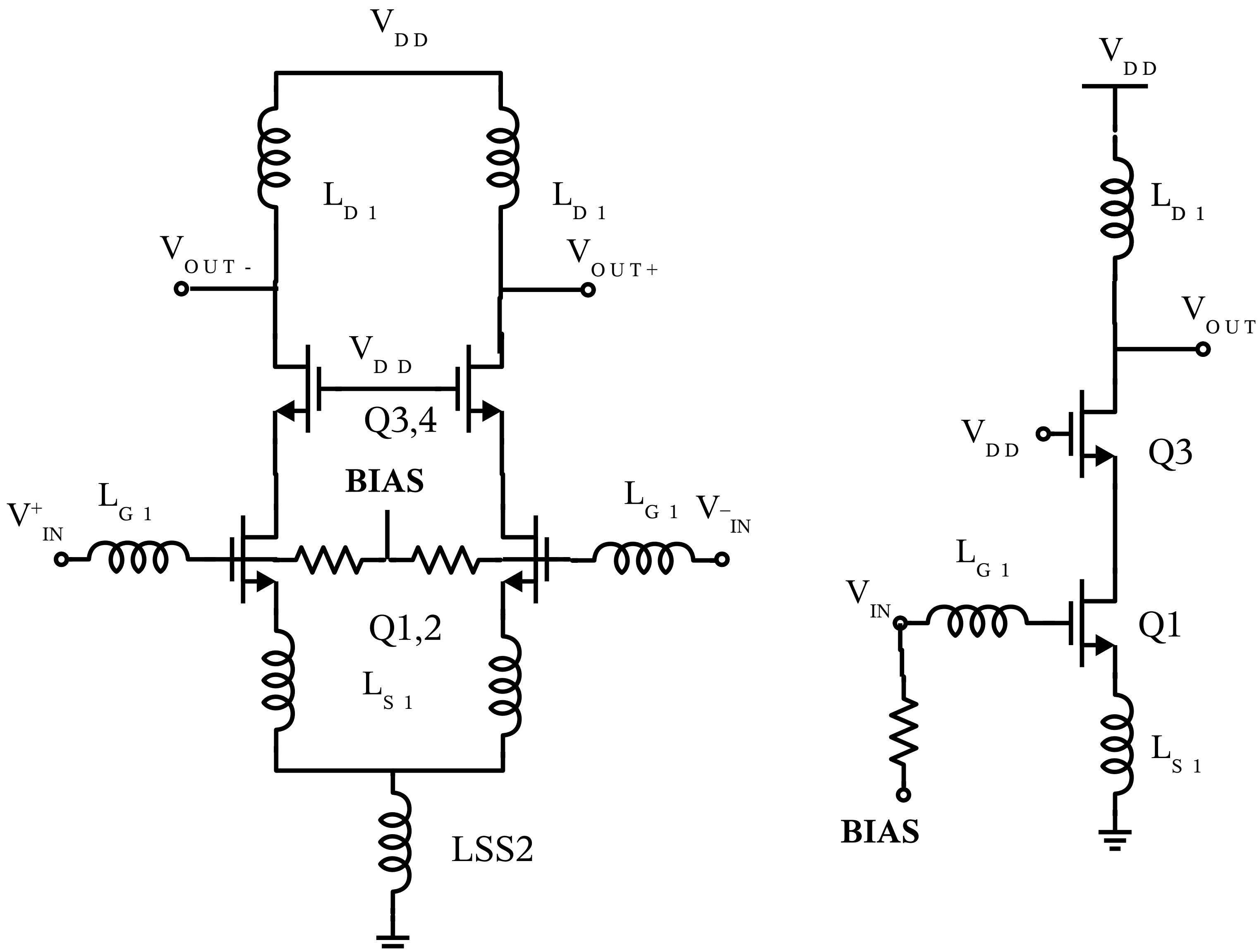


LNA bias network

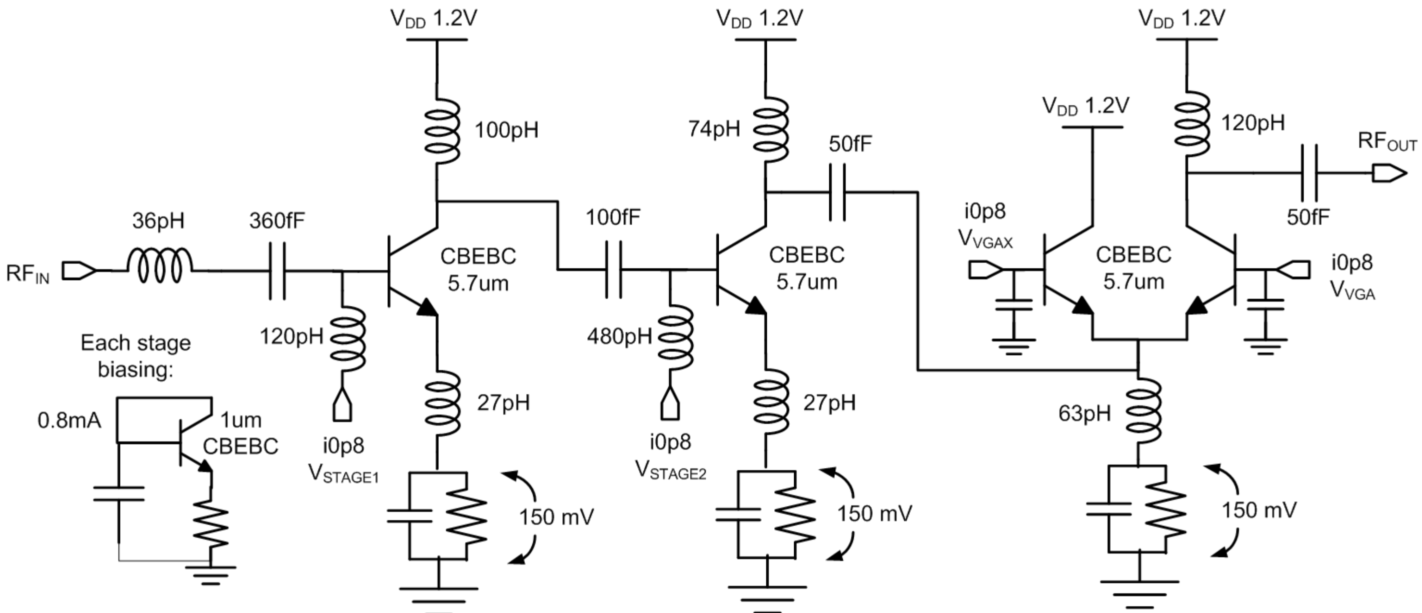
- Reference current may come from bandgap circuit
- Base resistance should not allow for >2mV drop
- Transistors must be in close proximity in layout.
- $V_{CE}(Q_2)$ should be large for large IIP3

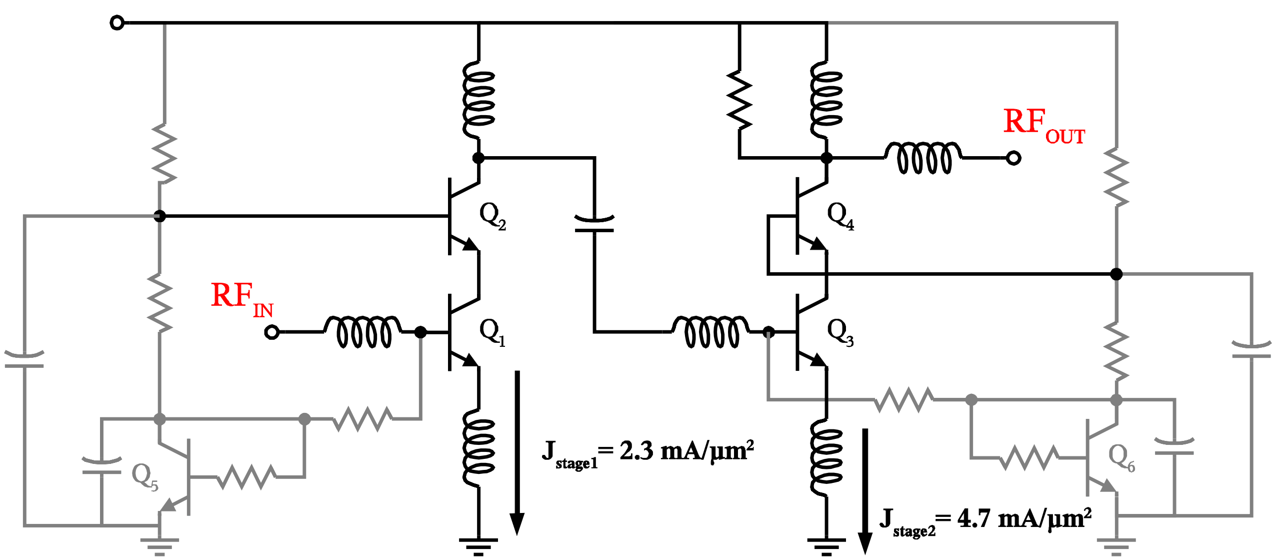


Bias circuits (ii)



Bias circuits (iii)





Differential noise matching

- Design differential half-circuit to be matched to Z_{sopt} (50Ω)
- $Z_{soptdIff} = 2Z_{sopt}(Q_1) + 2j\omega(L_E + L_B)$
- $Z_{INdIff} = 2\omega_T L_E$

Tuned LNA design notes

- MOSFET LNA design usually compromises noise figure for power dissipation (low-noise current is too high!)
- In this approach linearity increases with Z_O.
- Pad capacitance and parasitic capacitance of L_B reduce input impedance
- Tail current source in diff-pair adds noise and common-mode instability. Not recommended!

Tuned LNA topologies summary

CS/CE (L or xfmr feedback)

- low-voltage, low-noise, good linearity,
- poor isolation => difficult to separately design input/output network

CB/CG (no feedback)

- moderate noise, good isolation (HBT-only)
- poor linearity, difficult to simultaneously match noise and source impedance

Cascode (L or xfmr feedback)

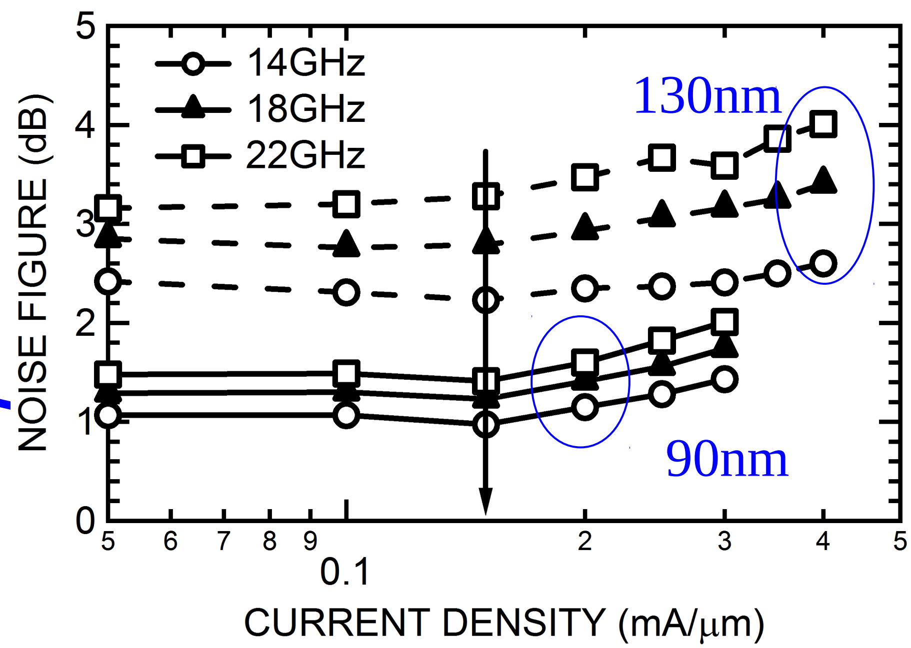
- best isolation, low-to-moderate noise, easy to match, good linearity
- higher supply voltage (but available due to mixer)

Frequency scaling of CMOS LNAs

- **Goal**: Scale the LNA centre frequency

$$f_0^{'} = \alpha f_0$$

- Step 1: *Biasing for Minimum Noise*
  - J_{OPT} unchanged @ 0.15mA/µm
- Step 2: *Device Sizing*
  - W_F unchanged



$$N_F^{'} = N_F / \alpha$$

$$W^{'} = W / \alpha$$

Frequency scaling of CMOS LNAs (ii)

- Step 3: *Input Impedance Matching*
  - L_S: unchanged

$$L_S = \frac{\Re Z_0 - \alpha(R_g + R_s)}{2\pi f_T}$$

$$L_G = \frac{1}{(\alpha\omega)^2 \left(\frac{C_{IN}}{\alpha}\right)} - L_S$$

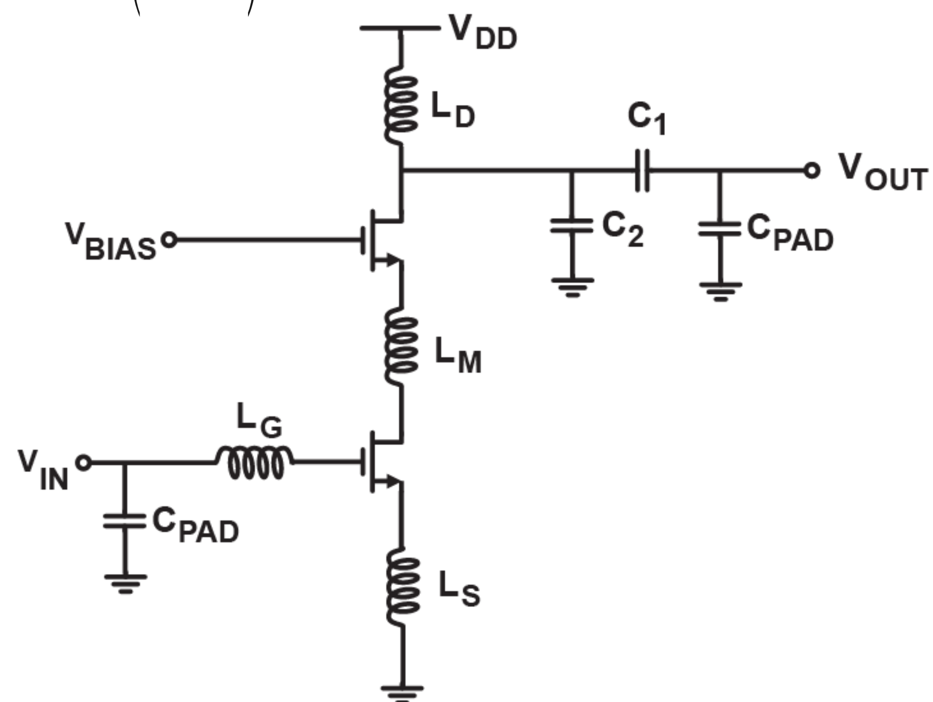
  - L_G: $L_G^{'} = L_G / \alpha$

- Step 4: *Output matching*

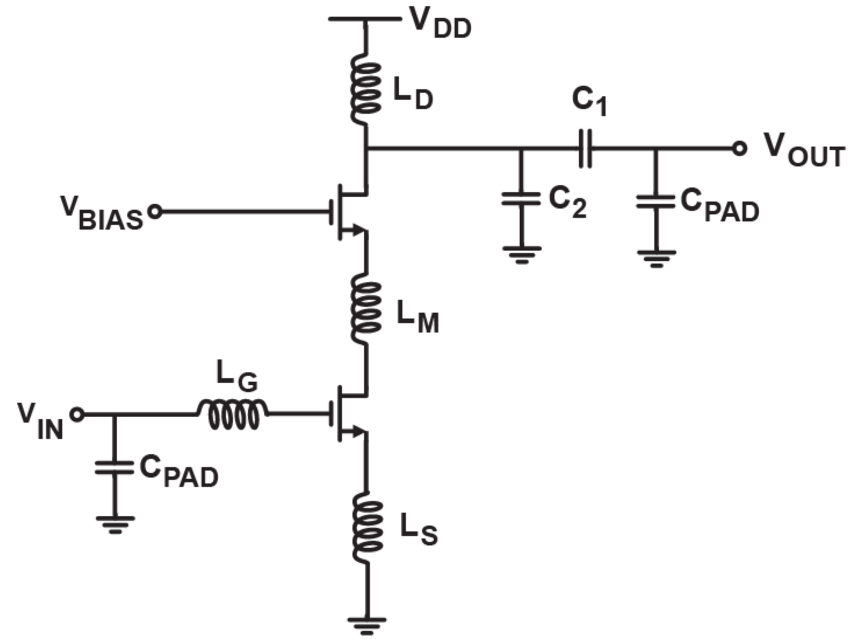
$$L_D^{'} = L_D / \alpha$$

$$C_1^{'} = C_1 / \alpha$$

$$C_2^{'} = C_2 / \alpha$$

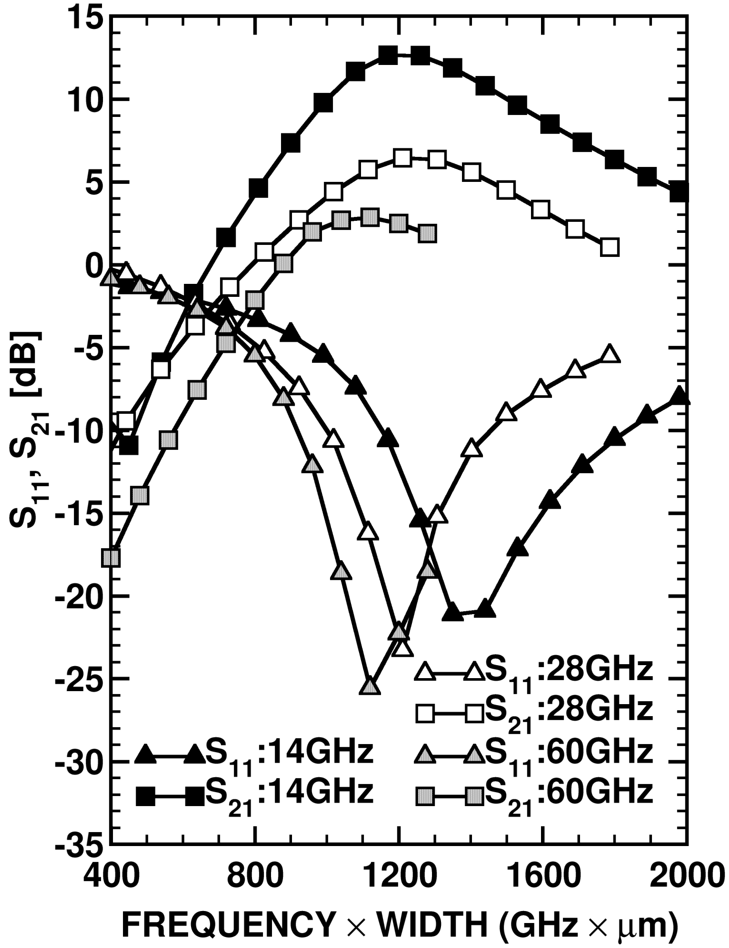


Experimental results



LNA	N_f	W_f um	I_{DS} mA	V_{DD} [V]	L_S [pH]	L_G [pH]	L_D pH	L_M pH	C_1 [fF]	C_2 [fF]	C_{PAD} [fF]
14 GHz, 90-nm	90	1	13.5	1.5	128	1100	545	-	145	70	20
28 GHz, 90-nm	45	1	6.75	1.5	128	535	235	-	75	59	20
60 GHz, 90-nm	20	1	3	1.5	55	190	140	190	30	-	20
12 GHz, 130-nm	90	1	13.5	1.8	177	1340	492	-	122	135	60
24 GHz, 130-nm	45	1	6.75	1.8	177	718	251	-	80	58	60

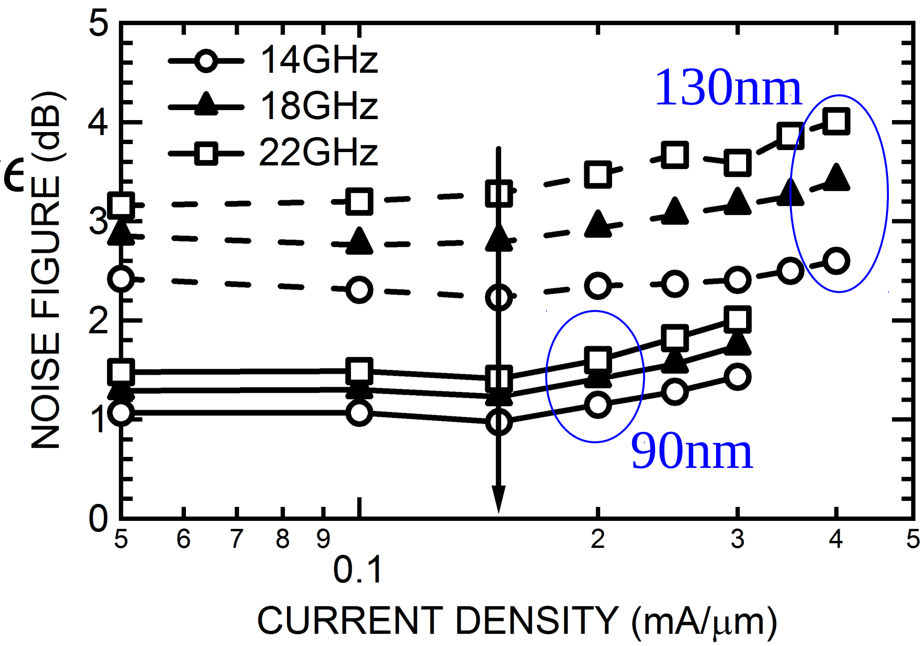
Frequency scaling of 90-nm CMOS LNAs



- Scaling error less than 8%
- Typical process variation: ~20%!

Design porting of CMOS LNAs

- **Goal:** Keep center frequency unchanged, port LNA to another technology node



- Step 1: *Biasing for Minimum Noise*
  - Unchanged: J_{OPT} is invariant between technology nodes

- Step 2: *Device Sizing*
  - Unchanged: Z_{OPT} is invariant between technology nodes

$$W'_f = \frac{W_f}{S}$$

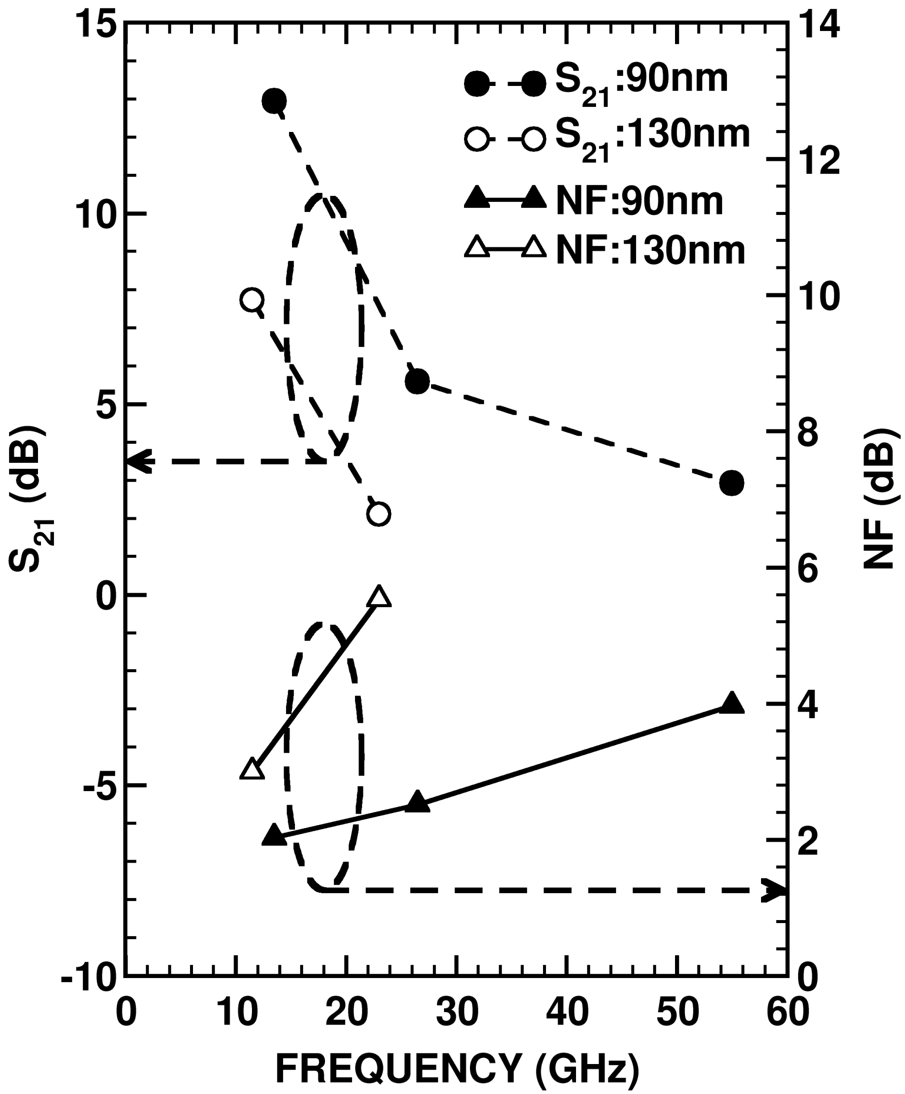
$$N'_f = N_f \times S$$

$$\Rightarrow \quad W' = W$$

Design porting of CMOS LNAs (ii)

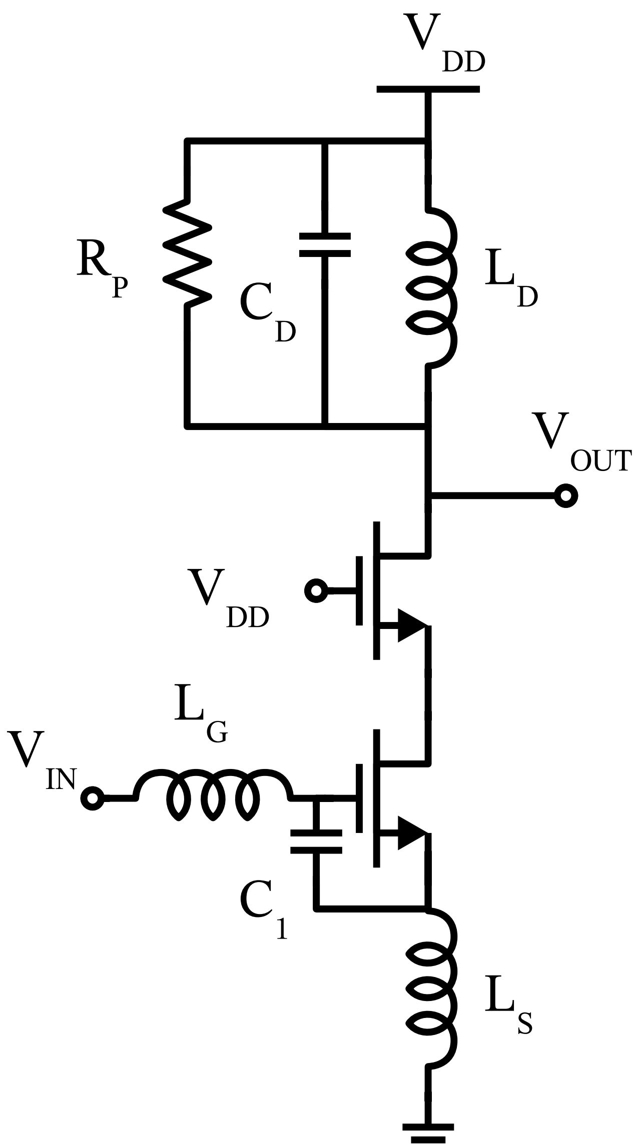
- <u>Step 3:</u> *Input Matching*
-
  - L_S roughly scaled by $1/f_T$: $$L_S = \frac{Z_0 - R_g - R_s}{2\pi f_T}$$
  - $R_G + R_S$ remains approximately constant if if $W_f \Rightarrow W_f/S$ and W=ct.
  - $L_S + L_G$ unchanged because transistor size unchanged

Benefits of scaling for RF/mm-wave



Gain and NF improve with scaling

Power-constrained LNA design



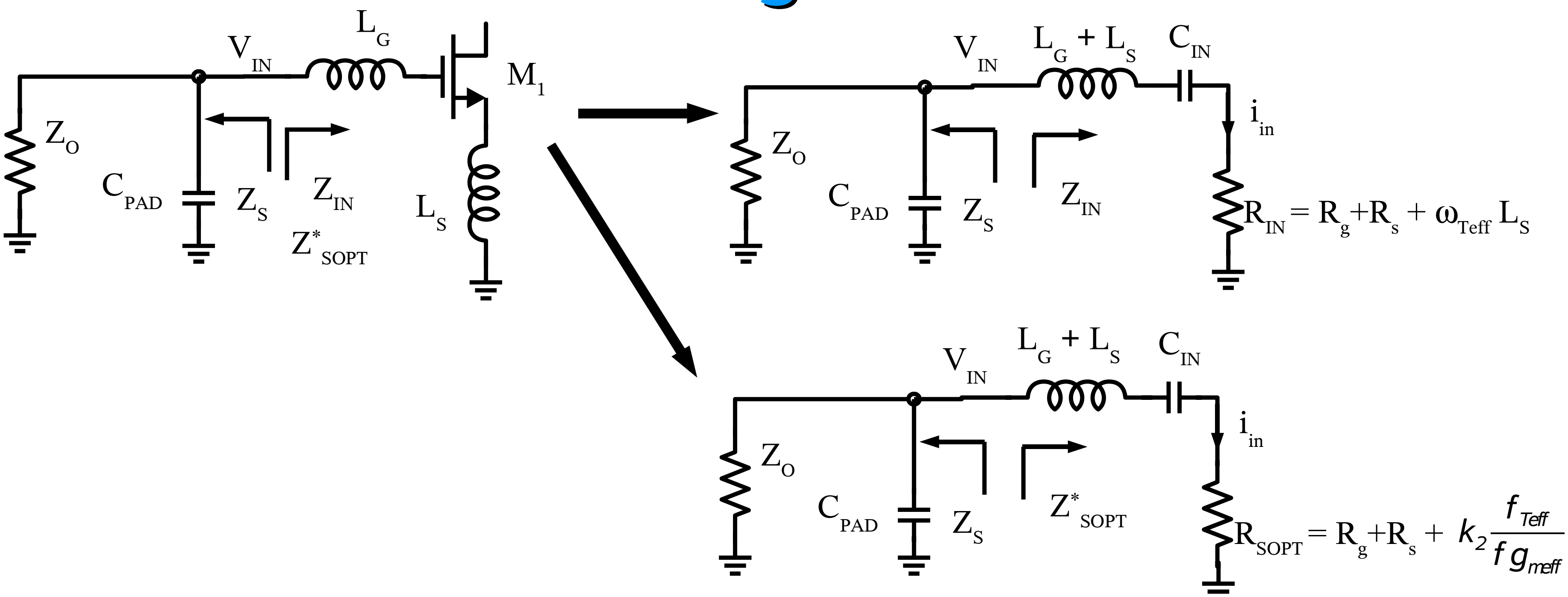
Problem: GHz-range, noise-matched CMOS LNAs consume significant power

Solutions

- Current re-use with CMOS inverter (doubles V_{DD} but still saves power
- Don't noise match, just bias at J_{opt}
- Use external capacitor between gate and source: degrades both gain and NF

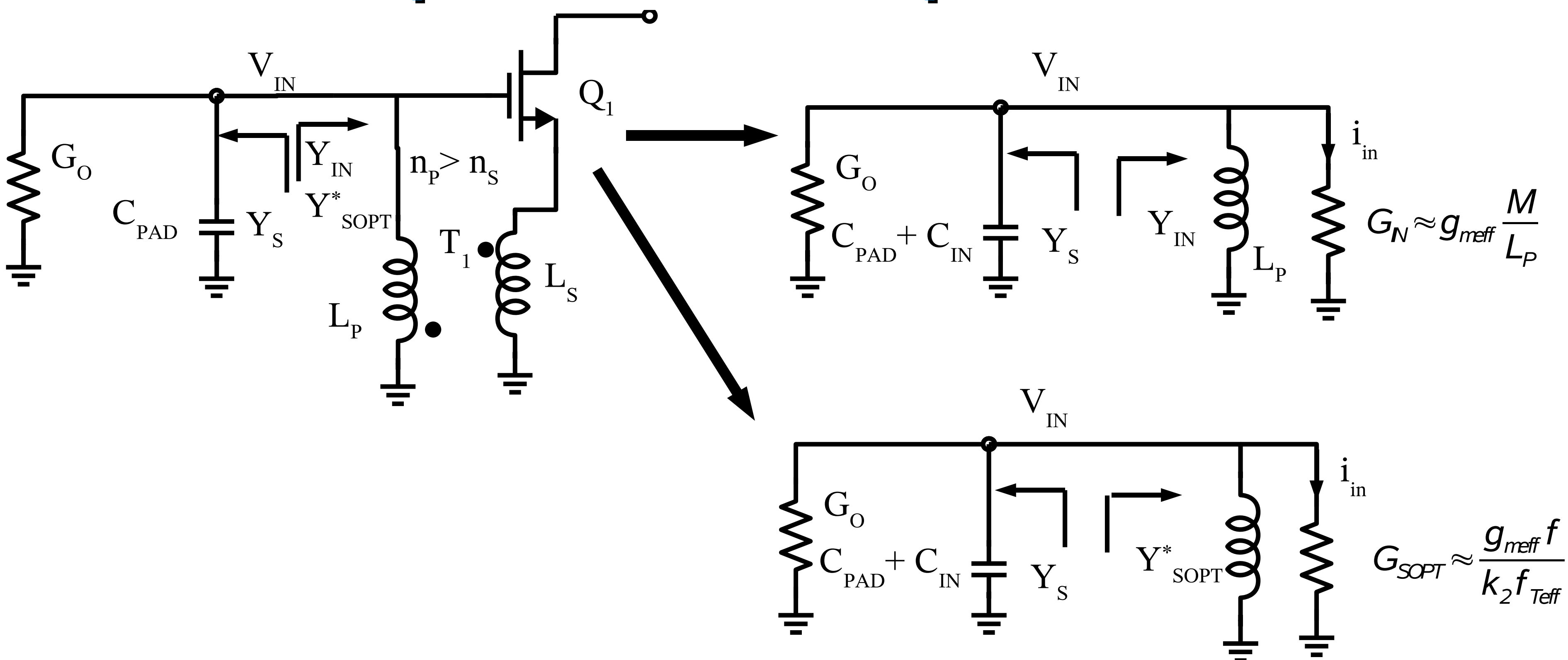
$$f_T \rightarrow \frac{f_T}{1+\frac{C_1}{C_{gs}+2C_{gd}}} \qquad L_S \rightarrow L_S\left(1+\frac{C_1}{C_{gs}+2C_{gd}}\right)$$

Lossless series-series feedback noise matching scheme



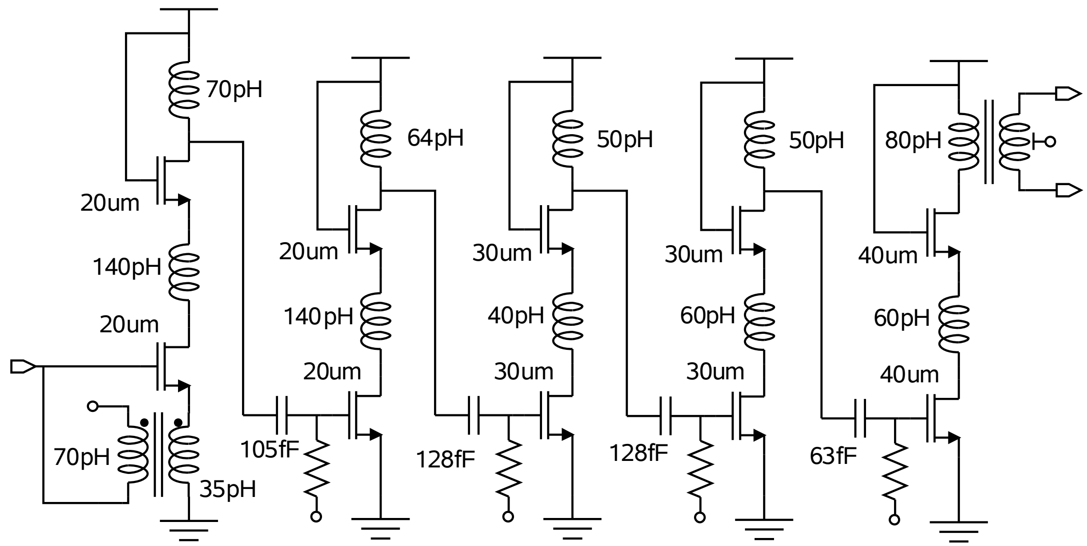
- Pad capacitance causes second, parallel resonance
- Series and parallel resonance reduce input impedance matching bandwidth
- R_{sopt}/G_{sopt} is frequency dependent, so noise matching is NOT broadband

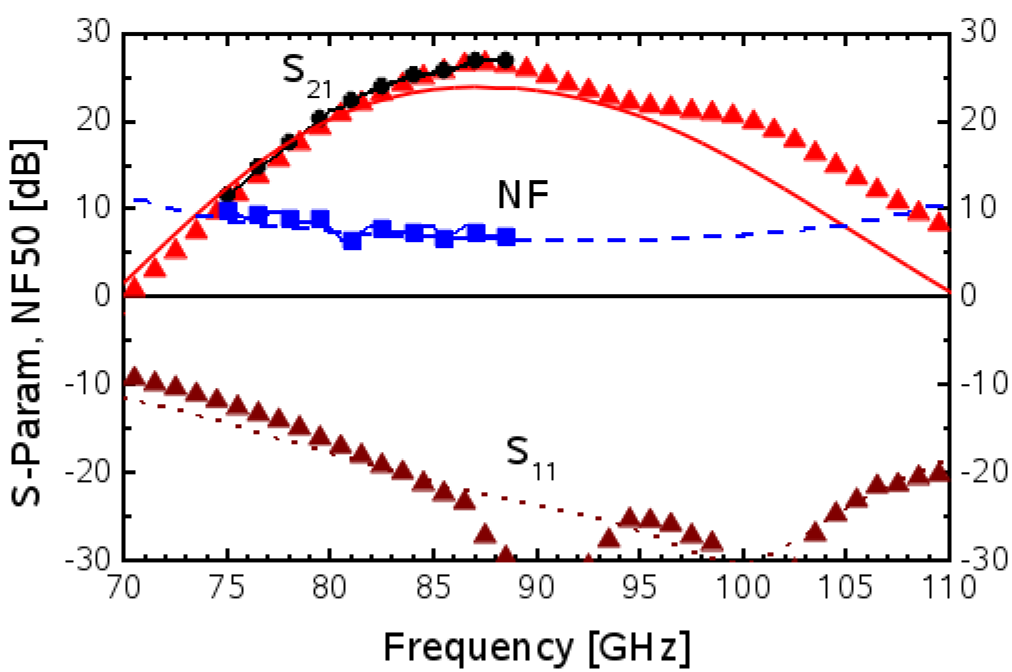
(Lossy) Shunt-series feedback reduces optimal noise impedance



- Single resonance increases input impedance matching BW
- Reduces the transistor size & current for noise matching
- The noise matching is still narrow band because G_{SOPT} is frequency-dependent

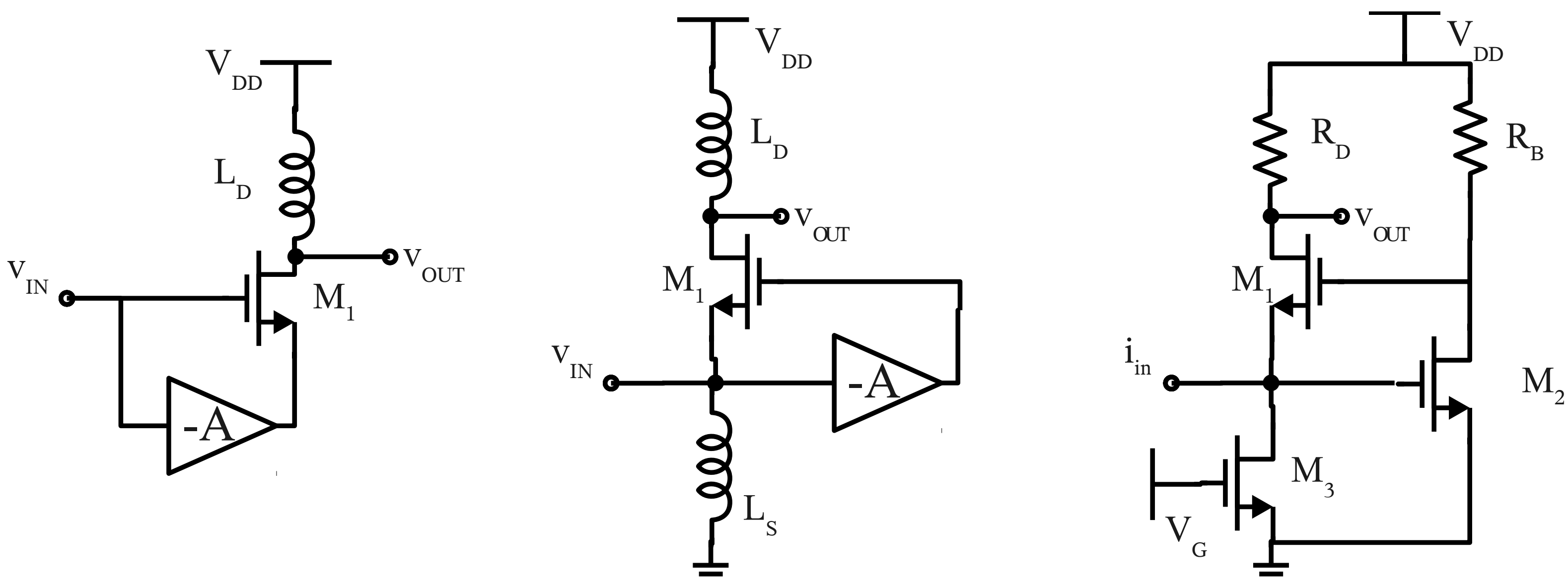
Ex.: W-Band LNA with xfmr feedback





Other low-noise amplifier concepts

- "Noise cancellation" idea by Bruccoleri et al. ISSCC-02
- CG for impedance matching and TIA/ CS for noise matching
- They don't cancel noise, they achieve noise matching over broader bandwidth



Tuned, narrow-band LNA summary

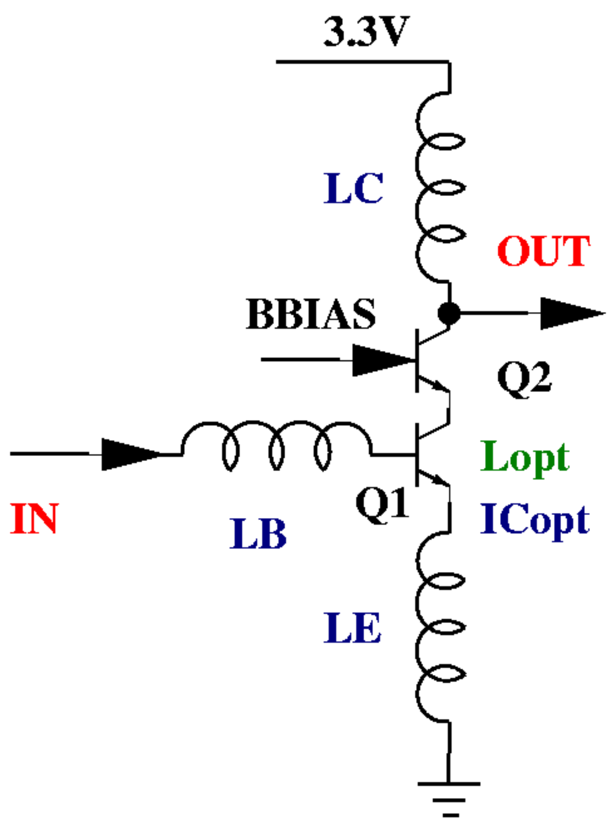
- Cascode with inductive degeneration is the most common topology for LNAs
- Algorithmic design methodology for MOS and HBT LNAs up to 90 GHz
- In MOSFETs J_{OPT} & Z_{OPT} invariant between nodes
- CMOS LNA design scalable in frequency and portable between nodes without redesign
- Frequency scaling error <8%

Back-up slides

7.2 Tuned LNA design methodology using a simulator

Cascode topology with series inductive feedback

- Good isolation allows for separate input/output matching network design.
- Bias current is shared resulting in low power.
- Limited to about 1.8V supply (HBT) or 1.2V supply (LVT MOSFETs)
- Noise slightly degraded (compared to CE/CS) by common base (gate) device.
- If common base/gate device is sized for max. speed, NF_{min} is degraded by a few tenths of dB.



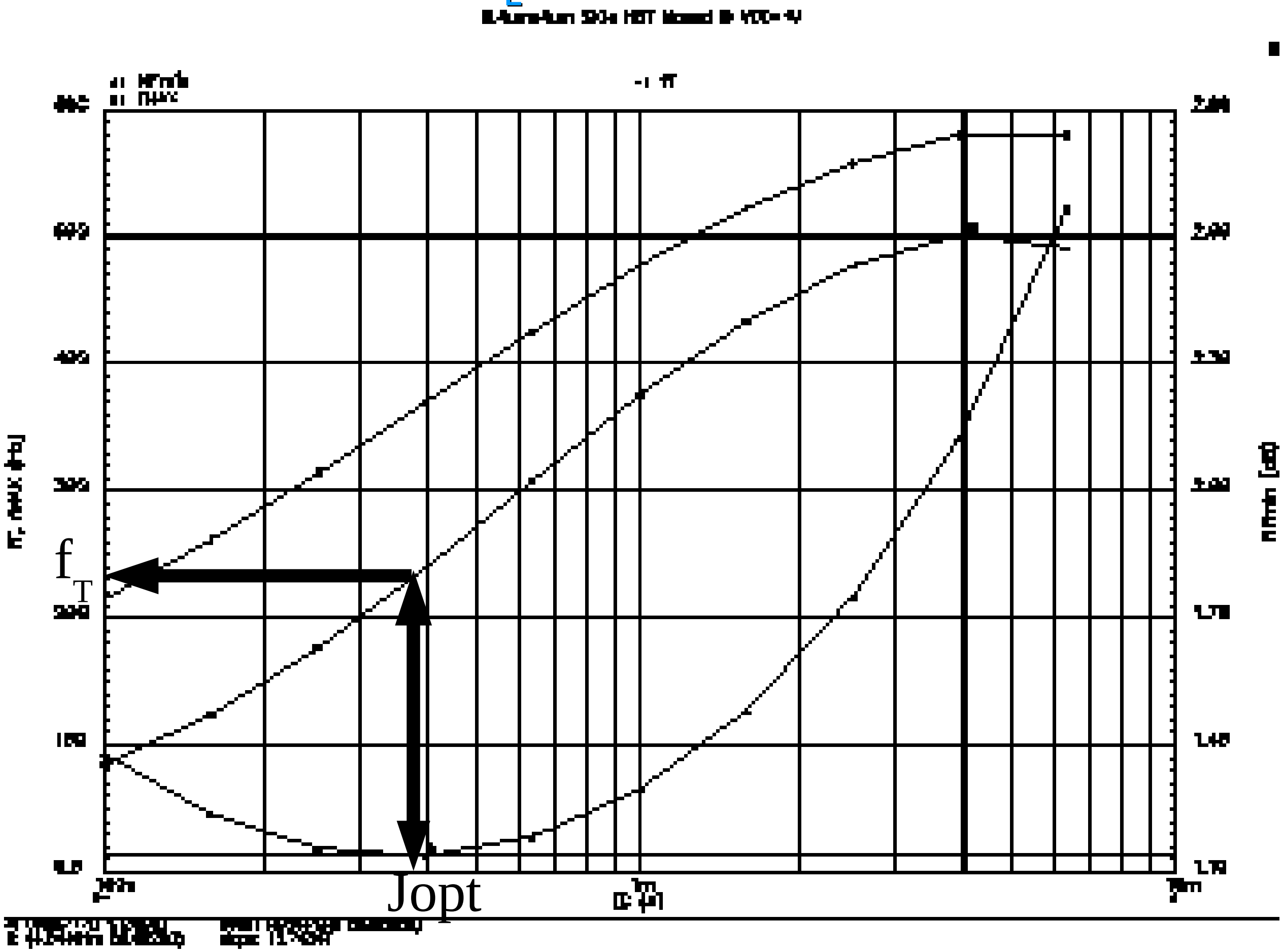
Tuned LNA design steps

- Set V_{CE}/V_{DS} on transistor to maximize linearity (avoid output clipping as in PA design)
- Bias transistor @ minimum NF current density;
- Size transistor for optimal noise resistance - active device matching;
- Add passive (inductive) components for optimal noise impedance, input/output impedance and gain - passive device (classical) matching;
- Add base/gate bias circuitry without impact on noise;
- If linearity goal is not met (typically because of transfer characteristics) use gain control schemes or increase size or current density (may change input matching)

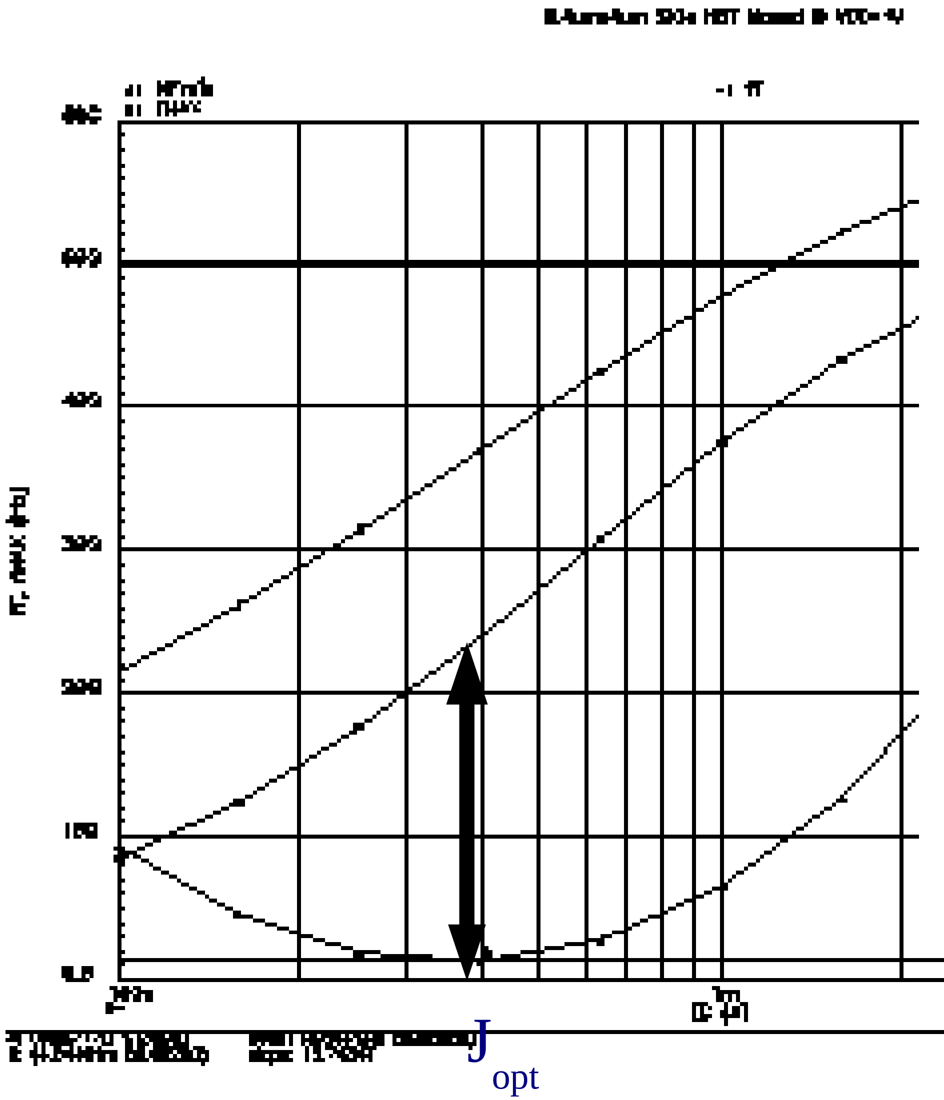
Step 1: find the J_{opt} for the HBT cascode

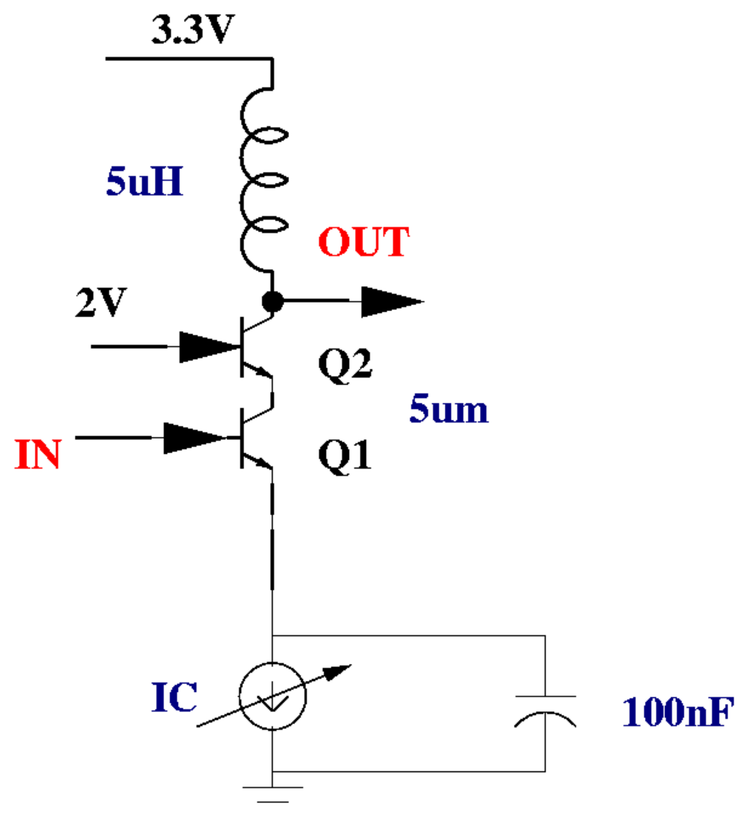
At low-noise bias read f_T;

use average initial size l_E=5 μm and 2 emitter, 3base, 2col. HBT

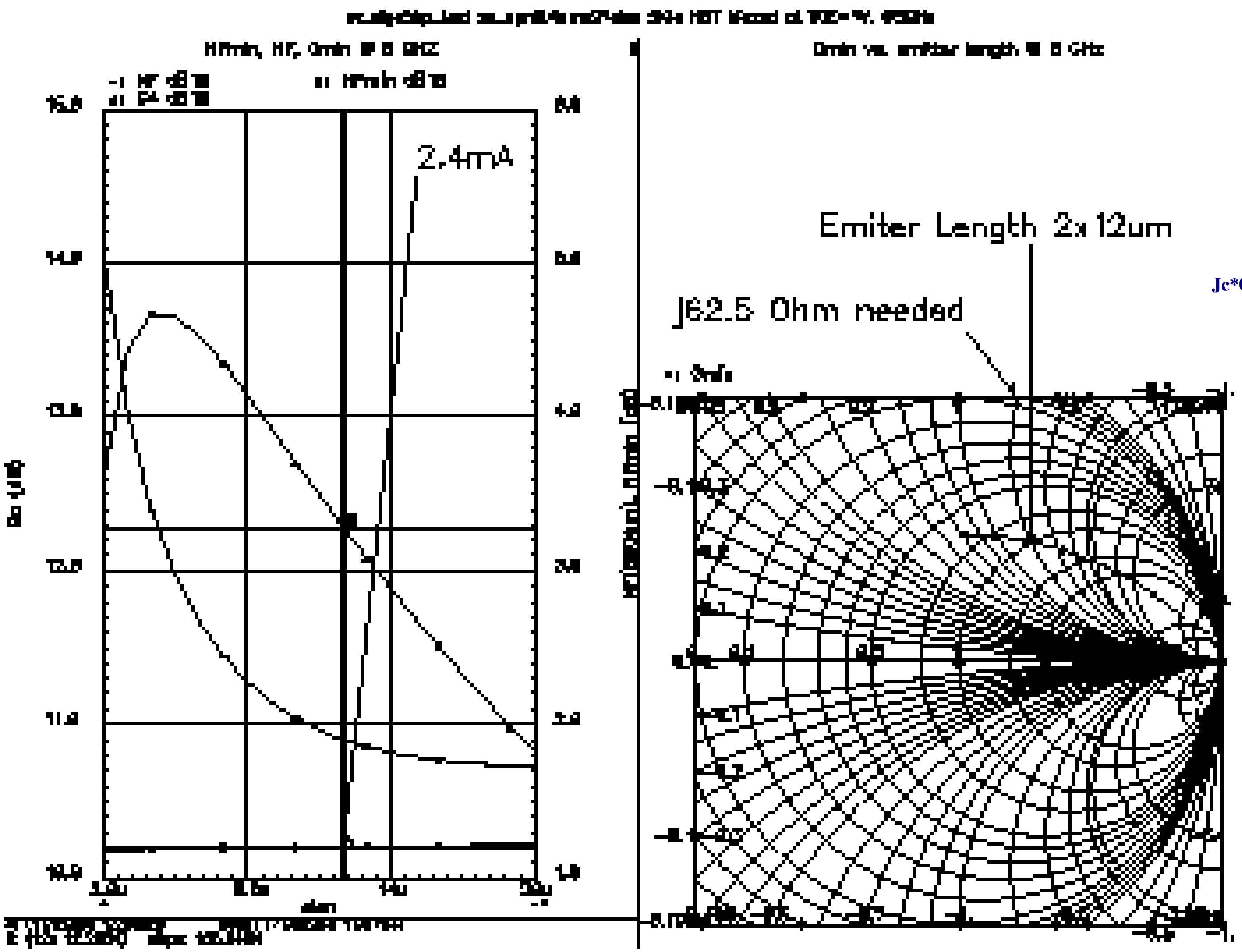


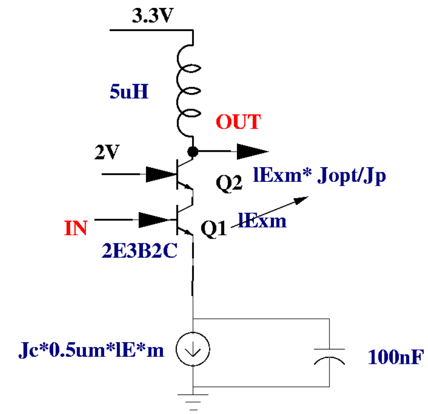
Step1b: HBT cascode low-noise bias (read J_{opt})





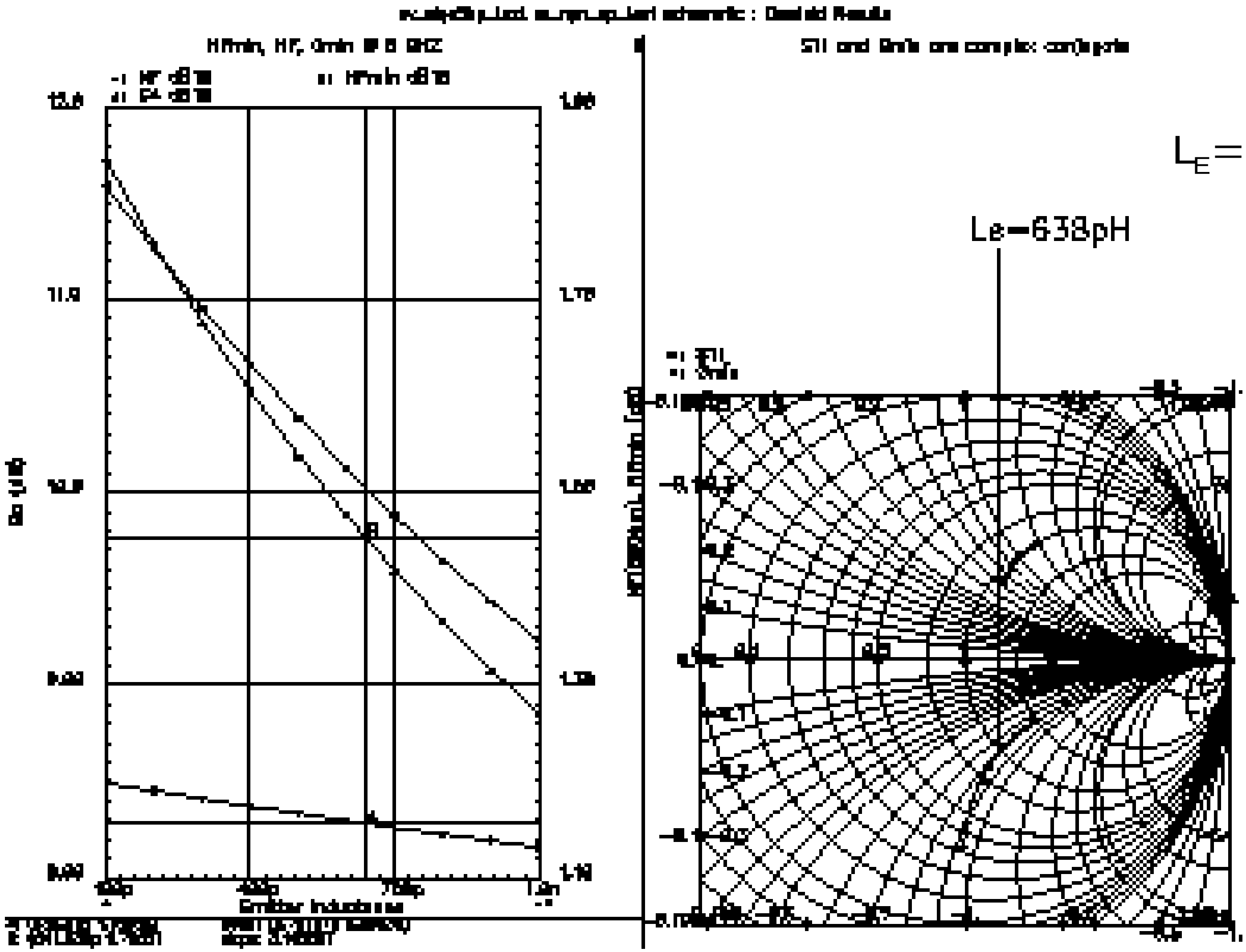
Step-2: cascode sizing for Re(Z_{sopt})=Z_O





Step 3a: add L_E such that $Re(Z_{IN}) = Z_O$

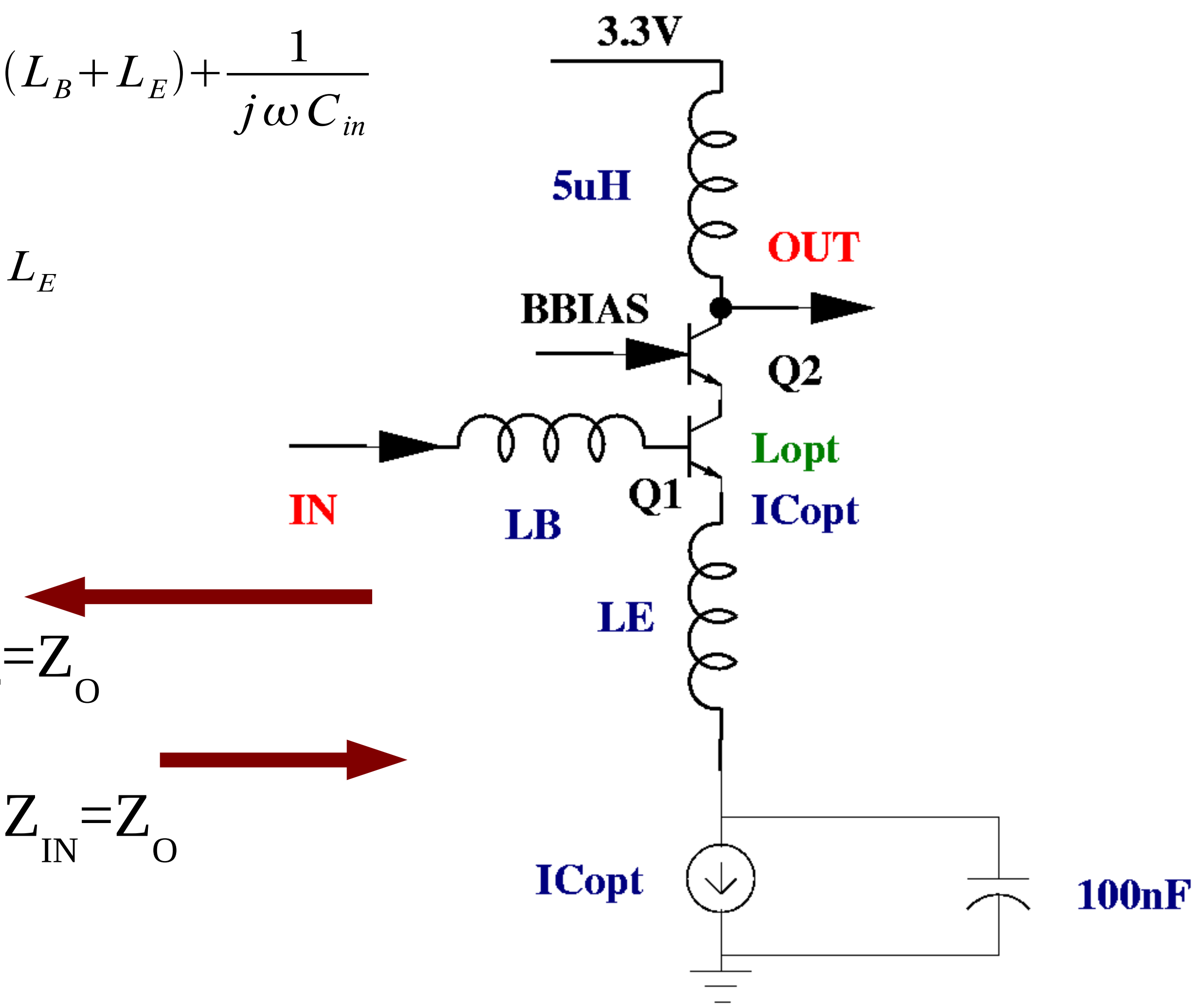
$$L_E = \frac{Z_O - R_b - R_E}{2\pi f_T(cascode)}$$



Step 3b: add L_B such that $Im(Z_{IN}, Z_{sopt}) = 0$

$$Z_{in} \approx Z_O + j\omega(L_B + L_E) + \frac{1}{j\omega C_{in}}$$

$$L_B \approx \frac{1}{\omega^2 C_{in}} - L_E$$



$Z_{SOPT} = Z_O$

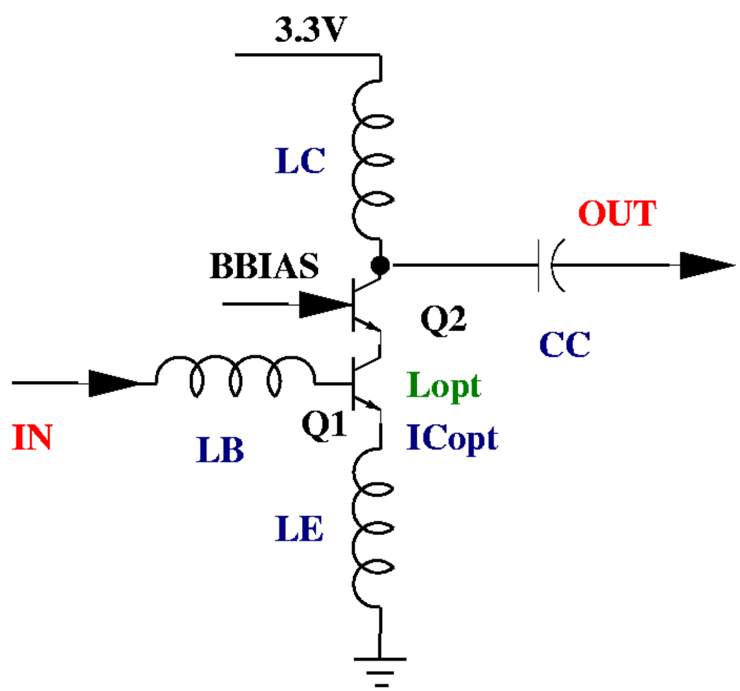
$Z_{IN} = Z_O$

Step 3c: add L_C for maximum gain

- L_C should be as large as possible for gain
- C_C helps lower impedance
- May use 3-terminal inductor or transformer for impedance transform to Z_O
- Linearity is maximized by setting:

R_{CTank} x I_{copt} = V_{CE}(Q2) – V_{CESAT}

- R_{CTank} is the equiv. parallel ac resistance at the output node



Step 3d: matching the output

- Use the Smith chart with the series-shunt or shunt-series technique
- Make sure not to short-ckt. the output to ground (use shunt inductor to V_{CC} not to GND.
- Use 2pF ... 5pF (depending on LNA freq) to de-couple cascode bias and V_{CC} to AC ground.

$$G \leq \frac{1}{4} \frac{f_T^2}{f^2} \frac{R_P}{Z_{in}}$$