Problems for Chapter 5 of 'Ultra Low Power Bioelectronics'

Problem 5.1

a) From Figure 5.12 (a), prove that the unity gain frequency of a transistor can be expressed by the following formula: $f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd} + C_{gb})}$

b) Assume that the transistor is saturated. Ignoring extrinsic capacitances, use known expressions for the small-signal parameters g_m, C_{gs}, C_{gd}, and C_{gb}, and appropriate approximations to show that f_T is nearly $\frac{1}{\pi\tau}$, where τ is the electron transit time in saturation.

Problem 5.2

Assume that you have an NMOS transistor with $W = L = 0.3$ μm that has its source grounded, its drain connected to the power-supply V_{DD}, and its gate connected to a voltage source of value v_{GS}. For parts a) and b) you must take both extrinsic and intrinsic capacitances into account. Use the following device parameters: $\mu C_{ox} = 113$ μA/V^2, $t_{ox} = 14$ nm, $C_{gd0} = C_{gs0} = 205$ fF/m, $V_{T0} = 0.65$ V, $\kappa_0 = 0.7$, $I_0 = 2.5$ fA, $C_{gbe} = 0$, and $\alpha = 1$ (in Equation (5.45)). Consider only the three gate capacitances C_{gs}, C_{gb}, and C_{gd} (ignore other capacitances like C_{bd} and C_{bs}).

a) By computing the values of g_m, C_{gs}, C_{gd}, and C_{gb}, calculate f_T at $V_{GS} = 0.5$ V.

b) By computing the values of g_m, C_{gs}, C_{gd}, and C_{gb}, calculate f_T at $V_{GS} = 1.5$ V.

Problem 5.3

Figure P5.3 illustrates a circuit that uses a strong-inversion MOSFET to create a grounded voltage-controlled linear conductance, whose current is proportional to v_{DS} with a constant of proportionality that varies linearly with v_{IN}. The circuit cancels the v_{DS}^2 term in the first line of Equation (5.18) to achieve a characteristic that is proportional to v_{DS}. You may assume that μ, C_{ox}, W, L, V_{TS}, and κ that describe the MOSFET's current are constant for the MOSFET in Figure P5.3.

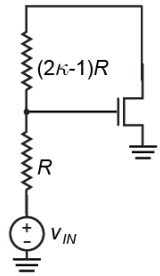

Figure P5.3 Grounded voltage-controlled linear conductance.

a) Assume that the resistors are large and that the current through them is negligible compared with that in the MOSFET. Compute how i_{DS} varies as a function of v_{IN} and v_{DS}.

b) Represent the overall circuit by a small-signal low-frequency model that represents i_{ds} as a function of v_{in} and v_{ds} with the small-signal parameters

being dependent on V_{IN}, V_{DS}, and the technology parameters of the MOSFET. You may ignore all capacitances in the circuit.

Problem 5.4

This problem investigates optimum biasing conditions for the common-source amplifier shown in Figure P5.4.

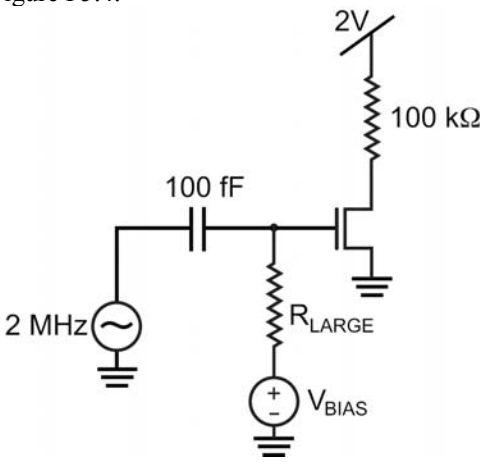

Figure P5.4 Common source amplifier for Problems 5.4 and 5.5.

The amplifier is designed to run off a 2 V supply. Treat V_{BIAS} as a voltage which is automatically adjusted (whenever any transistor parameters are changed) to keep a DC bias current of 10 μA flowing through the transistor. This current drops 1 V across the 100 kΩ load resistor, such that the transistor is kept in saturation. The dc voltage at the transistor gate is determined by V_{BIAS} and R_{LARGE}. The resistor R_{LARGE} is large enough to have little impact at 2 MHz, the input signal frequency, and may be treated as an open for this problem. The length of the transistor is fixed at 1.5 μm. The other transistor parameters are: C_{ox} = 2.4 fF/μm^2, μC_{ox} = 113 μA/V^2, t_{ox} = 14 nm, C_{gd0} = C_{gs0} = 205 fF/m, V_{T0} = 0.65 V, and κ_0 = 0.7.

a) Draw a small-signal model of this circuit including all small-signal components of the MOS transistor.
b) Ignoring C_{gd}, write an expression for the small-signal gain of this amplifier with the transistor biased in subthreshold.
c) How does the attenuation of the signal to the gate change with transistor width W?
d) How does the gain from the gate to the output change with transistor width?
e) Should the width be small or large for maximum gain?
f) How would including C_{gd} affect the small-signal gain?
g) If the dc gate bias is at the largest subthreshold bias possible, corresponding to a bias of I_{T0} = 200 nA in a W / L = 1 transistor, and given that we still want to maintain a 10 μA bias current, what is the gain that is achieved at the edge of subthreshold operation? (Hint: The W/L of the transistor will need to be increased beyond 1 to satisfy these constraints).

Problem 5.5

This problem is a continuation of Problem 5.4 and also pertains to Figure P5.4.

a) Including C_{gd}, write an expression for the small-signal gain of the amplifier with the transistor biased above threshold.
b) How does the attenuation of the signal from the input to the gate change with transistor width?
c) How does the gain from the gate to the output change with transistor width?
d) How does the feedback transmission from the output to the gate via C_{gd} change with transistor width?
e) Find the optimum width at which the gain of the amplifier at 2 MHz is maximized. You may use MATLAB to help you answer this part of the problem.

Problem 5.6

The structure shown in Figure P5.6 is a PMOS transistor whose gate is used to bias its well voltage using a PMOS source-follower. You may assume that $V_S > V_D$ and that all transistors have identical characteristics. Note that V_{BIAS} is referenced with respect to V_{DD}.

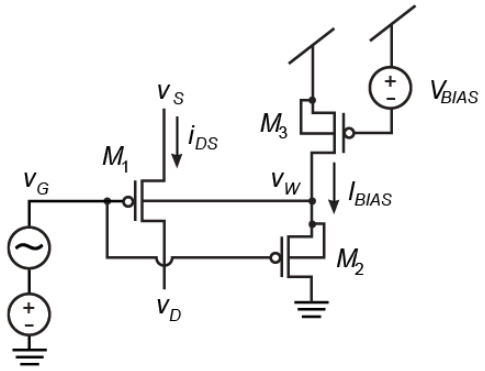

Figure P5.6 Well biasing though a source-follower.

a) If $i_{DS} = I_{BIAS}$, is $v_S = v_W$, $v_S > v_W$, or $v_S < v_W$?
b) A former student tells you that this circuit magically ensures that $\kappa = 1$ for M_1 as long as $i_{DS} < I_{BIAS}$ and as long as M_1 operates in subthreshold. Prove that the student is correct by showing the following:
    i. Show that the source-follower formed by M_2 and M_3 has a gain of 1 for small signals. For large signals, is the source-follower $\Delta V_W/\Delta V_G$ still 1?
    ii. Show that the small signal transconductance of M_1 is $\frac{\partial i_{DS}}{\partial v_G} = \frac{I_{DS}}{\phi_t}$, just like a bipolar transistor, and is independent of κ.
    iii. Extrapolating from your reasoning in previous parts, argue that $i_{DS} = I_{BIAS} e^{[v_S - v_G - V_{BIAS}]/\phi_t}$
    iv. If $i_{DS} < I_{BIAS}$, show that $V_W > V_S$, guaranteeing that the well-source junction remains reverse biased.

Problem 5.7

In this problem we will analyze the circuit shown in Figure P5.7 For this circuit, assume that $V_{DD}^{HIGH} > V_{DD}$, M_3 and M_4 are identical to each other with $W = L = 30$ µm, and that M_1, M_2, M_5, and M_6 are identical transistors.

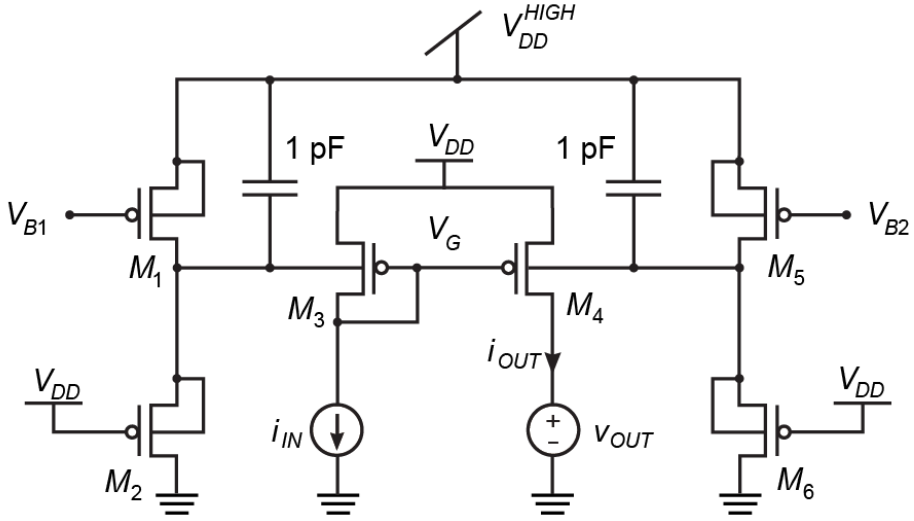

Figure P5.7 Circuit schematic for Problem 5.10.

a) Find the large-signal current gain $\frac{i_{OUT}}{i_{IN}}$ of the circuit in Figure P5.7 as a function of the differential voltage $\Delta V_B = V_{B1} - V_{B2}$ in subthreshold. You may assume that all transistors are saturated. Note that M_1, M_2, M_5 and M_6 all have their wells tied to their sources.

b) Find the small-signal output current change i_{out} caused by the application of a small-signal differential voltage $\Delta v_b = v_{b1} - v_{b2}$. Ignore Early-voltage effects and assume that $I_{OUT} = I_{IN} = 1$ nA.

Problem 5.8

This problem requires the use of a circuit simulator such as SPICE. Find the f_T and r_o of the following transistors using SPICE:

a) An NMOS transistor with $W = 1.5$ µm and $L = 0.6$ µm
b) An NMOS transistor with $W = 1.5$ µm and $L = 6$ µm
c) An NMOS transistor with $W = 15$ µm and $L = 0.6$ µm
d) An NMOS transistor with $W = 15$ µm and $L = 6$ µm
e) Comment on how f_T and r_o depend on W and L. Does the observed dependency match what you would expect?

Problem 5.9

This problem will explore small-signal models in micromechanical systems. An electrostatic parallel-plate micromechanical capacitor has a fixed voltage V_0, dielectric constant ε_0, plate area A, and a distance between its plates of x. The electrostatic force

of attraction between the capacitor plates is found by differentiating the stored $(1/2)C(x)V_0^2$ energy with respect to x.

a) Show that the magnitude of this force is given by $F_{attr} = (1/2)\varepsilon_0 A V_0^2 / x_0^2$
b) Compute the effective spring stiffness of the electrostatic plates at a given distance of separation x_0 by using small-signal analysis to determine how the electrostatic force varies as x varies around x_0 by a small-signal deviation.
c) Explain why the negative spring stiffness that you obtained in part b) is caused by the presence of positive feedback in the physical system.
d) To ensure that the overall capacitor is mechanically stable and does not result in the two plates crashing into each other, what is the minimum stiffness of a passive mechanical spring that must be attached to the capacitor to ensure that its plates remain separated at a distance of x_0 from each other?

Problem 5.10

Equation (5.32) reveals the functional dependence of the inversion charge in the channel for strong inversion while Equation (5.51) reveals the corresponding functional dependence in weak inversion.

a) If we are operating right in the central portion of moderate inversion, generate an intuitive guess for the shape of the charge distribution along the channel in moderate inversion.
b) If $Q_{IL} = 0$ in all regions of operation (strong, weak, or moderate), and Q_{I0} in all regions is normalized to 1, plot your intuitive guess along with the actual shapes of the charge distribution for weak inversion and strong inversion. You may use MATLAB to help you generate your plots.
c) Using arguments similar to that used to derive Equation (5.42) but noting that the diode-clamp approximation will not lead to one-for-one changes in the surface potential with changes in the source voltage, suggest how you would estimate an approximate value for the intrinsic value of C_{gs}.