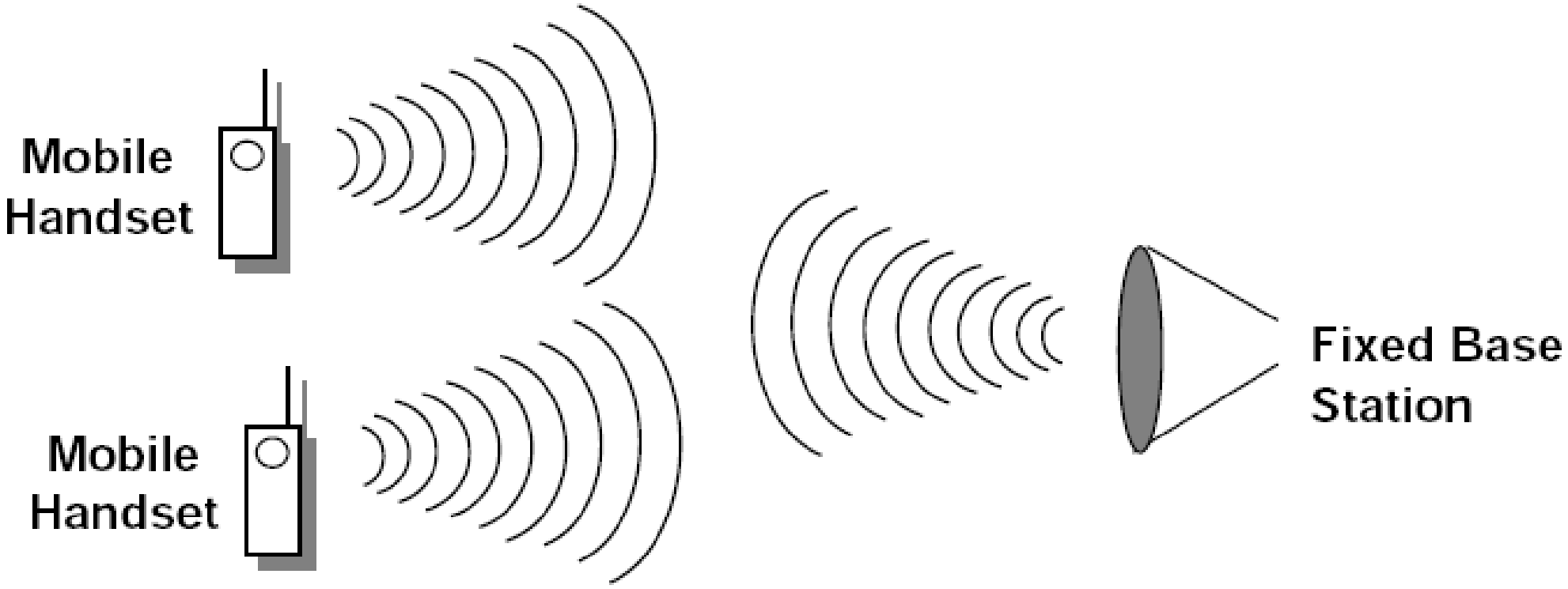
Chapter 6: Tuned Power Amplifiers

Outline

- Tuned PA Fundamentals
- Classes of Tuned PAs and Voltage Waveforms
- Linear Modulation of PAs
- Class A PA Design Methodology
- Examples of CMOS and SiGe HBT mm-wave PAs
- Efficiency and power combining techniques

Characteristics of PAs (L. Larson 2007)

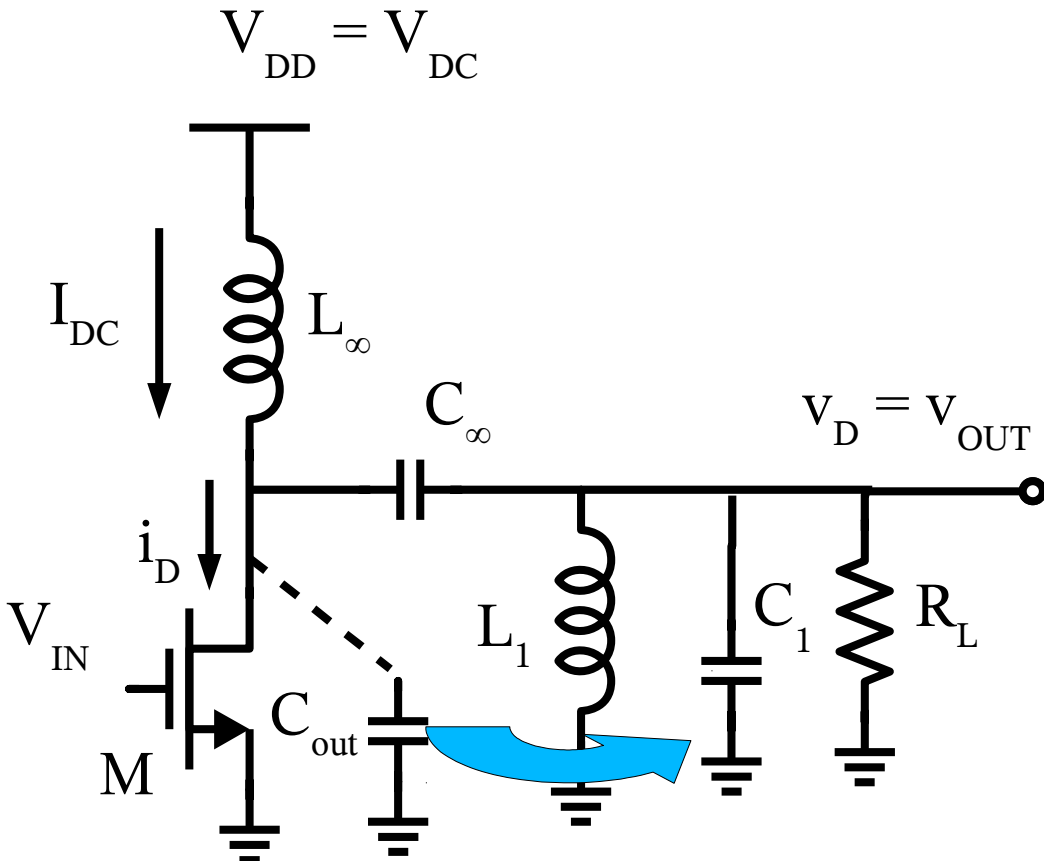


Power : 0.1 mW - 2 W
Linearity Requirement: Moderate-Severe
Cost: Very Low (<$3)
Efficiency Requirement:PAE>30%
Worldwide Market:>800M/yr(!).

Power : 50W - 200W
Linearity Requirement: Severe(!)
Cost: High (>$100)
Efficiency Requirement:PAE>10%
Worldwide Market > 1000K/yr.

Tuned PA Fundamentals

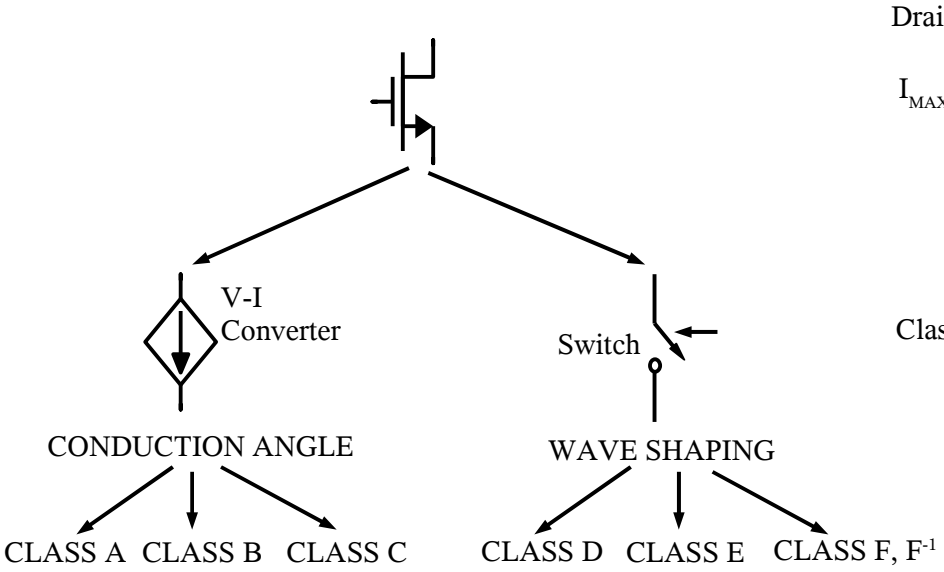
- ***G*** is the power gain of the PA
- P_{out} is the output power of the PA
- ***f*** is the centre frequency of the PA
- ***PAE*** = $(P_{OUT} - P_{IN})/P_{DC}$
- **Fourier series analysis required**

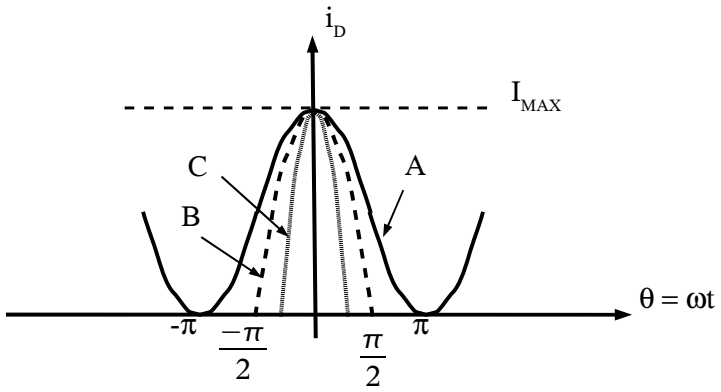


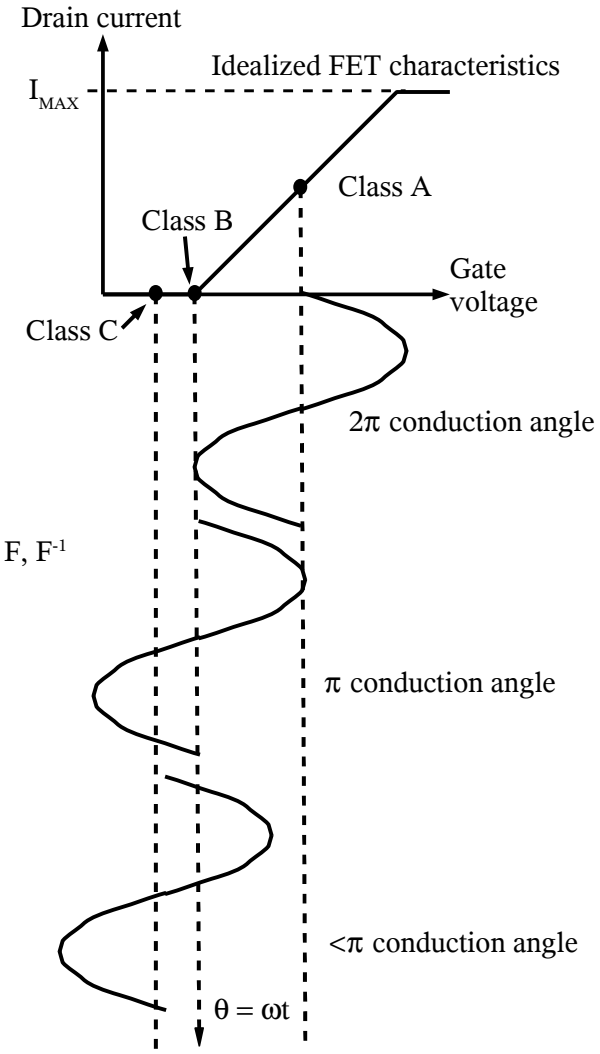
$$FoM_{PA} = P_{OUT} \times G \times PAE \times f^2$$

$$P_{OUT} = \frac{1}{T}\int_0^T V_{DD}\cos(\omega t)\frac{V_{DD}\cos(\omega t)}{R_L}dt = \frac{V_{DD}^2}{2TR_L}\int_0^T [1+\cos(2\omega t)]dt = \frac{V_{DD}^2}{2R_L}$$

Classes of tuned PAs







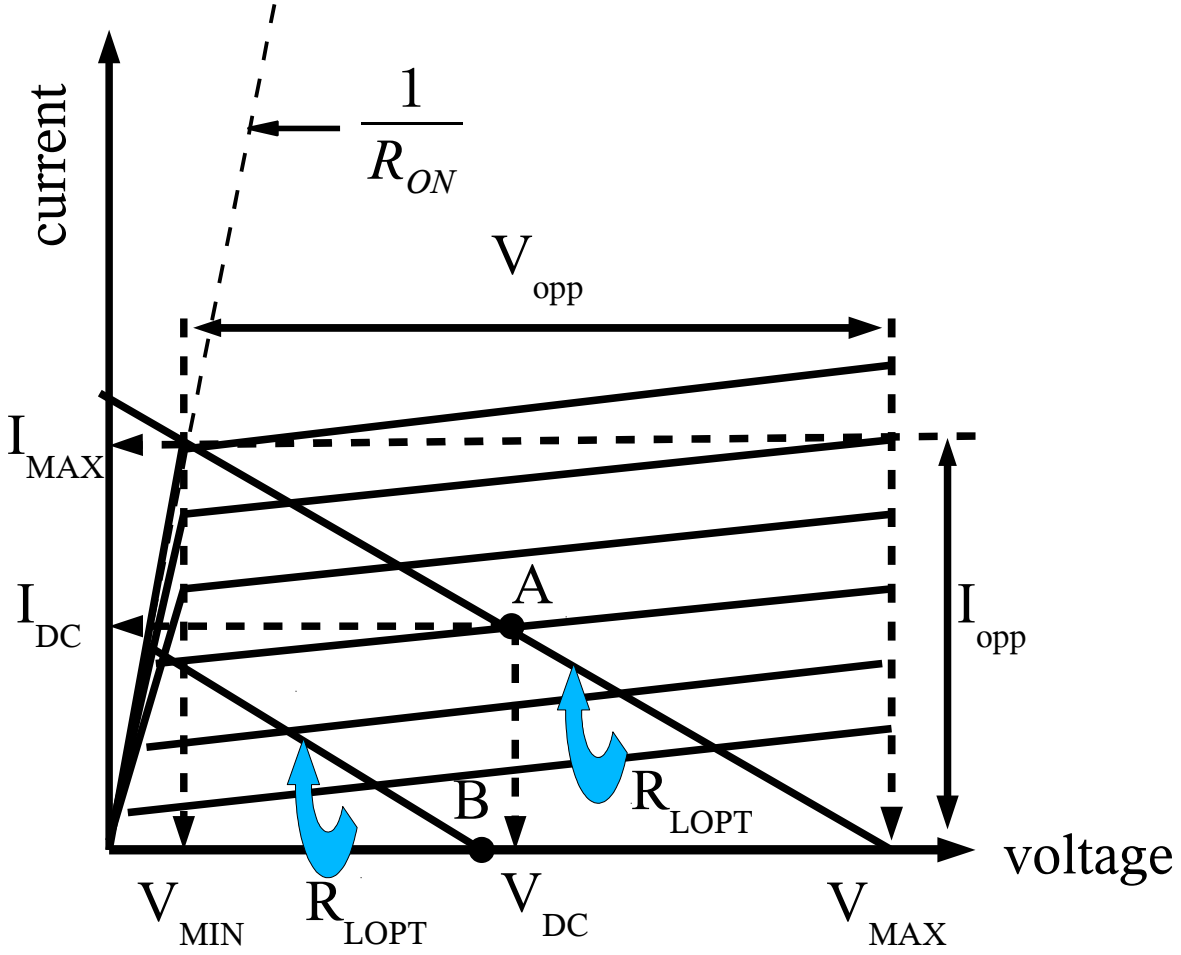
- Controlled current source: A (100% conduction), B (50% conduction), AB (50%<conduction angle<100%), C (<50% conduction)
- Switching PAs (high efficiency > 50%): Class D, E, F, F^{-1}

PA Design Fundamentals: R_{LOPT}

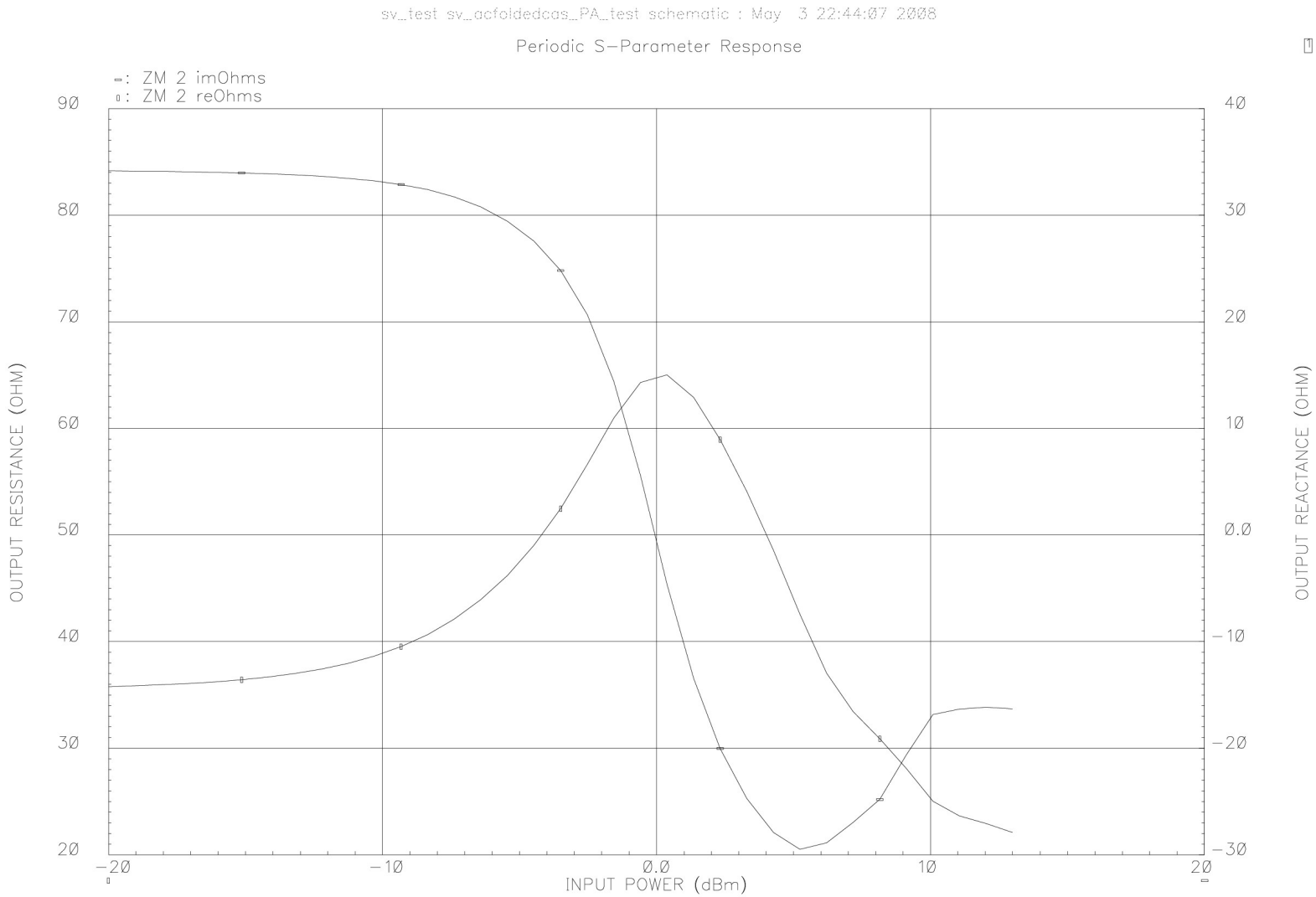
$P_{OUT} \sim (V_{MAX} - V_{MIN}) * I_{MAX}$

$PAE \sim (1 - V_{MIN}/V_{MAX})$

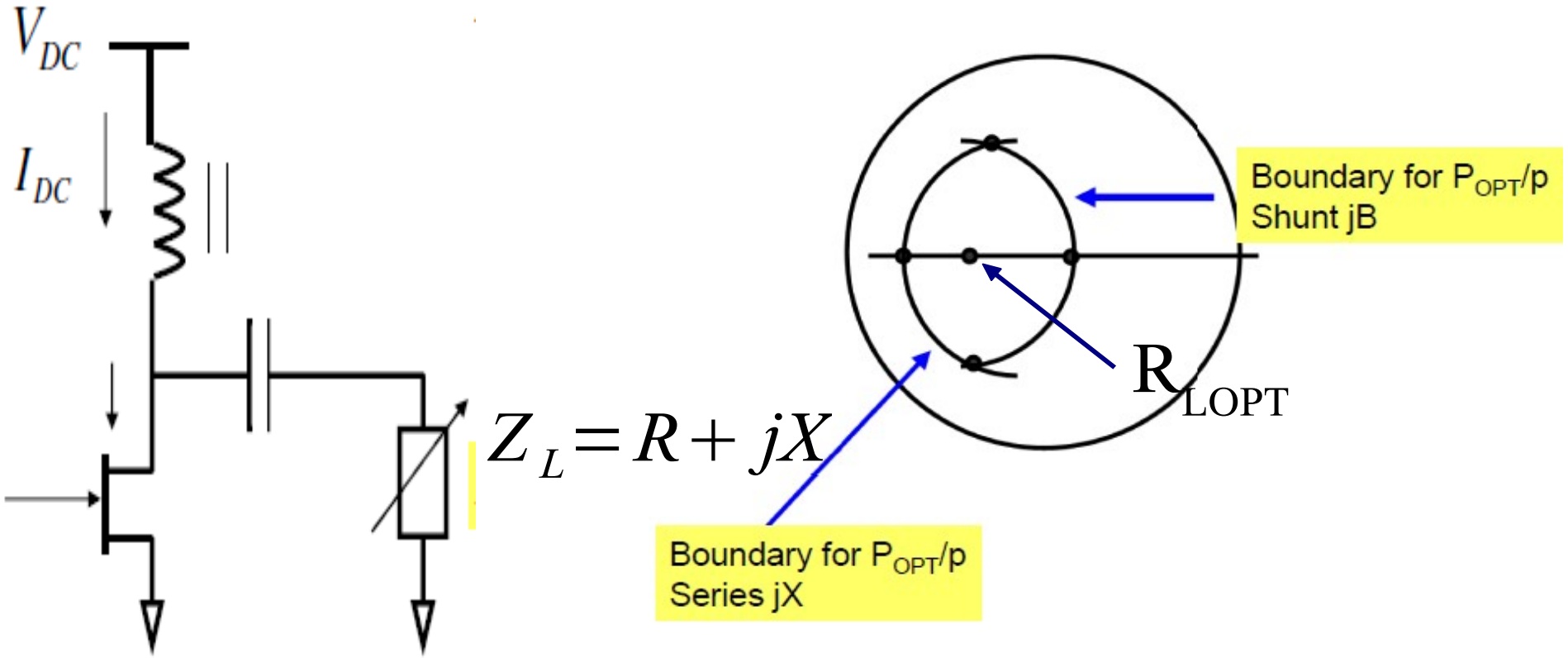
$$R_{LOPT} = \frac{V_{opp}}{I_{opp}} \approx \frac{V_{MAX}}{I_{MAX}} = \frac{V_{MAX}}{2 \cdot I_{DC}}$$



Z_{out} as a function of P_{in}



Load pull contours



Courtesy of Stephen Long
UCSB

Output matching network design

- Performs several functions:
  - transforms the load impedance Z_0 to R_{LOPT}
  - provides a short-circuit at all harmonics so that only the power of the fundamental is transferred to the load, and
  - maintains the impedance transformation over the entire transmit bandwidth.

$$Q = \sqrt{\frac{Z_0}{R_{LOPT}} - 1} = \sqrt{\frac{50}{2} - 1} = 4.9 \approx 5$$

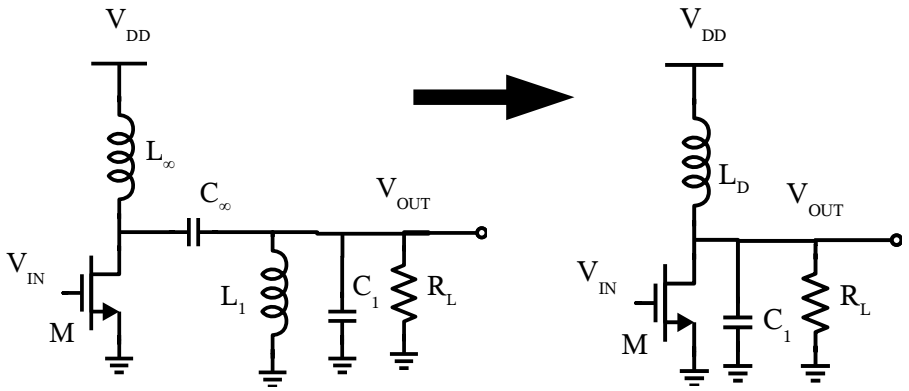
Use one (or two cascaded) lossless matching L networks

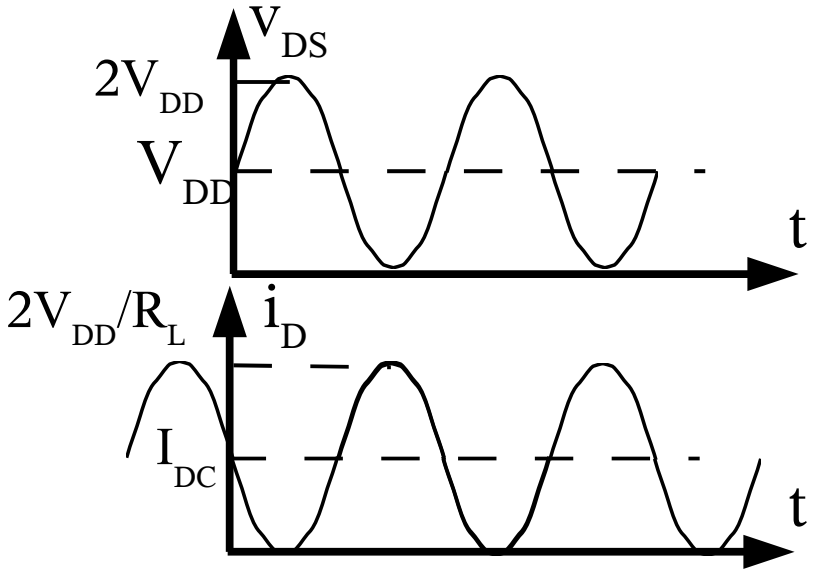
Class A voltage and current waveforms

$$Z_L(f_0)=R_L;Z_L(nf_0)=0$$

For n>1

$$\eta_{drain}=\frac{P_L}{P_{DC}}=\frac{\frac{(V_{DS}-V_{MIN})}{\sqrt{2}}\frac{(I_{DS}-I_{MIN})}{\sqrt{2}}}{V_{DS}\cdot I_{DS}}$$





Class B voltage and current waveforms

I_{MAX}, P_{OUT} and R_{LOPT} similar to class A, but conducts only for %50 of *T:*

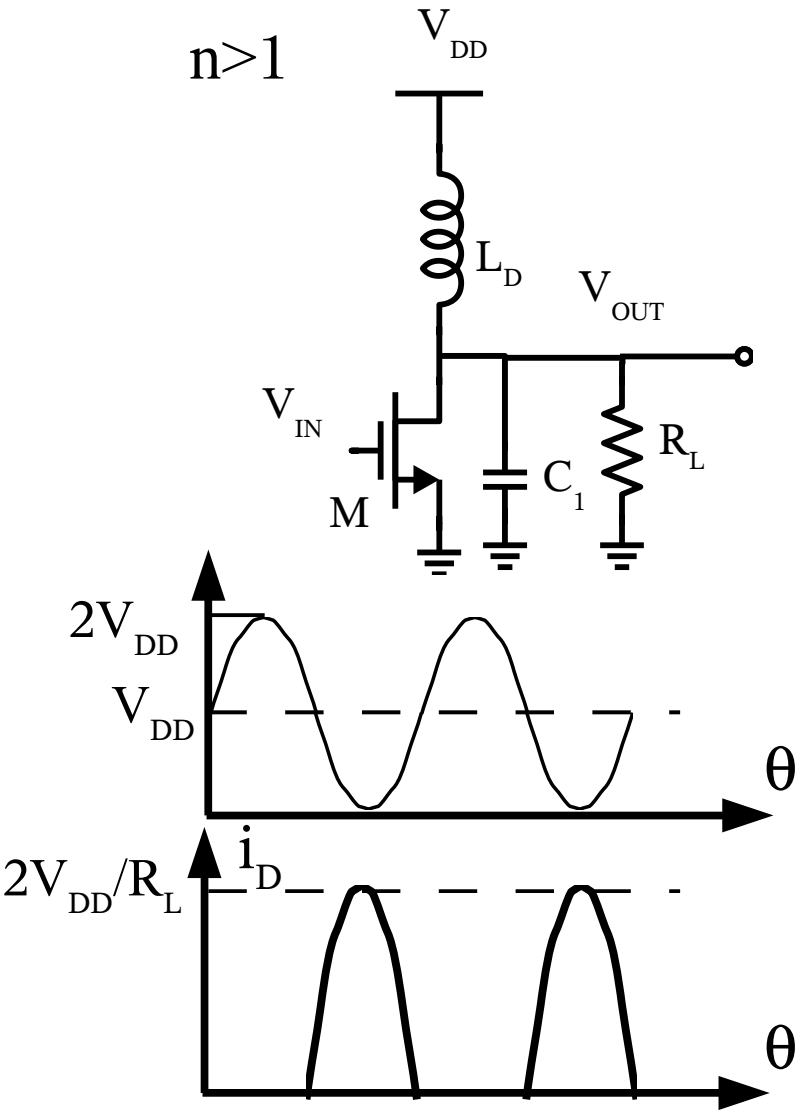
- g_m and *G* lower than class A.
- Highly nonlinear to increases PAE
- Maximum PAE= 78%.

$$I_{DC}=\frac{-I_{MAX}}{2\pi}\int_{\pi}^{2\pi}\sin\theta\,d\theta=\frac{I_{MAX}}{\pi}=\frac{2\cdot V_{DD}}{\pi\cdot R_L}$$

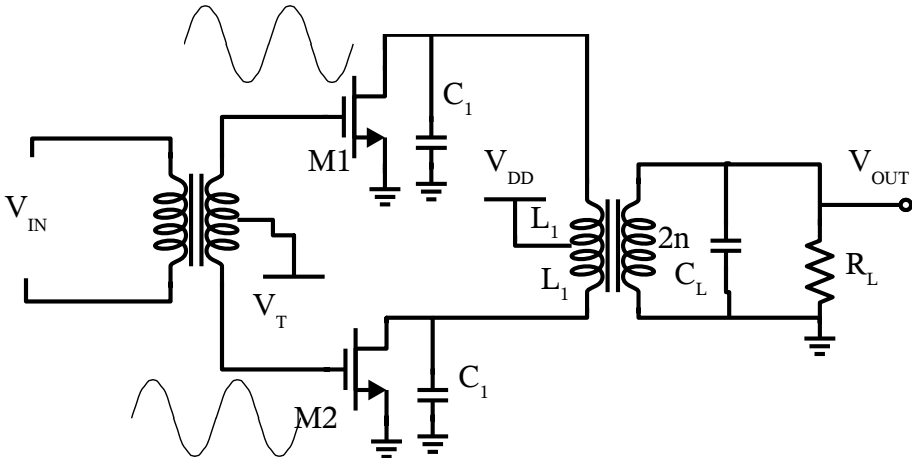
$$R_{LOPT}=\frac{V_1}{I_1}=\frac{V_{DD}}{\frac{I_{MAX}}{2}}=\frac{2V_{DD}}{I_{MAX}}=\frac{V_{MAX}}{I_{MAX}}$$

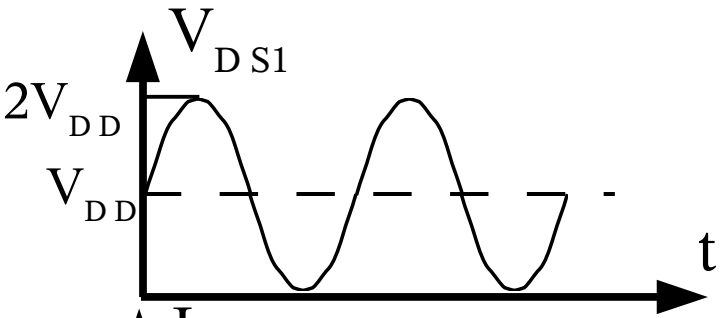
$$\eta_{drain}=\frac{P_L}{P_{DC}}=\frac{V_1\cdot I_1}{2\cdot I_{DC}\cdot V_{DD}}=\frac{V_{DD}\cdot\frac{I_{MAX}}{2}}{\frac{2\cdot V_{DD}\cdot I_{MAX}}{\pi}}=\frac{\pi}{4}$$

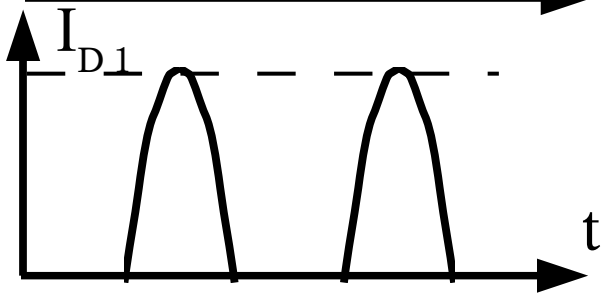
$$Z_L(f_0)=R_L;Z_L(nf_0)=0$$

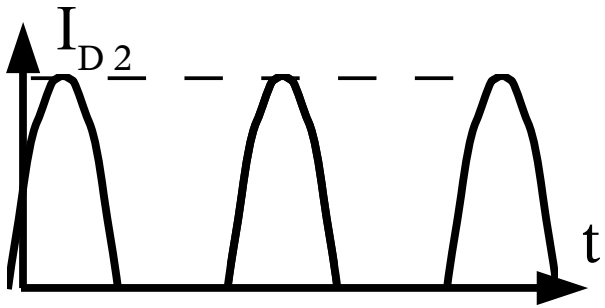


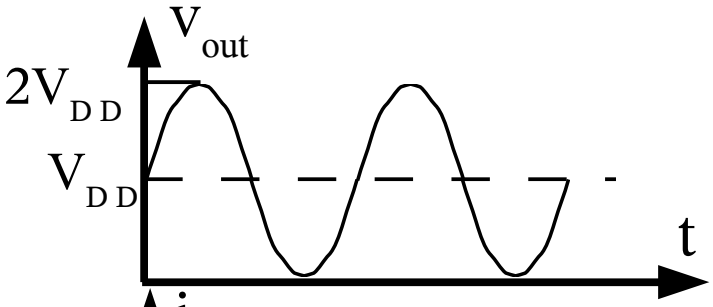
Push-pull class B voltage and current waveforms

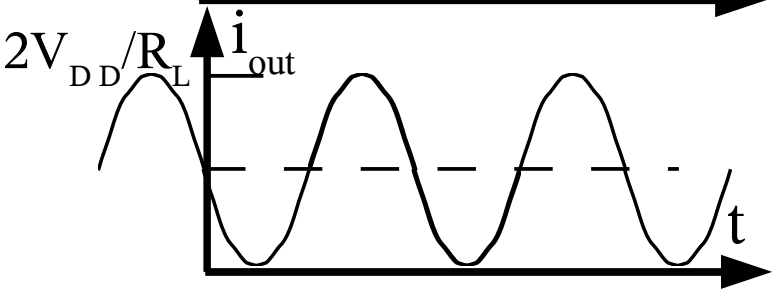












Class AB PA

- Workhorse (still) of the PA industry
- Reaches a compromise between the linearity of the class A and the efficiency of the class B power amplifiers.
- Current waveforms are a train of “chopped” sinusoids

$$i_D(t) = I_{DC} + I_p \sin(\omega t) \text{ for } \omega t \le \frac{3\pi}{2} - \frac{\theta_{off}}{2}$$

$$i_D(t) = 0 \text{ for } \frac{3\pi}{2} - \frac{\theta_{off}}{2} \le \omega t \le \frac{3\pi}{2} + \frac{\theta_{off}}{2}$$

$$i_D(t) = I_{DC} + I_p \sin(\omega t) \text{ for } \omega t \ge \frac{3\pi}{2} + \frac{\theta_{off}}{2}$$

Class AB equations

- I_{DC} = drain bias current when P_{in} =0,

$$I_{DC}+I_p\sin\left(\pi+\frac{\pi-\theta_{off}}{2}\right)=0$$

- I_p is amplitude of sinusoid

Angle of cutoff conduction θ_{off}

$$\theta_{off}=2\cos^{-1}\left(\frac{I_{DC}}{I_p}\right)$$

- DC component of current $I_{DC}=I_p\left\{\cos\left(\frac{\theta_{off}}{2}\right)+\frac{1}{\pi}\left[\sin\left(\frac{\theta_{off}}{2}\right)-\left(\frac{\theta_{off}}{2}\right)\cos\left(\frac{\theta_{off}}{2}\right)\right]\right\}$

- Fundamental component of current $I_1=I_p\left\{1-\frac{1}{2\pi}\left[\theta_{off}-\sin(\theta_{off})\right]\right\}$

$$R_{LOPT}=\frac{V_{DS}-V_{MIN}}{I_1}$$

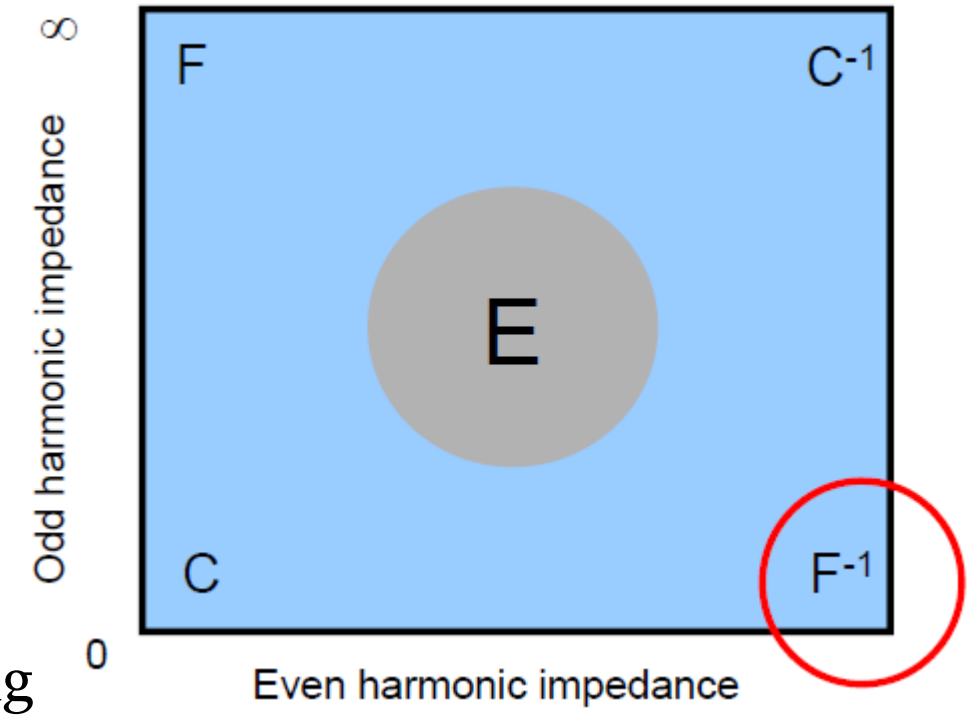
$$\eta_{drain}=\frac{1}{2}\frac{1-\frac{1}{2\pi}\left[\theta_{off}-\sin(\theta_{off})\right]}{\cos\left(\frac{\theta_{off}}{2}\right)+\frac{1}{\pi}\left[\sin\left(\frac{\theta_{off}}{2}\right)-\frac{\theta_{off}}{2}\cos\left(\frac{\theta_{off}}{2}\right)\right]}\left(\frac{V_{DD}-V_{MIN}}{V_{DD}}\right)$$

Switching-mode PAs

Switching mode PAs minimize power in the transistor by avoiding overlap between current and voltage waveforms

Examples: Class D, E, F, F^{-1}

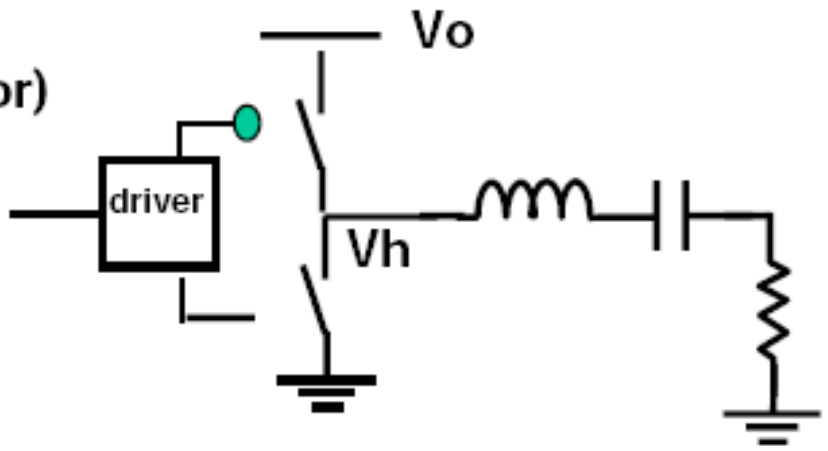
But require special linearization techniques

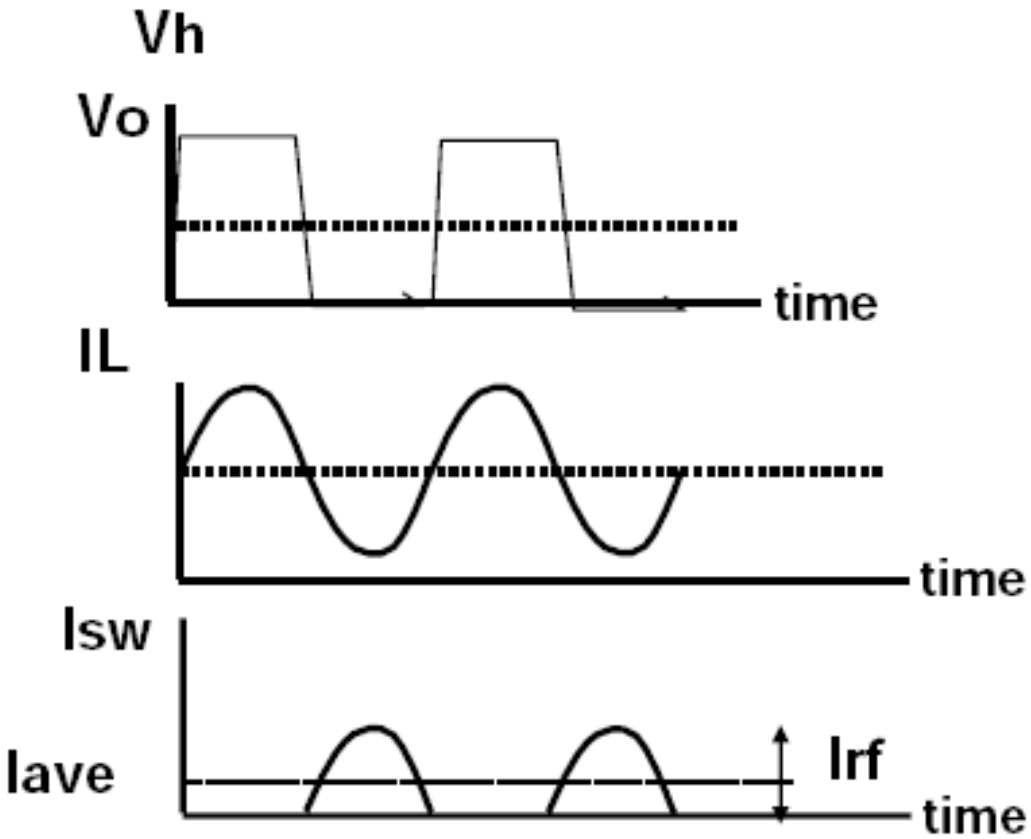


Courtesy of Stephen Long

Class D concept (T-P Hung et al. MTT Dec 2007)

Switches provide square wave voltage source
Nominally open circuit at all harmonics
(In reality, need to optimize for given transistor)





Problem:

Energy wasted in switch

$E = \frac{1}{2} (C_{out} V^2)$

Power loss is high: $E \times f$

But gaining popularity.

Asbeck 2004

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Class D CMOS INV implementation

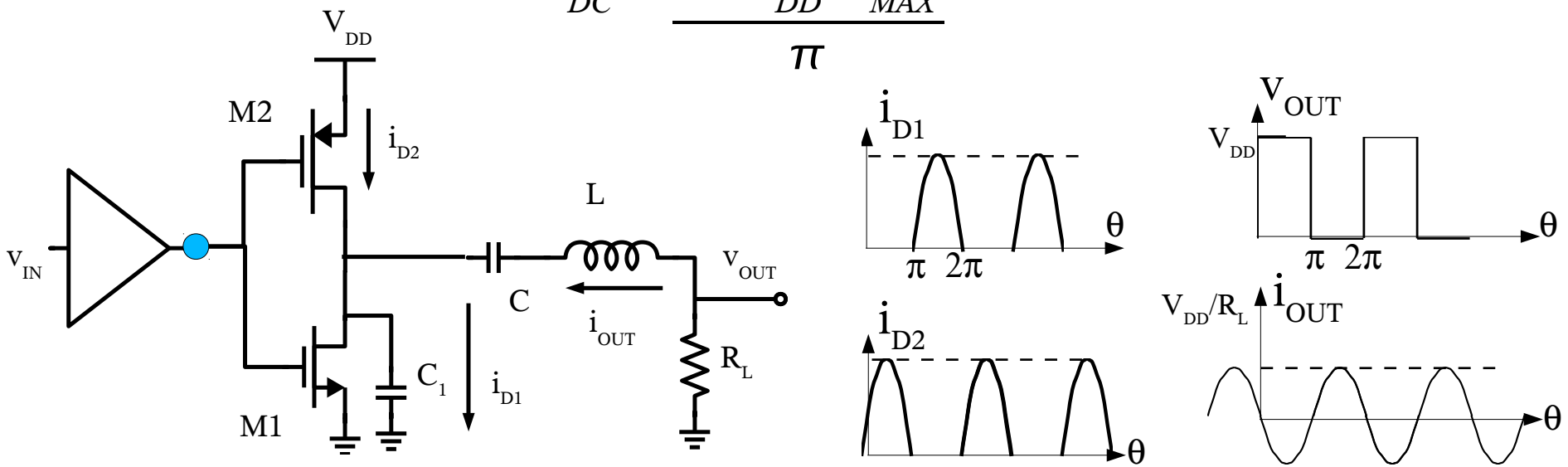
$$Z_L(f_0)=R_L;Z_L(nf_0)=\infty$$

$$V_1=\frac{1}{\pi}\int_{-\pi/2}^{\pi/2}V_{DD}\cdot\cos(\theta)\,d\theta=\frac{2V_{DD}}{\pi}=\frac{2V_{MAX}}{\pi}$$

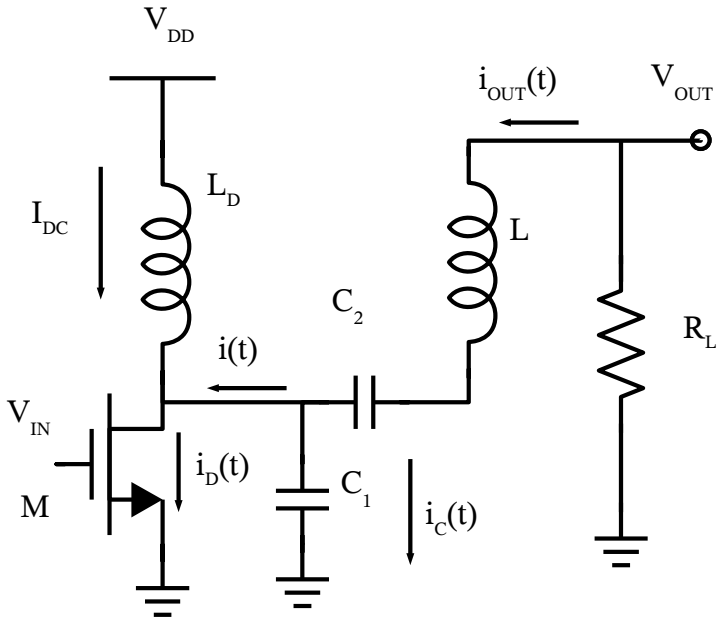
$$R_{LOPT}=\frac{V_1}{I_1}=\frac{2V_{MAX}}{\pi I_{MAX}}=\frac{2}{\pi}\frac{V_{DD}}{I_{MAX}}$$

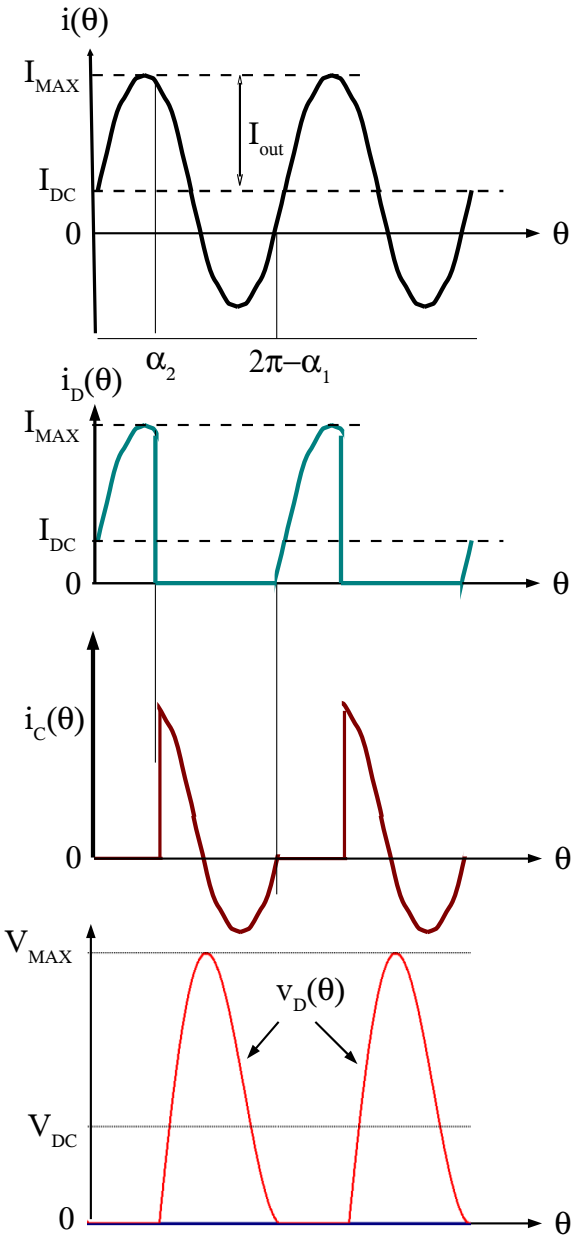
$$P_L=\frac{V_1 I_1}{2}=\frac{2V_{DD}I_{MAX}}{2\pi}=\frac{V_{DD}I_{MAX}}{\pi}$$

$$\eta=\frac{P_L}{P_{DC}}=\frac{V_{DD}\cdot I_{MAX}}{\frac{\pi\cdot V_{DD}\cdot I_{MAX}}{\pi}}=1$$



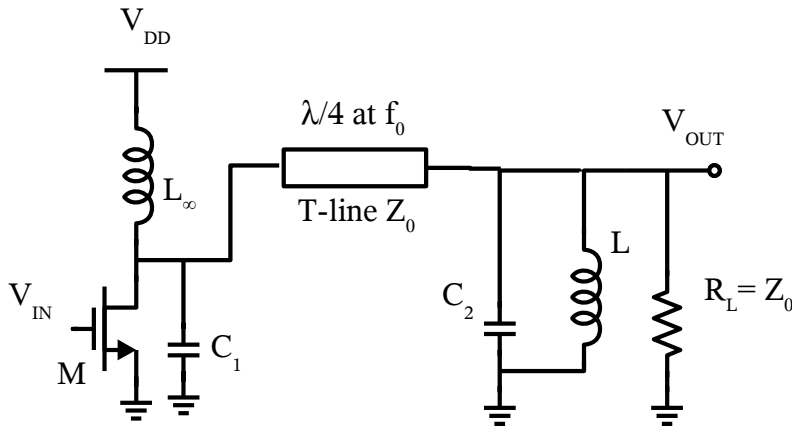
Class E concept

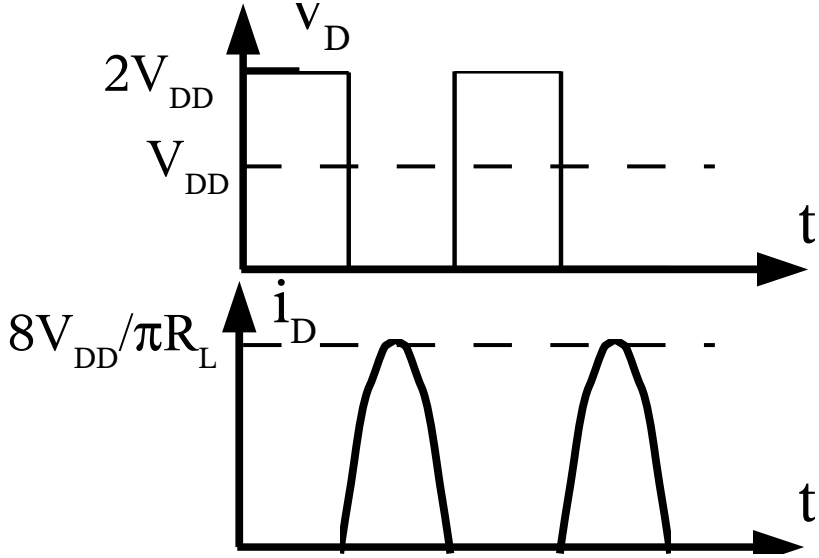




- V_{DS}=0 and dV_{DS}/dt=0 when switch closes,avoids ½ (CV^2f) loss
- dV_{DS}/dt=0 when switch closes makes operation insensitive to rise time of input signal
- $V_{MAX} = 3.6V_{DD}$, $I_{MAX} = 1.7V_{DD}/R_L$

Class F voltage and current waveforms

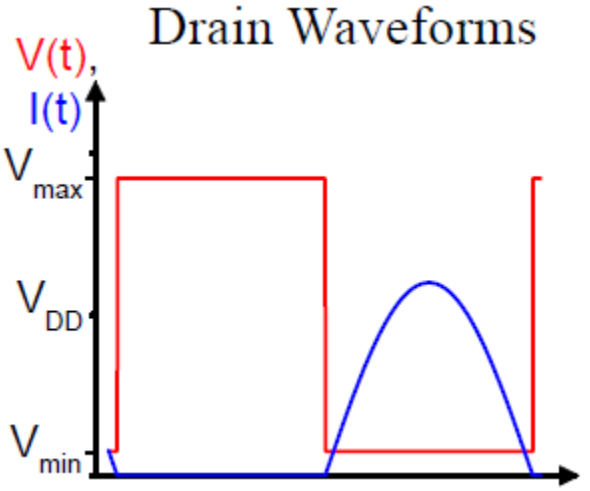




$$Z_L(f_0)=R_L;\ Z_L(2k\times f_0)=0;\ Z_L[(2k+1)\times f_0]=\infty$$

$$I_{DC}=\frac{I_{MAX}}{\pi} \qquad I_1=\frac{I_{MAX}}{2} \qquad V_1=\frac{4V_{DD}}{\pi}=\frac{2V_{MAX}}{\pi}$$

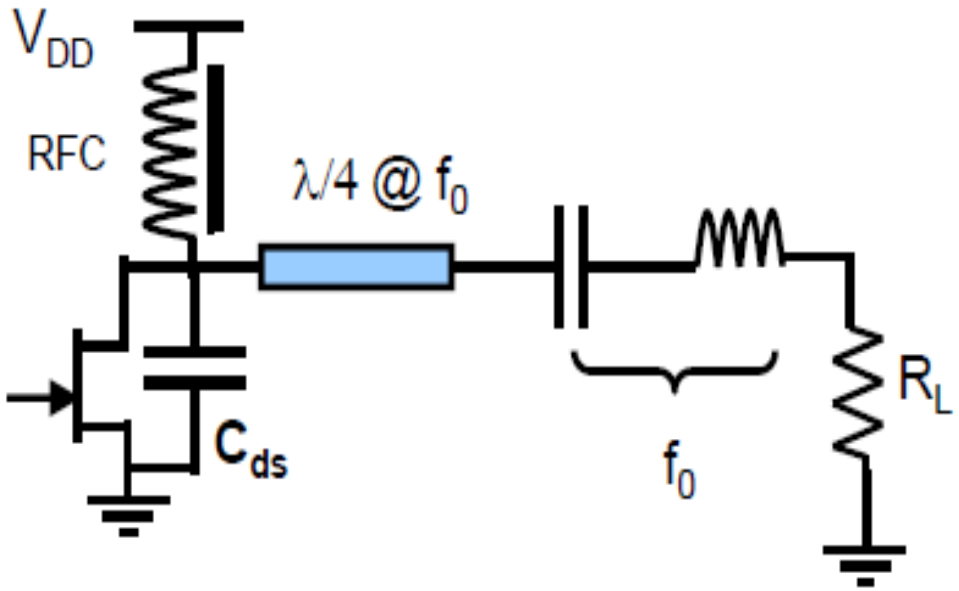
$$R_{LOPT}=\frac{V_1}{I_1}=\frac{4V_{MAX}}{\pi I_{MAX}}=\frac{8V_{DD}}{\pi^2 I_{DC}}$$

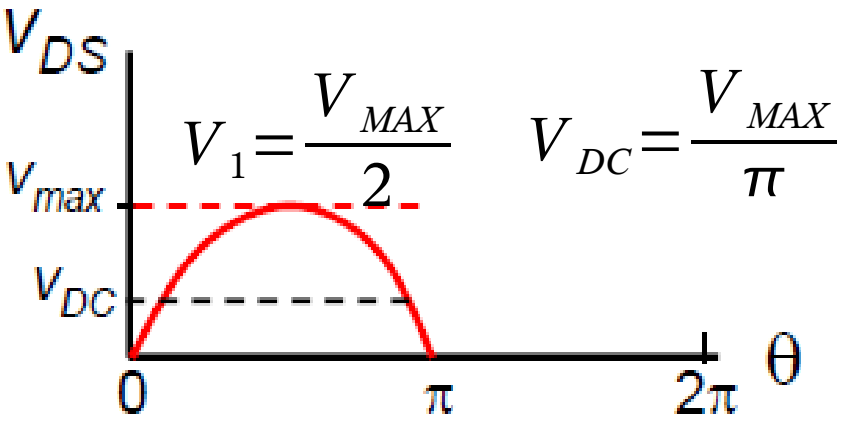


- Suffers from ½ (CV^2f) loss

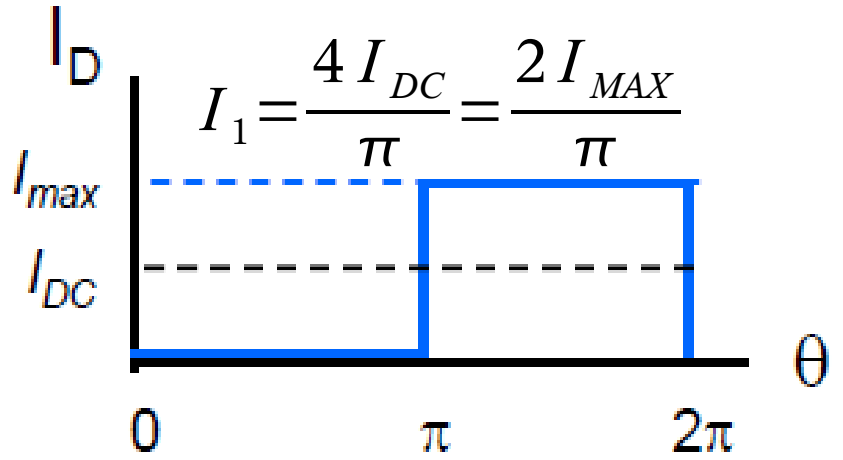
Inverse class F (F^{-1}) stage

$$Z_L(f_0)=R_L;\ Z_L(2k f_0)=\infty;\ Z_L[(2k+1)f_0]=0$$





$$V_1=\frac{V_{MAX}}{2} \qquad V_{DC}=\frac{V_{MAX}}{\pi}$$



$$I_1=\frac{4\,I_{DC}}{\pi}=\frac{2\,I_{MAX}}{\pi}$$

$$P_L=\frac{V_1 I_1}{2}=\frac{V_{MAX} I_{MAX}}{2\pi}$$

$$R_{LOPT}=\frac{V_1}{I_1}=\frac{\pi V_{MAX}}{4 I_{MAX}}=\frac{\pi^2 V_{DC}}{8 I_{DC}}$$

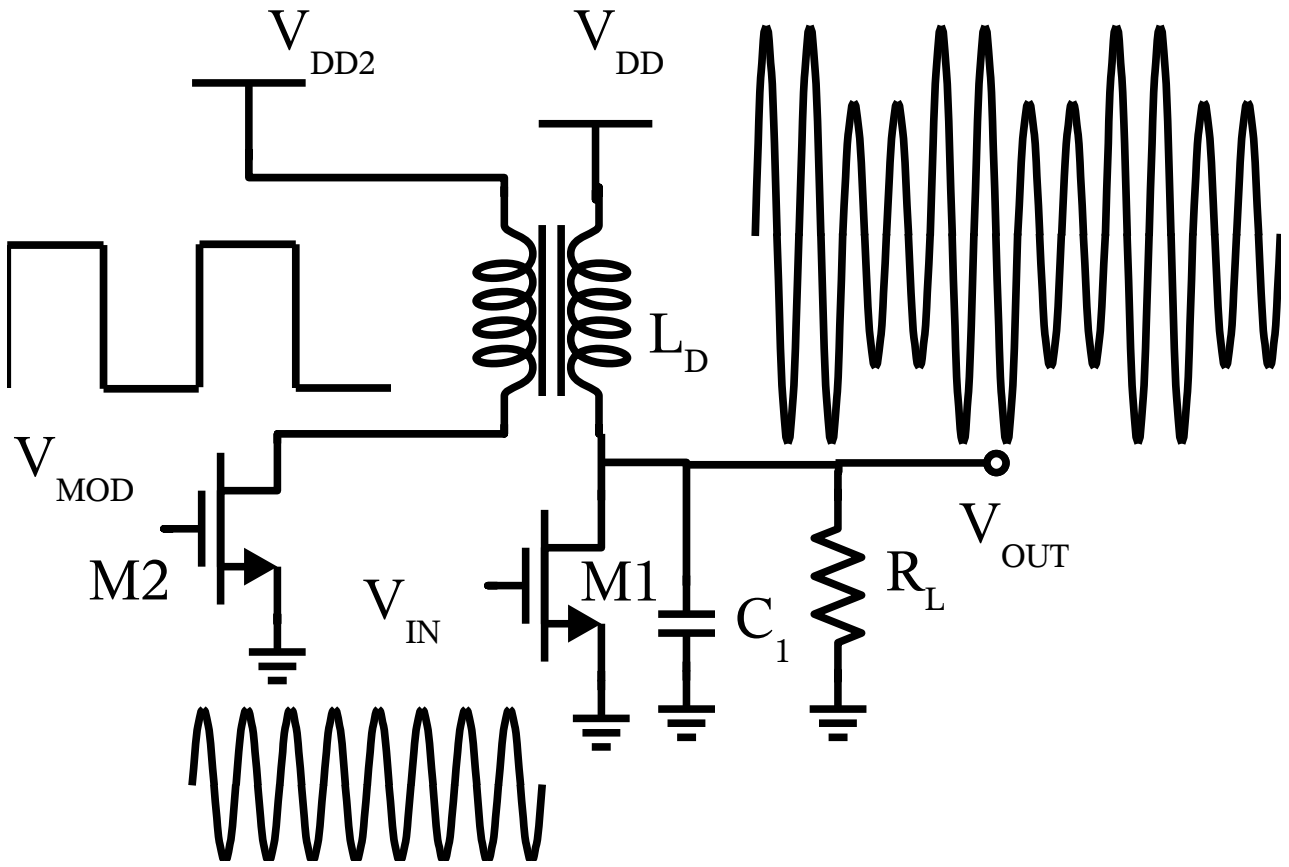
$$I_{DC}=\frac{I_{MAX}}{2}$$

Comparison of PA classes

param/class	A	B	D	E (one case)	F	F^{-1}
V_{DD}	$V_{MAX}/2$	$V_{MAX}/2$	V_{MAX}	$V_{MAX}/3.6$	$V_{MAX}/2$	V_{MAX}/π
I_{DC}	$I_{MAX}/2$	I_{MAX}/π	I_{MAX}/π	$I_{MAX}/2.06$	I_{MAX}/π	$I_{MAX}/2$
$P_L/V_{MAX}I_{MAX}$	0.13	0.13	0.16	0.16	0.16	0.16
R_{LOPT}	V_{MAX}/I_{MAX}	V_{MAX}/I_{MAX}	$2V_{MAX}/\pi I_{MAX}$	$1.075V_{MAX}/I_{MAX}$	$4V_{MAX}/\pi I_{MAX}$	$\pi V_{MAX}/4I_{MAX}$
η_d	50%	78%	100%	100%	100%	100%

Linear modulation of PAs

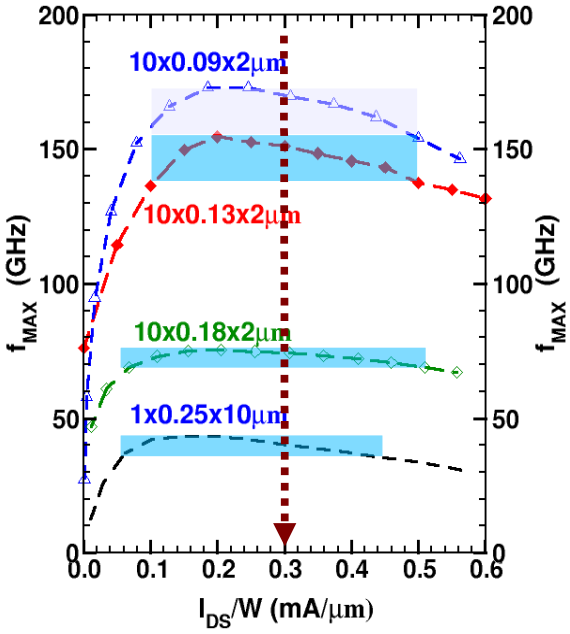
- Class A, B, AB: directly in the input signal
- Class C,D, E, F: separately from the carrier, typically through the supply node

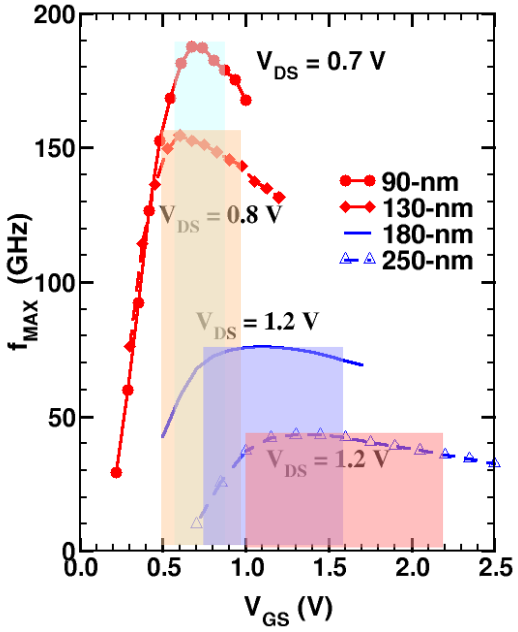


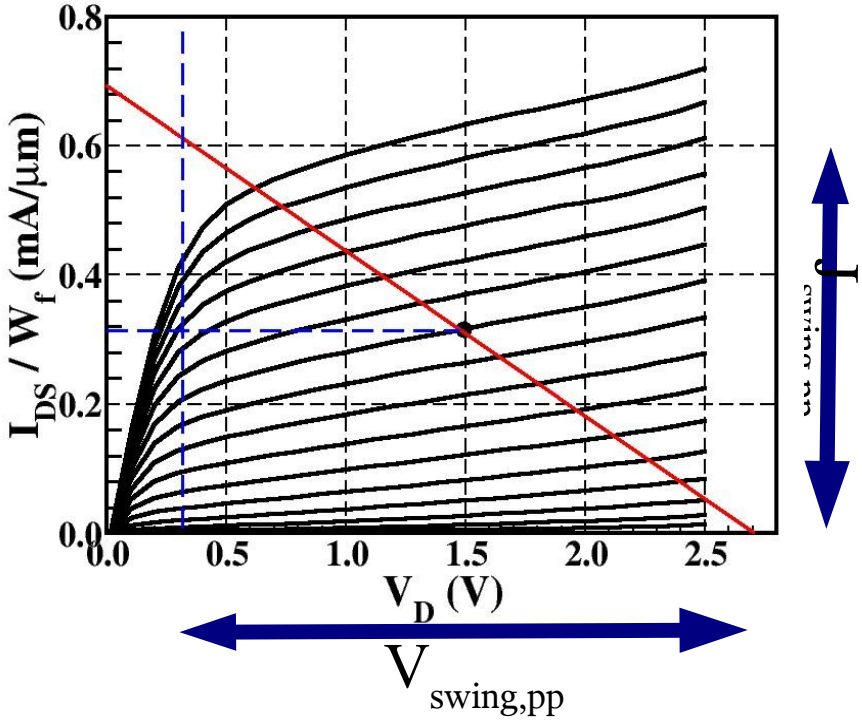
Class A FET PA Design Fundamentals

- Linear voltage swing at input/output decreases in each new node
- OP_{1dB} current swing $J_{swing,pp}$ is constant across nodes at about 0.4 mA/μm

$$OP_{1dB} = W \cdot J_{swing,pp} \frac{(V_D - V_{dsat})}{4} = W \cdot J_{swing,pp} \frac{(V_{MAX} - V_{dsat})}{8}$$







Class A PA Design Fundamentals (ii)

- P_{sat} current swing $J_{sat,pp}$ is about 0.6 $mA_{pp}/\mu m$ for n-FETs and $2J_{pfT}$ for HBTs
- P_{sat} voltage swing V_{satpp} is $2V_{DD} <= V_{MAX}$

$$P_{sat} = \frac{W \cdot J_{sat,pp} V_{DD}}{4} = \frac{W \cdot J_{sat,pp} V_{MAX}}{8}$$

Typical Class A PA Power Densities and R_{Lopt}

- 90/65nm CMOS
  - V_{MAX}=1.5V, $J_{sat,p}$=0.6mA/μm; P_{sat}=0.11mW/μm; R_{Lopt}=2.5kΩ× μm,
- 0.15μm GaN FET
  - V_{MAX}=40 V, J_{satpp}=1 mA/μm; P_{sat} =5 mW/μm; R_{Lopt}=40 kΩ× μm
- 50 GHz GaAs HBT
  - V_{MAX}=6 V, J_{satpp}=0.5 mA/μm; P_{sat} =0.375 mW/μm; R_{Lopt} = 12 kΩ× μm
- 230 GHz SiGe HBT
  - V_{MAX}= 3 V, $J_{at,pp}$= 3.9 mA/μm; P_{sat} = 1.5 mW/μm; R_{Lopt}=770 Ω× μm

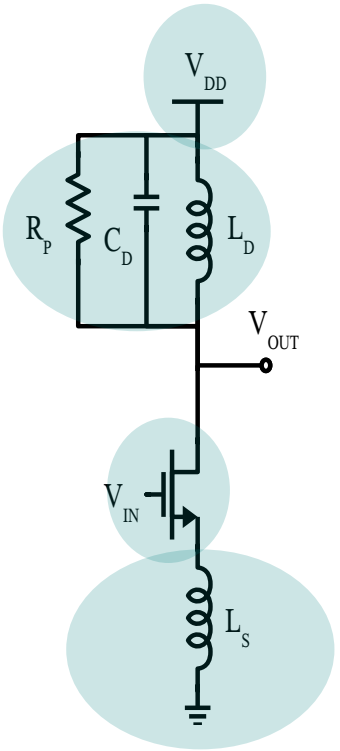
Example of 1W PA design (through 40 GHz)

- 90/65nm n-MOS: W= 9.09mm; R_{Lopt} = 0.27 Ω (impossible to match from 50Ω)
- 150nm GaN FET: W= 0.2mm; R_{Lopt} = 200 Ω (easy to match from 50Ω)
- 50GHz GaAs HBT: l_E= 2.66mm; R_{Lopt} = 4.5 Ω (possible to match from 50Ω)
- 230GHz SiGe HBT: l_E= 0.67mm; R_{Lopt} = 1.16 Ω (possible but difficult to match from 50Ω)

Conclusion: Need high voltage device for >1W

mm-Wave Class-A PA Design Methodology

Start with output stage



- Voltage Swing: $V_{swing} = V_{MAX} - V_{dsat}$,

$V_{DD} = V_{dsat}/2 + V_{MAX}/2$

- Bias Current Density: set J_p = 0.3 mA/μm for linearity
- Device Size: find *W* from OP_{1dB}, V_{swing}, I_{swing} = 0.4 mA/μm
- L_S: If $V_{swing}/MAG > V_{in,swing}$ add degeneration
- Output matching network (L_D, C_D)from V_{swing}/I_{swing} to 50 Ω
- Repeat steps for 2nd. last stage and scale W by 0.66 to 0.5
- Design input stage to match to 50 Ω and to maximize gain.

Ex: Output Stage with P_{1dB} = 10dBm at 60 GHz

Given: V_{DD} = 1.2V, $V_{DS,sat}$ = 0.3 V at 0.3mA/μm OP_{1dB} = 10dBm = 10 mW

$V_0 = V_{DD} - V_{DS,sat}$ = 0.9 V (1.8Vpp)

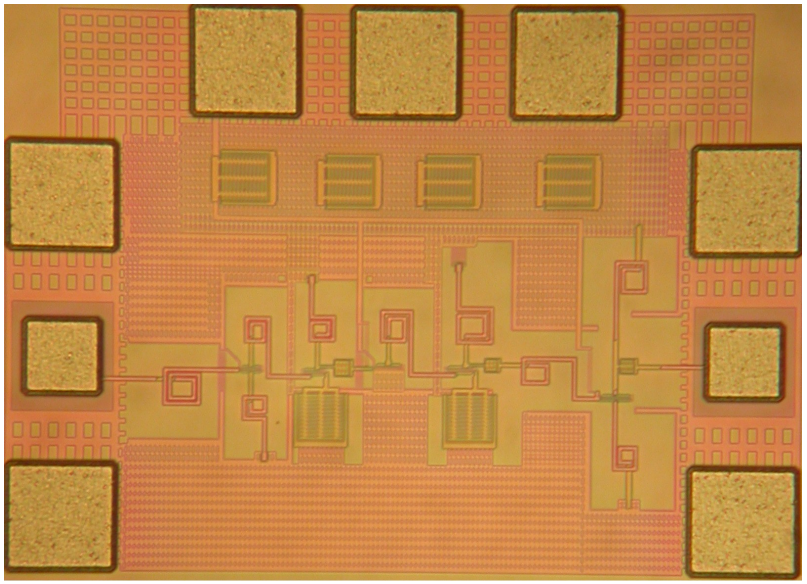
From OP_{1dB} = 10 mW = $V_0 \times I_{DC}/2$ => , I_O = 22 mA

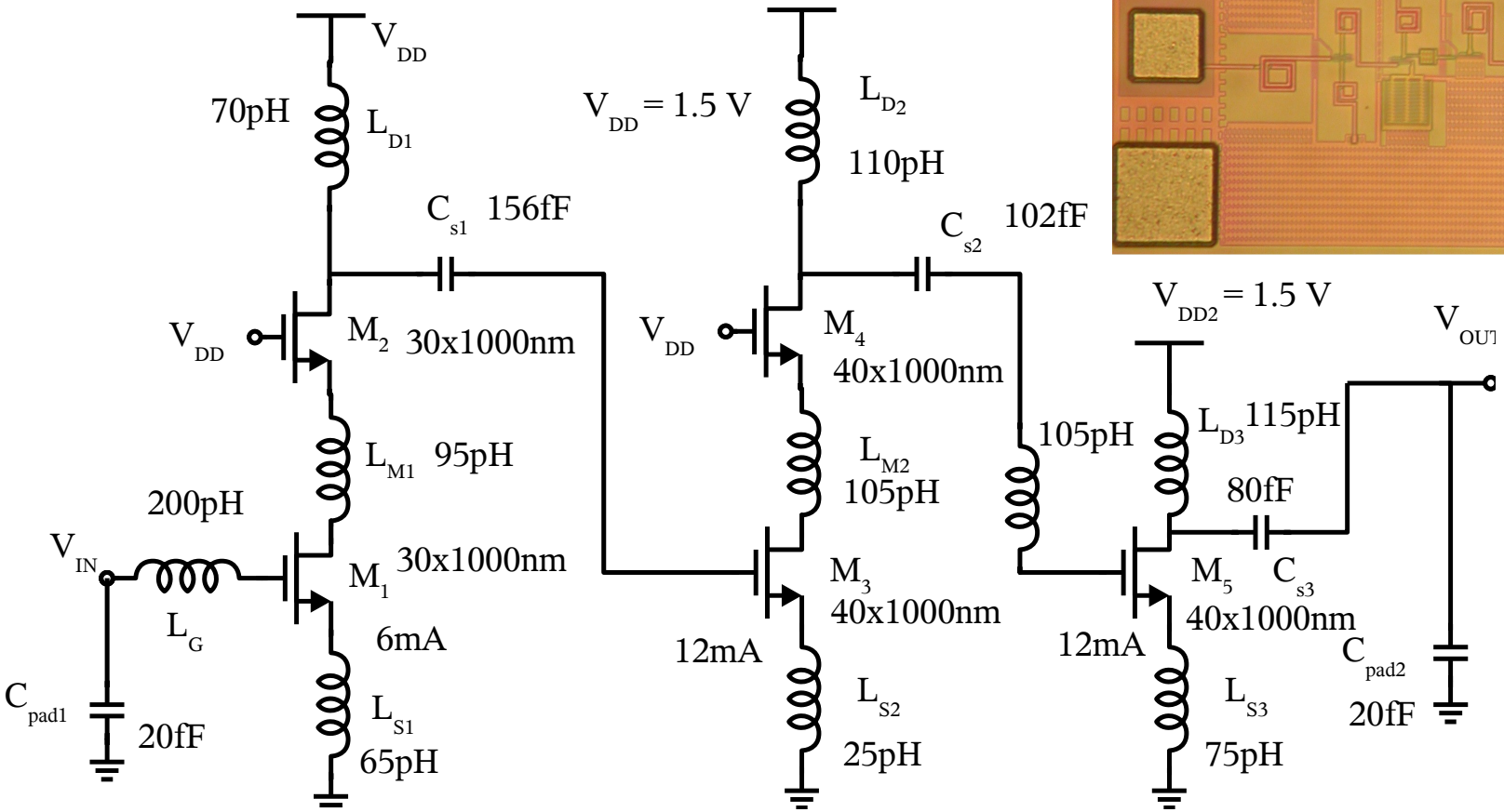
$W = I_{DC}/0.28mA/\mu m = 78\mu m$

$R_L = V_o/I_o = 900/22 = 41\ \Omega$

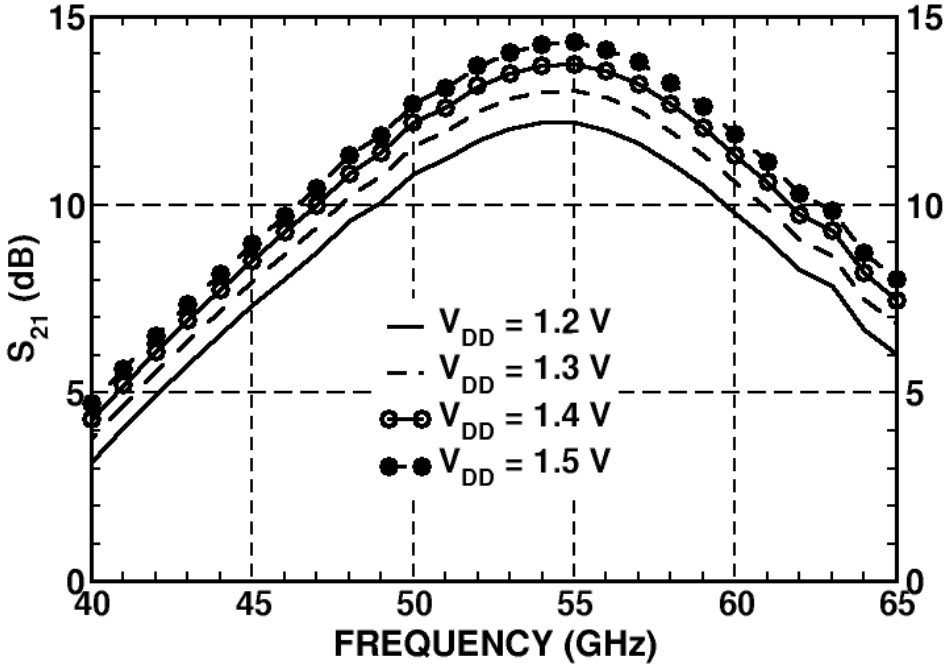
Since MAG @ 60 GHz is only 6 dB (voltage gain of 2), the swing at input of last stage is $1.8V_{pp}/2 = 0.9V_{pp} > 0.45V_{pp}$. We need degeneration, hence L_S.

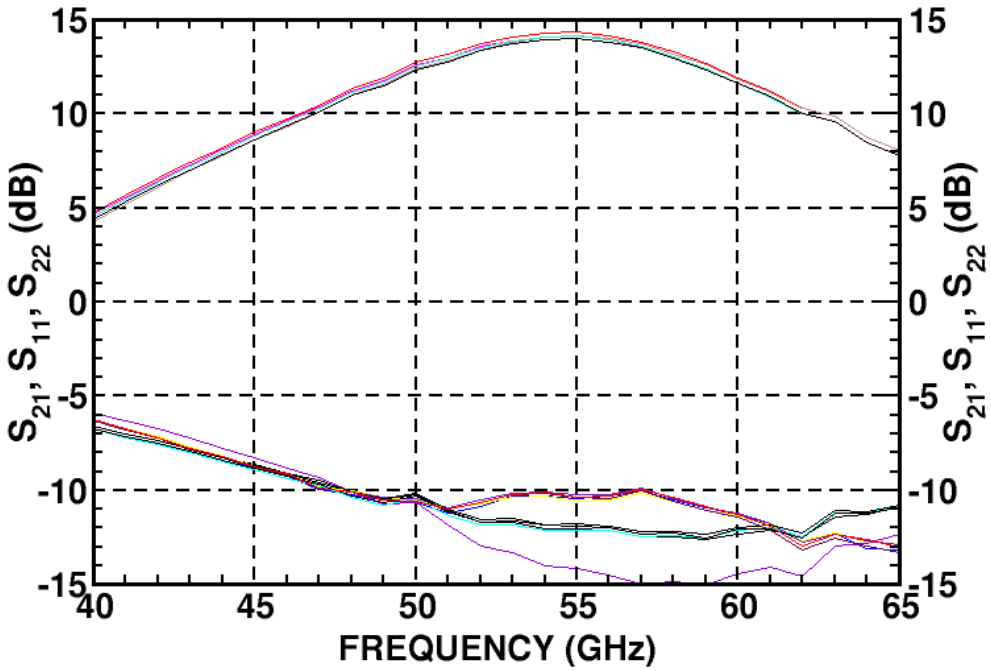
2-stage cascode + 1 CS stage PA in 90nm CMOS (M. Khanpour et al, CSICS-2007)



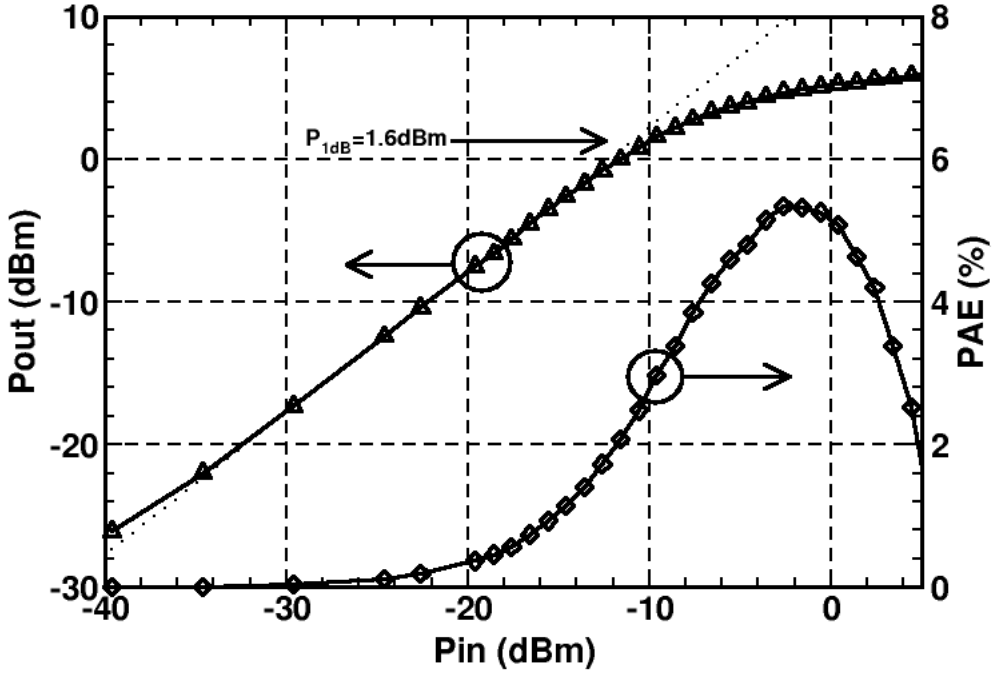


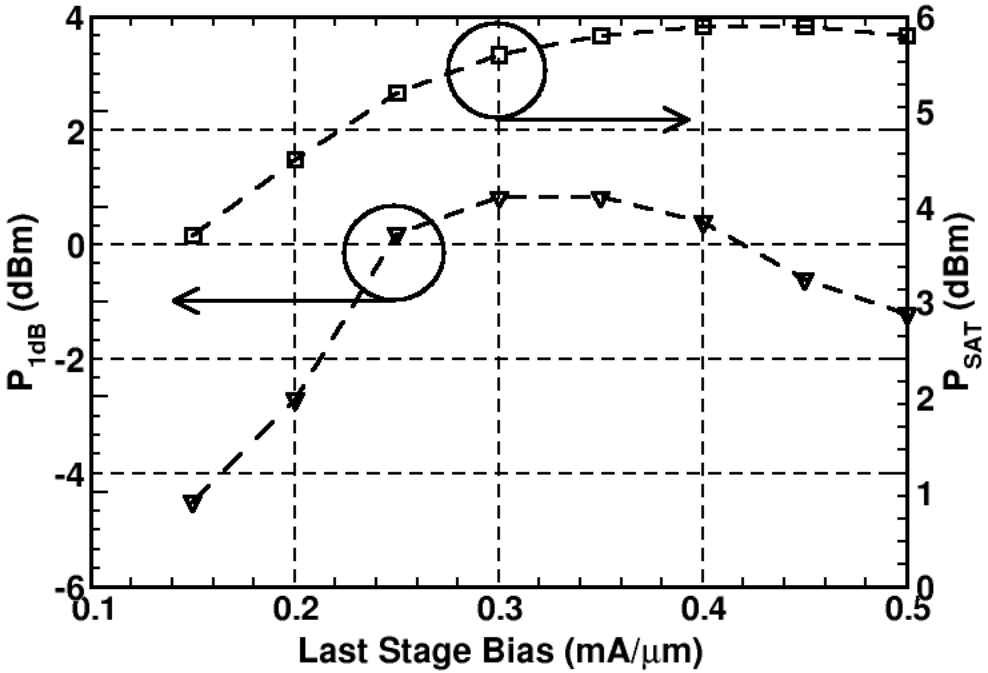
Measurements across dies and vs. supply voltage



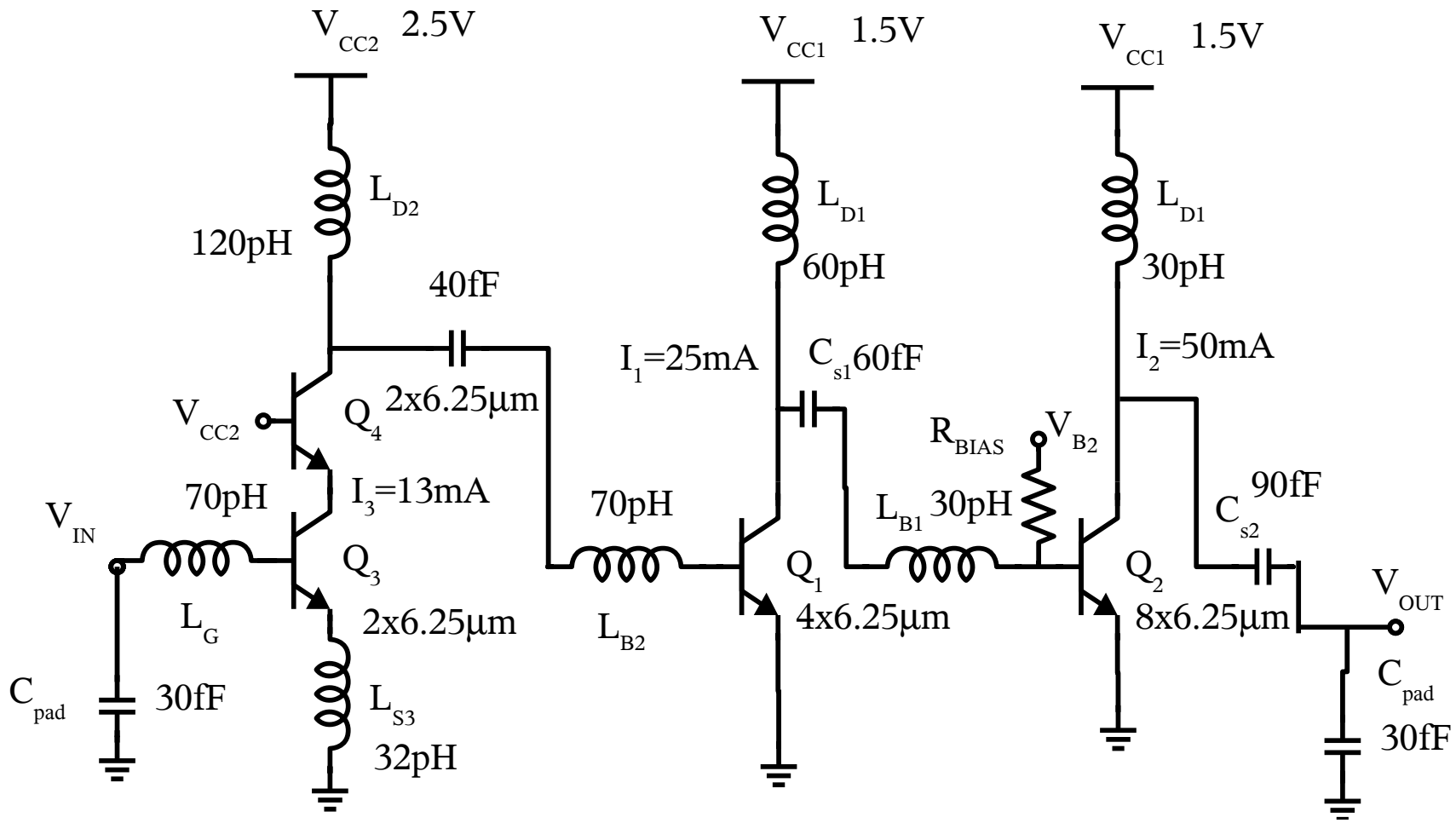


OP_{1dB}, PAE and P_{SAT} measurements



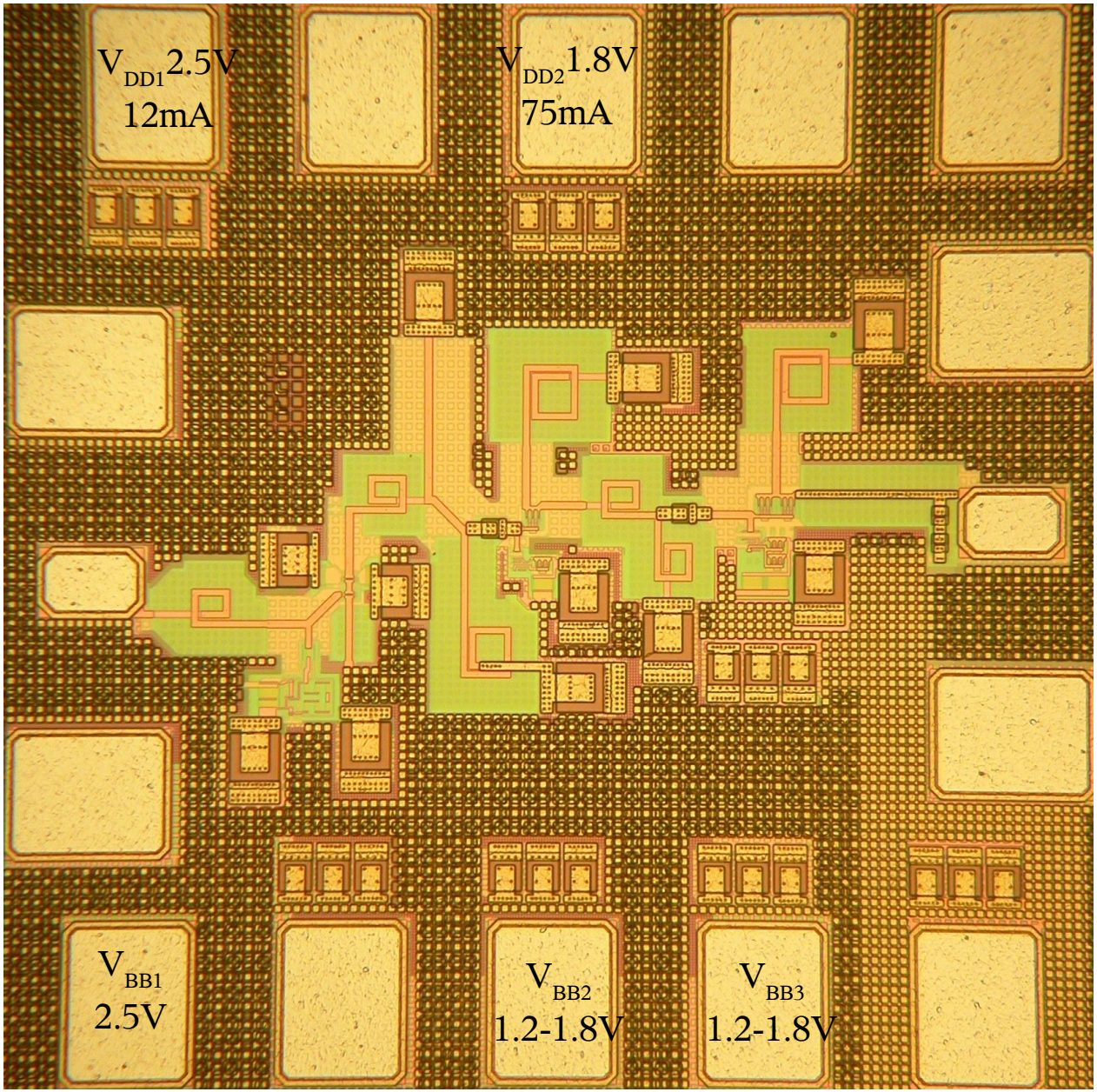


77GHz SiGe HBT PA (S. Nicolson et al. IMS-2007)

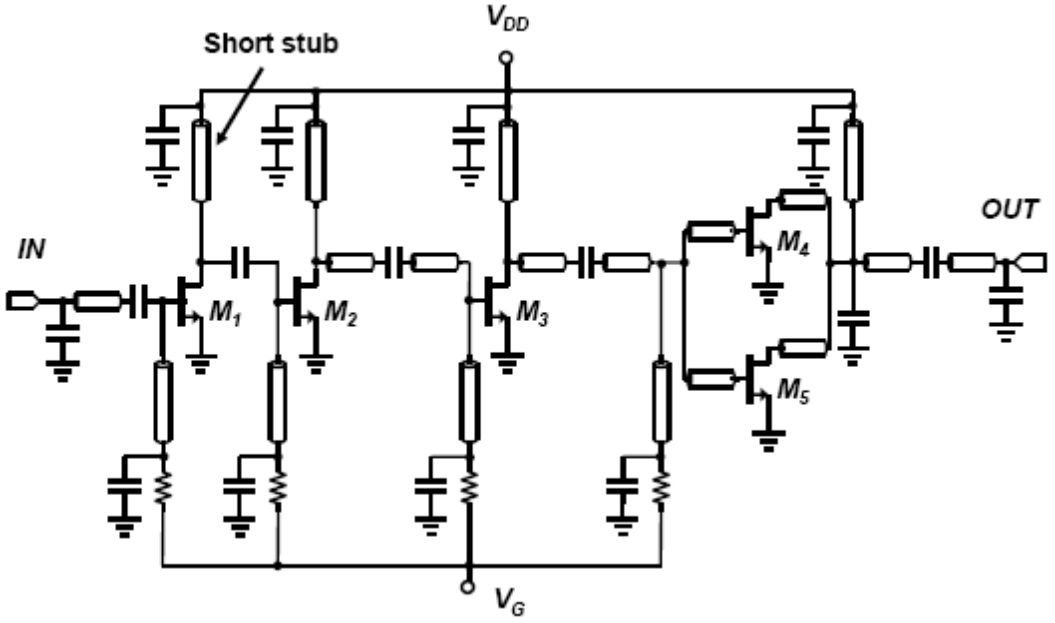


$$P_{sat} \le \frac{I_{DC} \cdot V_{CC1}}{2} = \frac{44mA \cdot 1.5V}{2} = 33\,mW = 15.2\,dBm$$

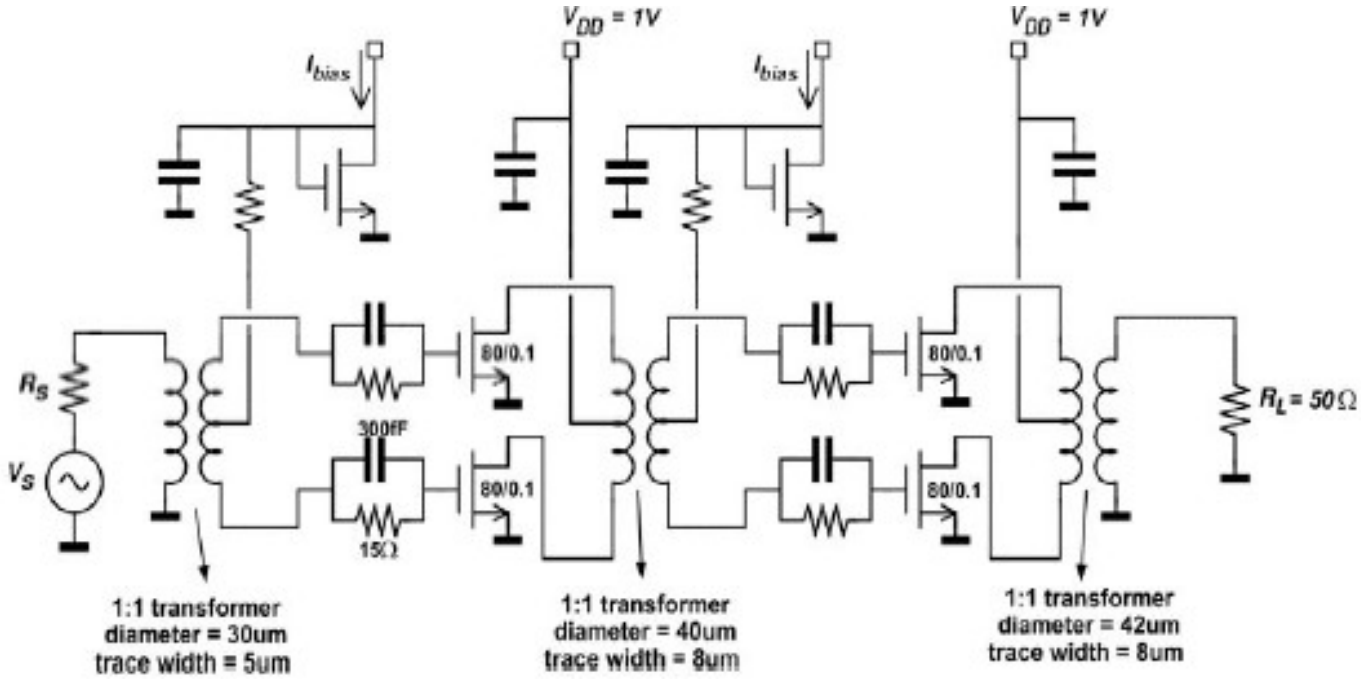
PA Layout



Other CS mm-wave CMOS PAs (ISSCC-2008)



- 77GHz CS PA (Fujitsu)
  - G=12dB, P_{sat}=7 dBm
- 50-60GHz CS PA (Berkeley)
  - G= 5.5dB, P_{sat} =12dBm



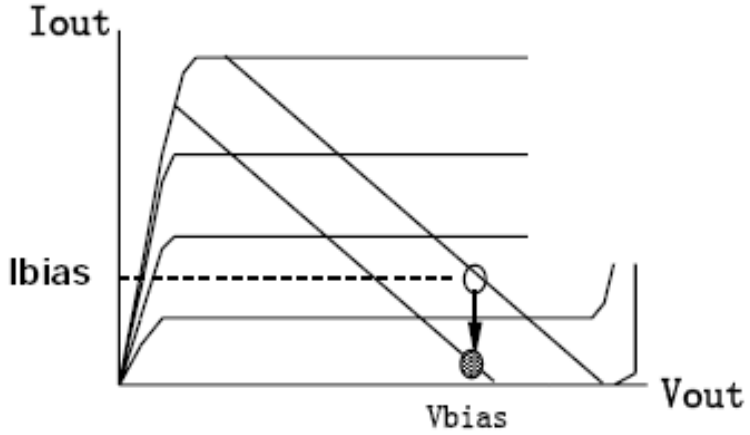
Efficiency Enhancement Techniques

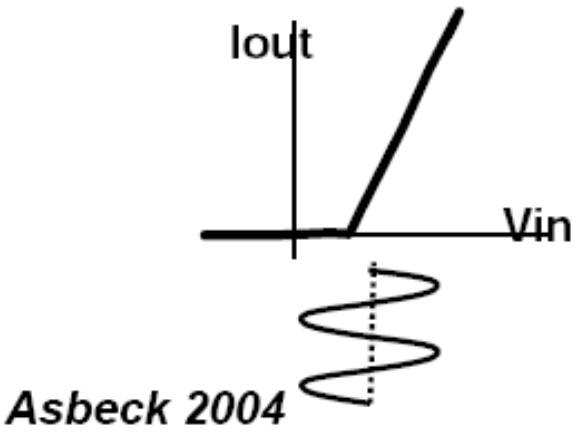
Dynamic biasing techniques (L. Larson, 2007)

Dynamic Current Biasing Amplifier

Strategy: Vary I_{dc} as signal level changes

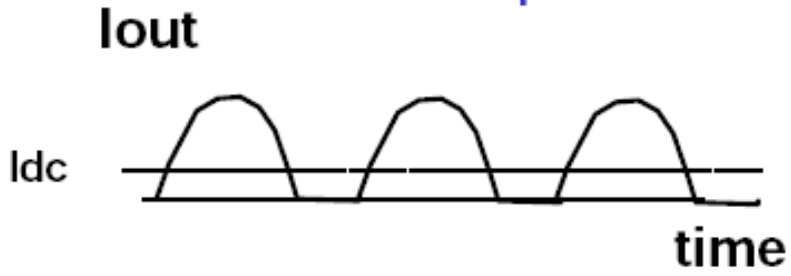
- Used by most amplifiers for wireless systems (to some extent)
- Significant benefit obtained automatically with Class AB operation





Asbeck 2004

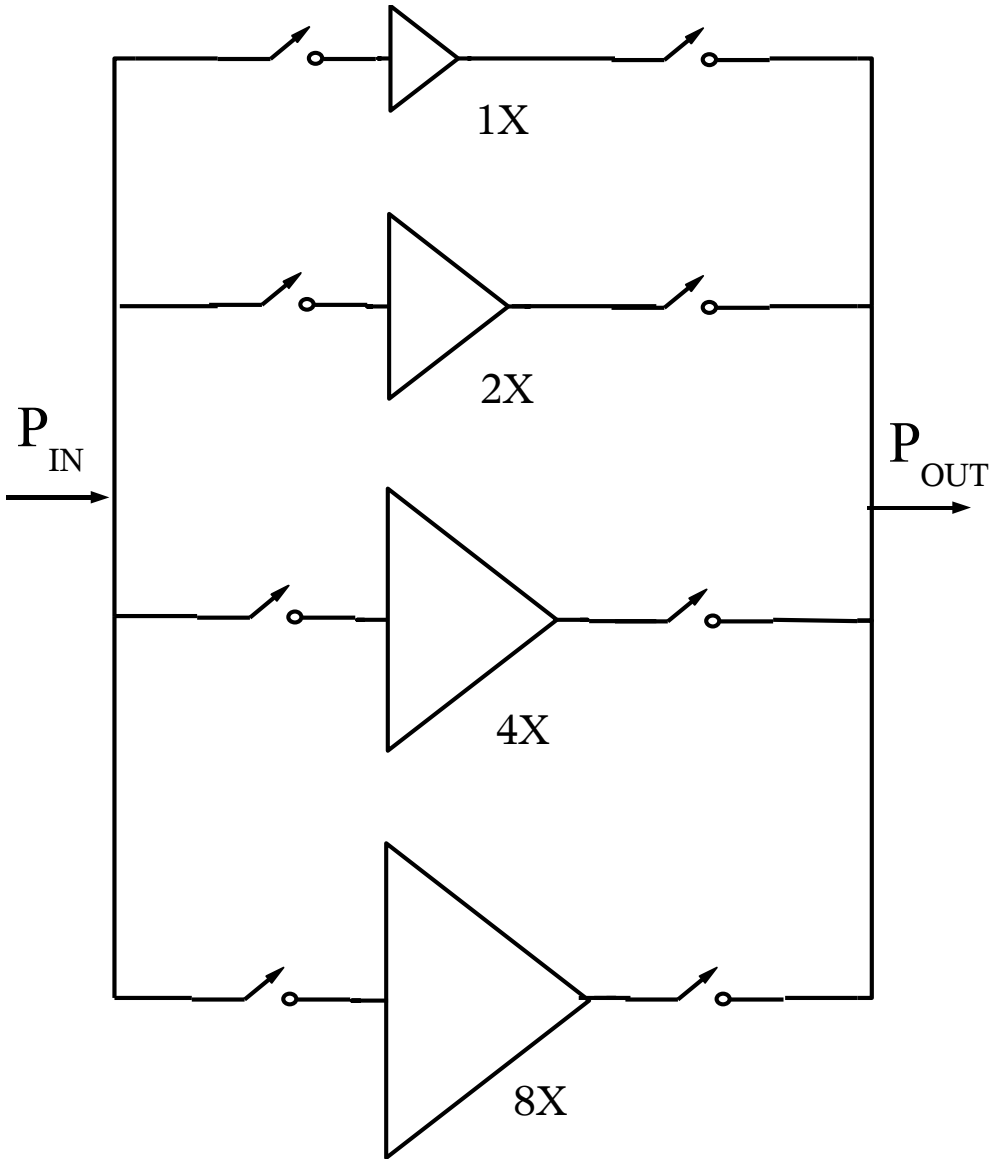
Class AB operation
asymmetric output waveform
has dc component



In Class B, Idc~ K Imax ~ sqrt (Pout)

PA subranging

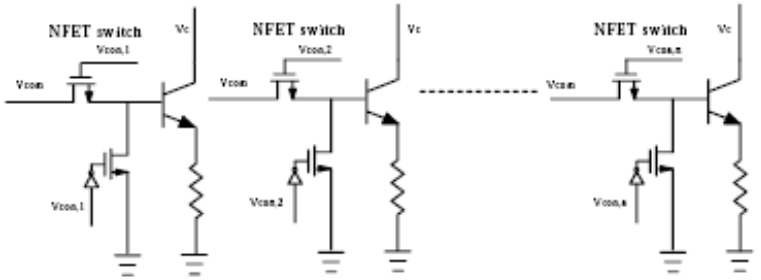
- Optimally biased for efficiency (binary-weighted) PA sections are switched in and out as needed by the transmitter
- But R_{LOPT} changes with number of switched on stages

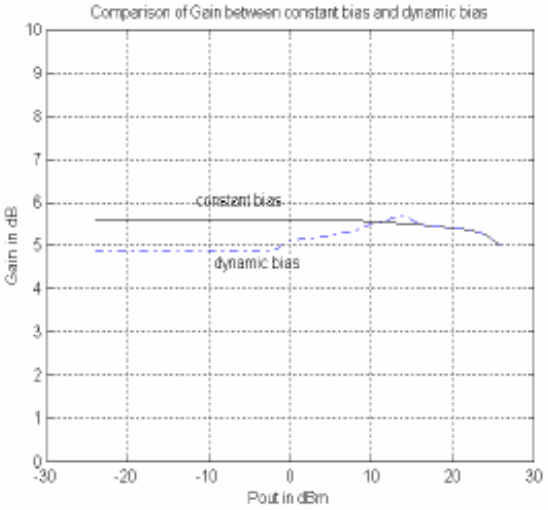


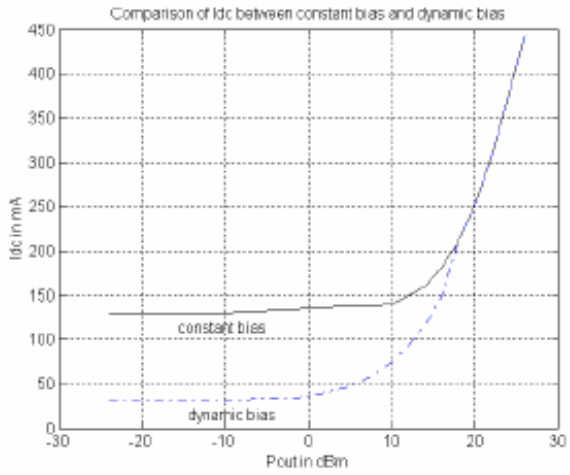
HBT example: (L. Larson, 2007)

Maintaining Constant Gain Over Wide Range of DC Bias

Si/SiGe HBT BiCMOS WCDMA Power Amplifiers With Dynamic Biasing and Reconfiguration Via MOSFET Switches







By selecting number of HBT fingers, the input and output load capacitance can be varied with power level, keeping gain nearly constant

Deng, 2004

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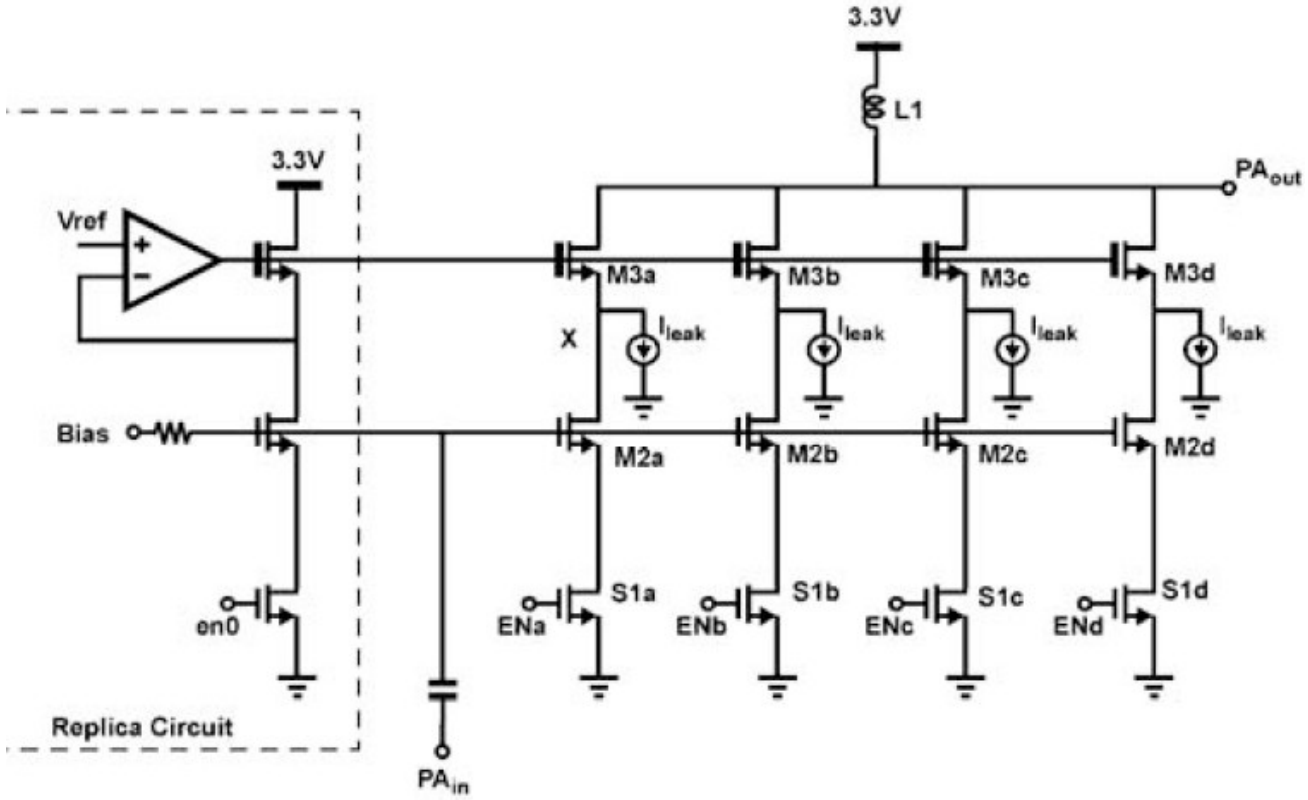
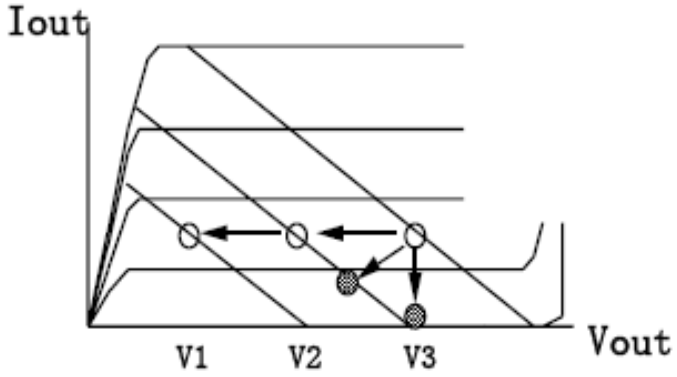
5GHz digitally-controlled class A WLAN PAs (Atheros, ISSCC-2008)

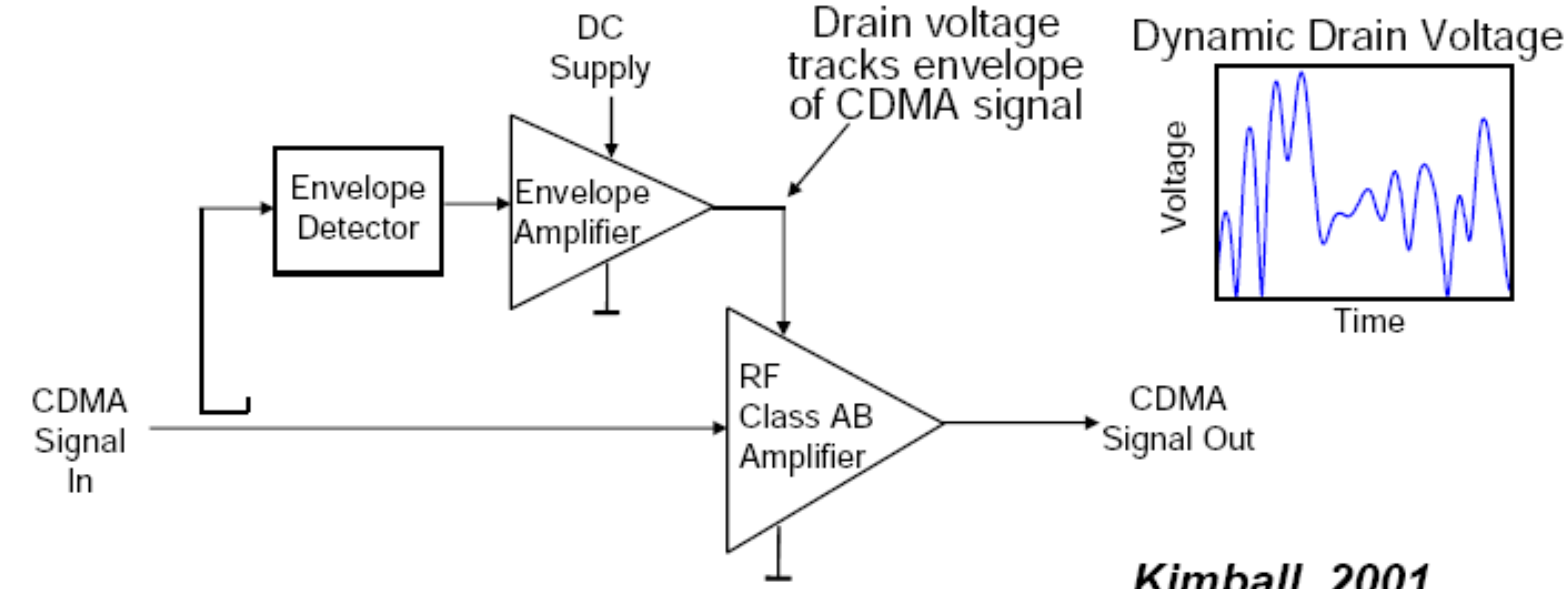


- 4-bit control, digitally-programmable output power level 10mW
- Thick gate oxide common-gate device for reliability
- Replica bias and I_{leak} to avoid overstress of the thin-oxide CS device

Envelope tracking technique (L.Larson 2007)



- Maximizes PA efficiency by keeping RF transistor closer to saturation for all envelope amplitudes
- Envelope Amplifier provides dynamic drain voltage



Kimball, 2001

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In Envelope Tracking, PA is Class AB.
Input signal contains envelope and phase information.

2GHz PA with pulse-width modulation and ER
(TI -2005, Univ. of Washington ISSCC-2008)

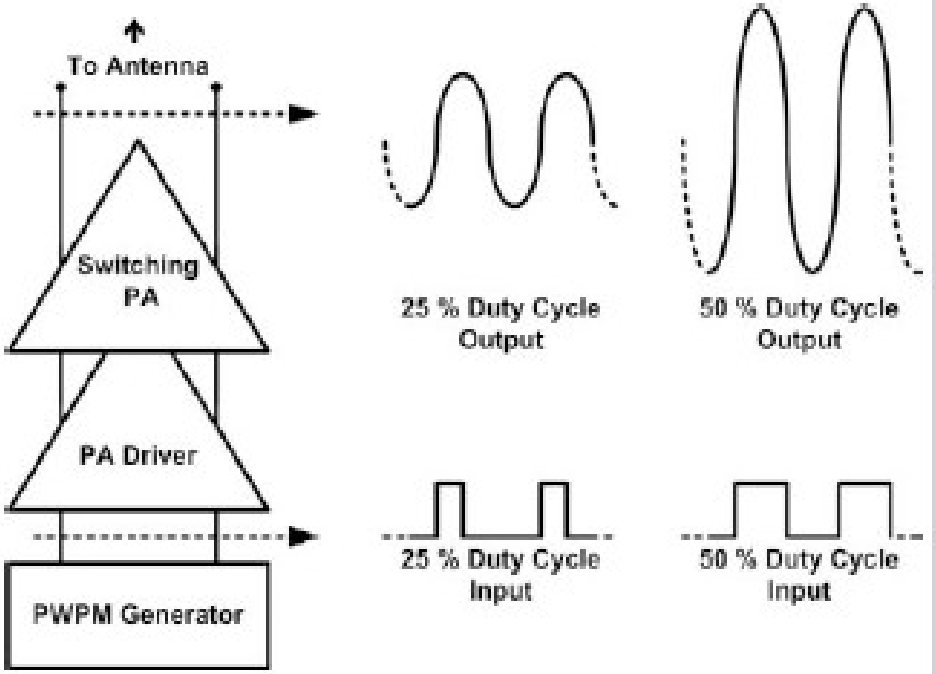


Figure 31.5.1: Generalized PWPM PA.

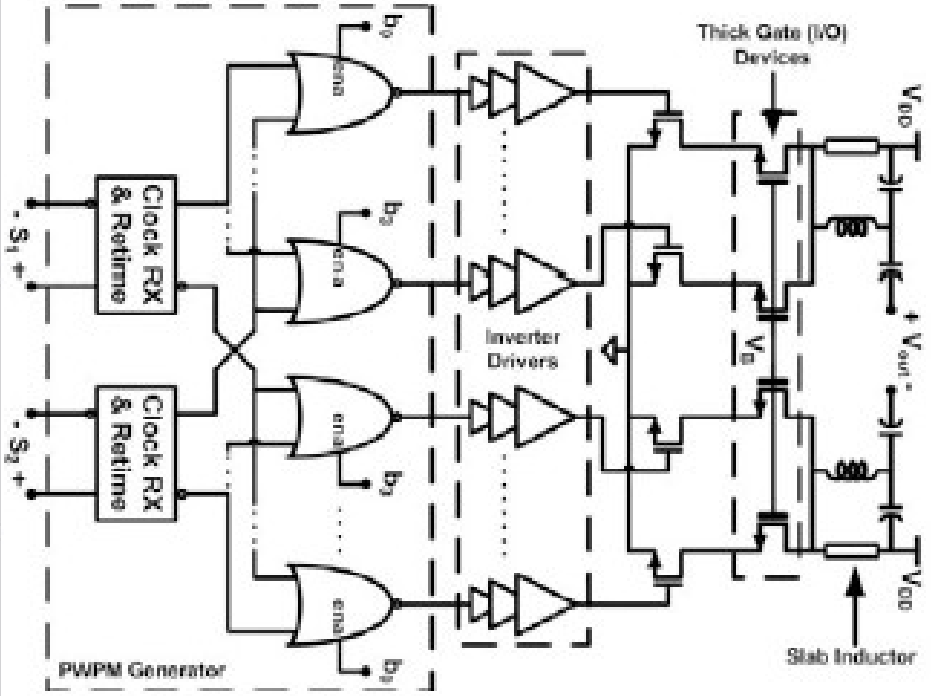
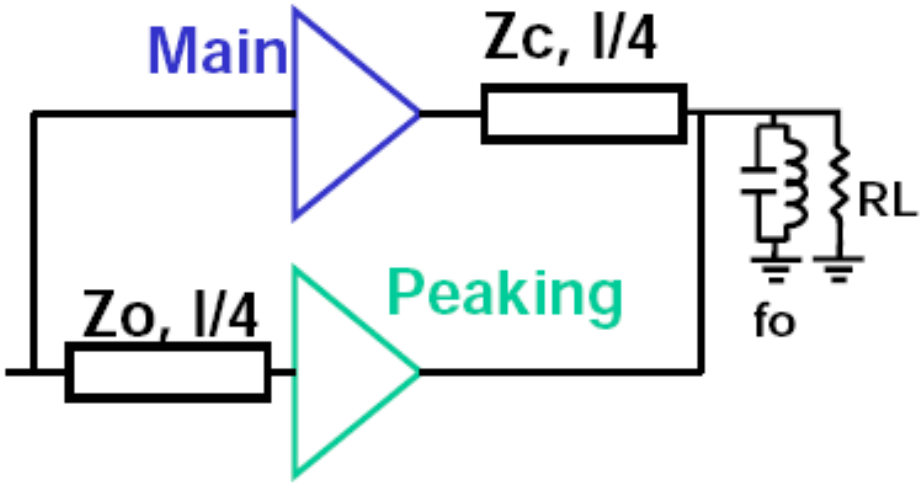


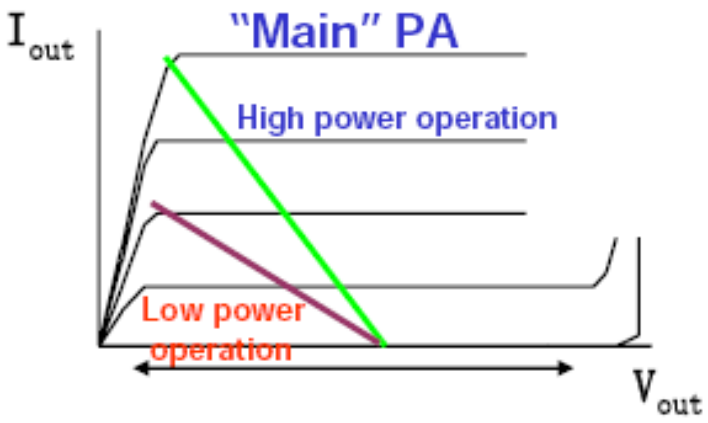
Figure 31.5.2: Schematic of the Class-E PWPM PA.

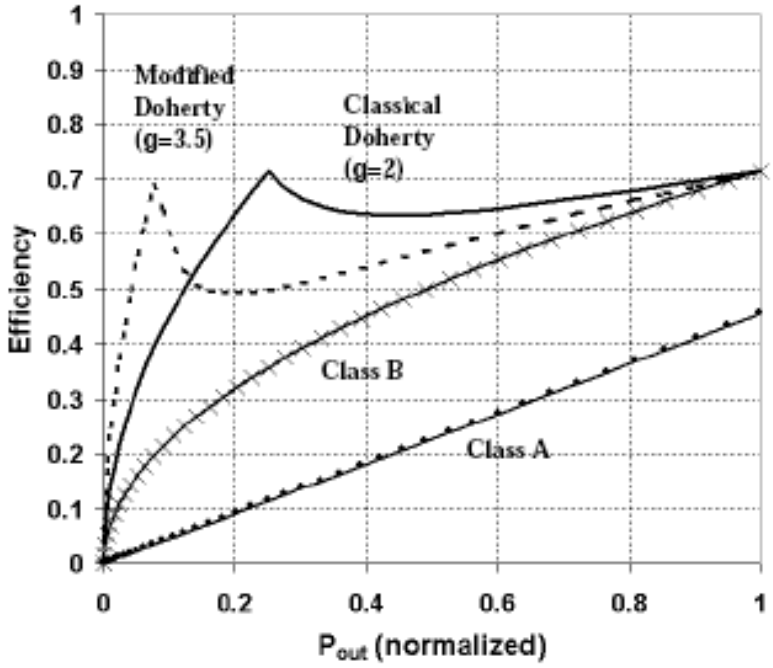
- Envelope restoration => Amplitude information is coded in the pulse width
- Pure digital signal applied at PA gate => sinusoidal output
- Output power is controlled by 4 bits

Doherty amplifier (L.Larson 2007)

Uses two coupled amplifiers
Peaking amplifier acts as "active load" for main amplifier







Asbeck 2004

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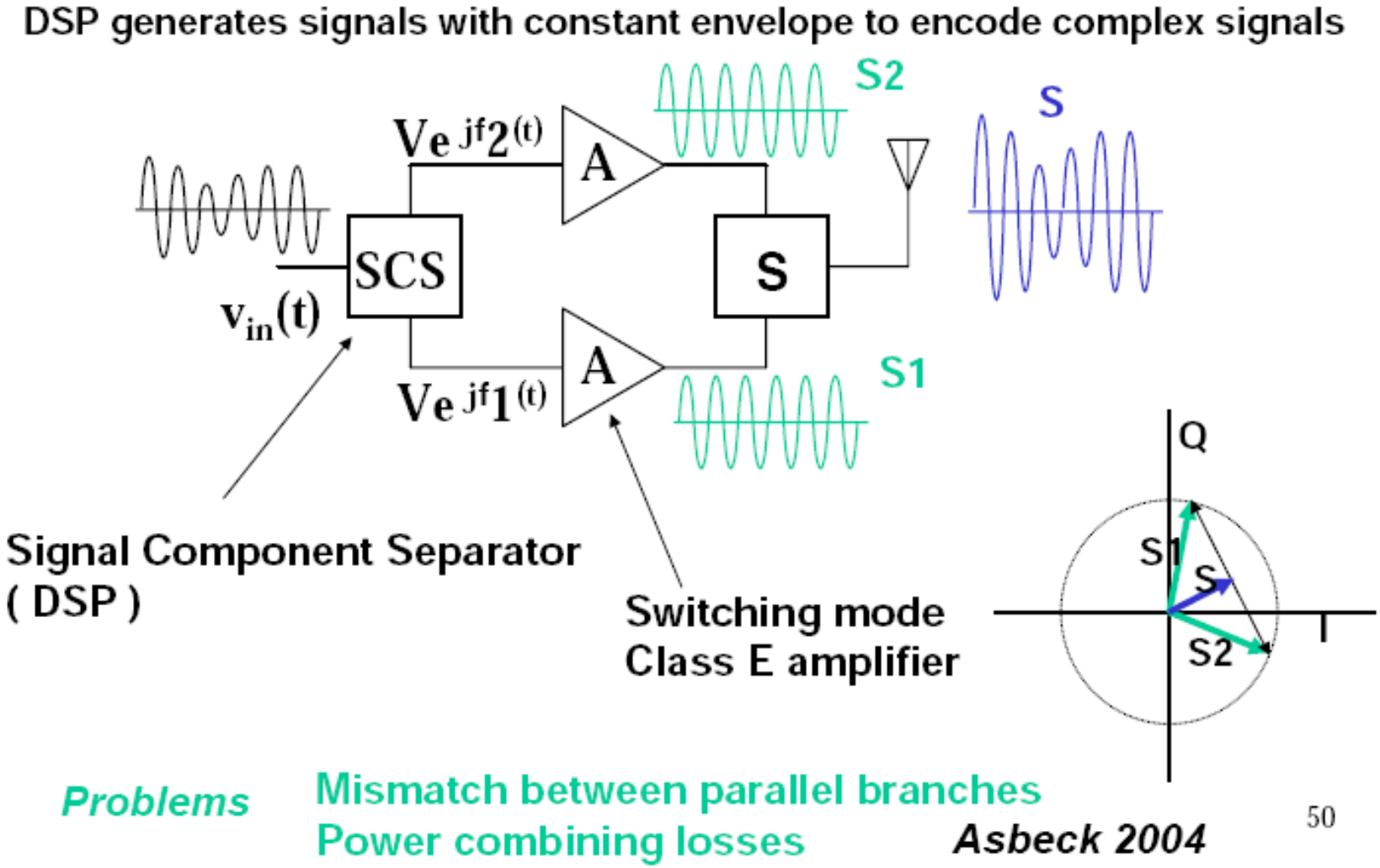
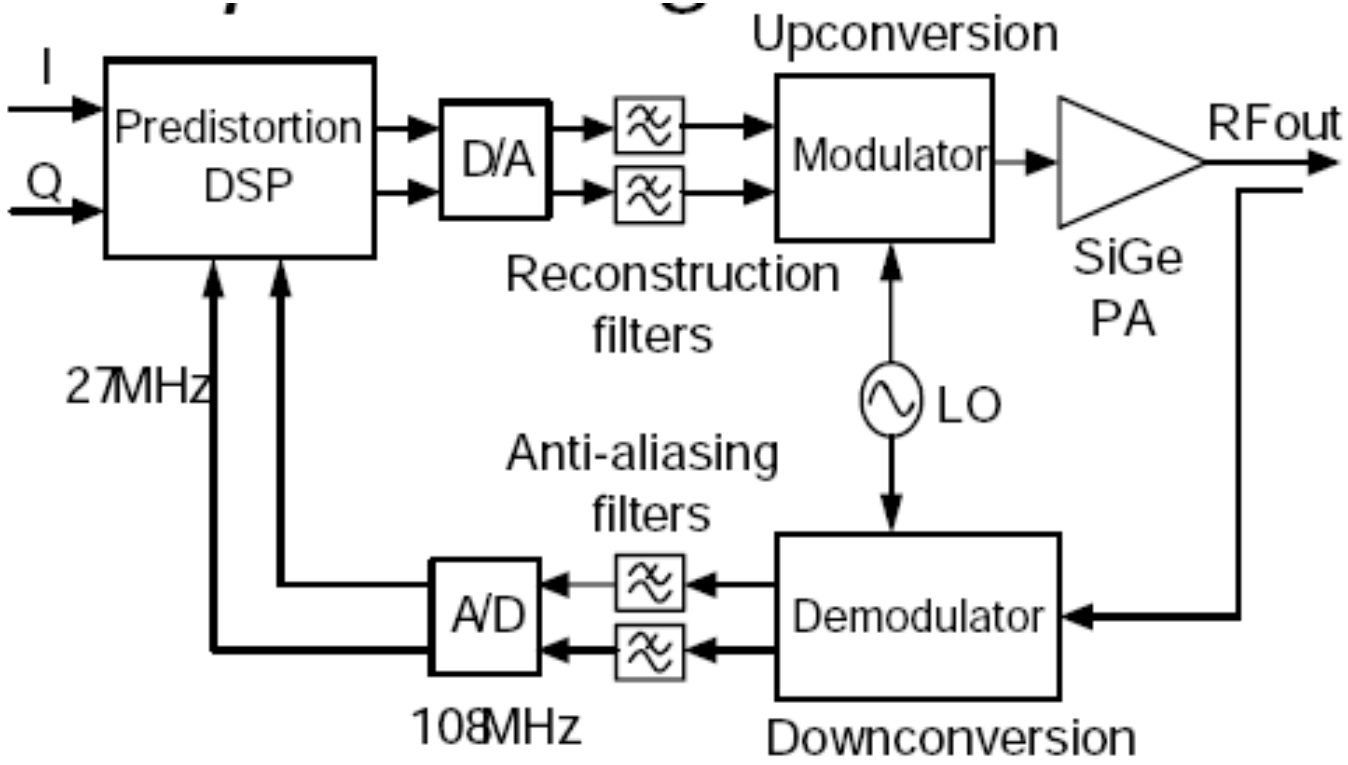
LINC amplifier (L. Larson 2007)

- Linear Amplification with Nonlinear Components



Digital predistortion (L. Larson 2007)

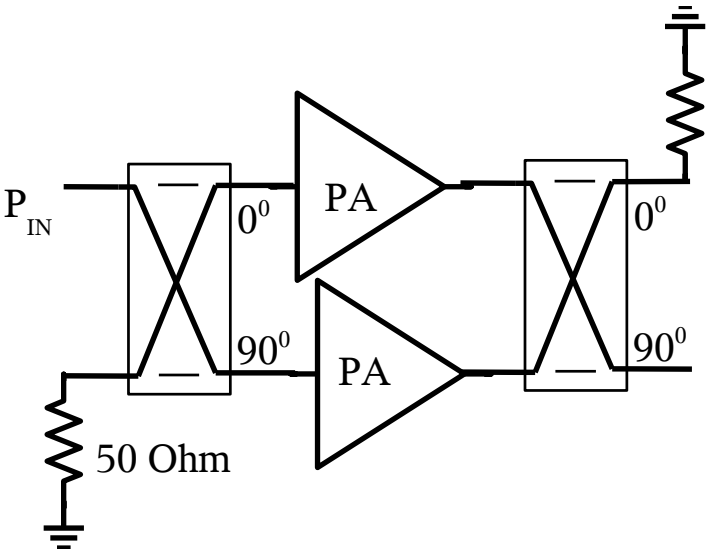


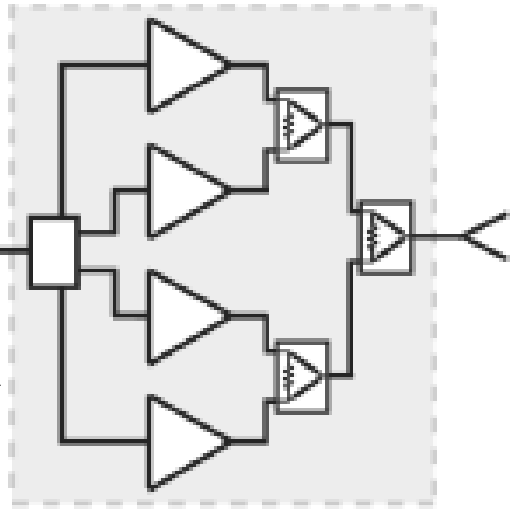
- Digital predistortion creates an "inverse" PA nonlinearity in the DSP.
- Issues: bandwidth expansion; DSP memory table size and updating.

Power combining techniques

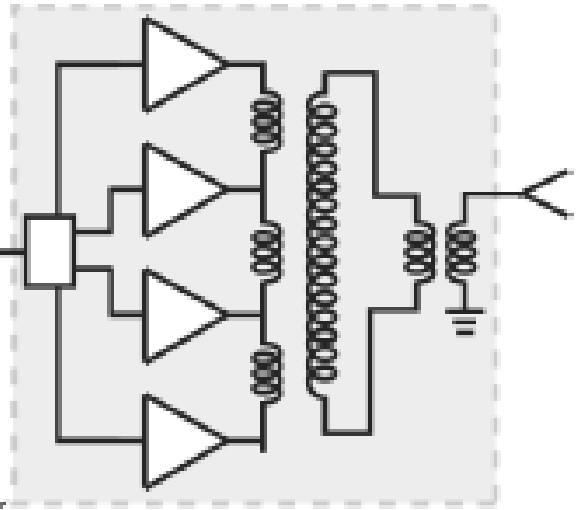
- Critical in nanoscale CMOS where voltage swing is low
  - Two-way: balanced, push-pull, in-phase power combining using Wilkinson couplers
  - multi-way power combining
    - series connection of transistor output voltage
    - half-wavelength paralleling
      - simple
      - Bagley polygon
      - spatial (through the air) lambda/2 power combining

Power combining examples

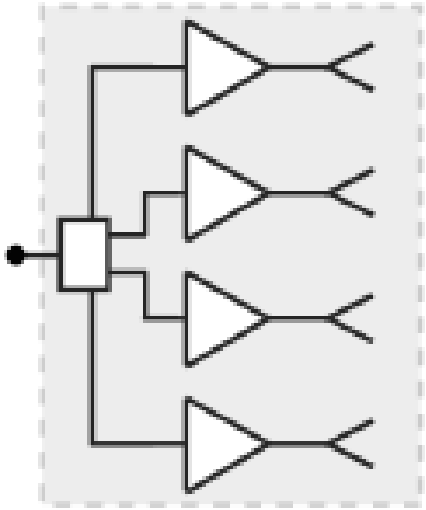


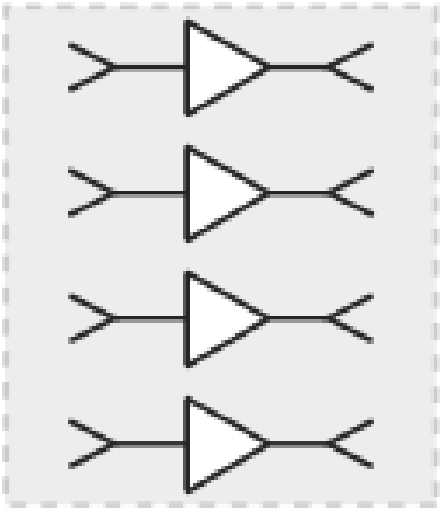


(a)



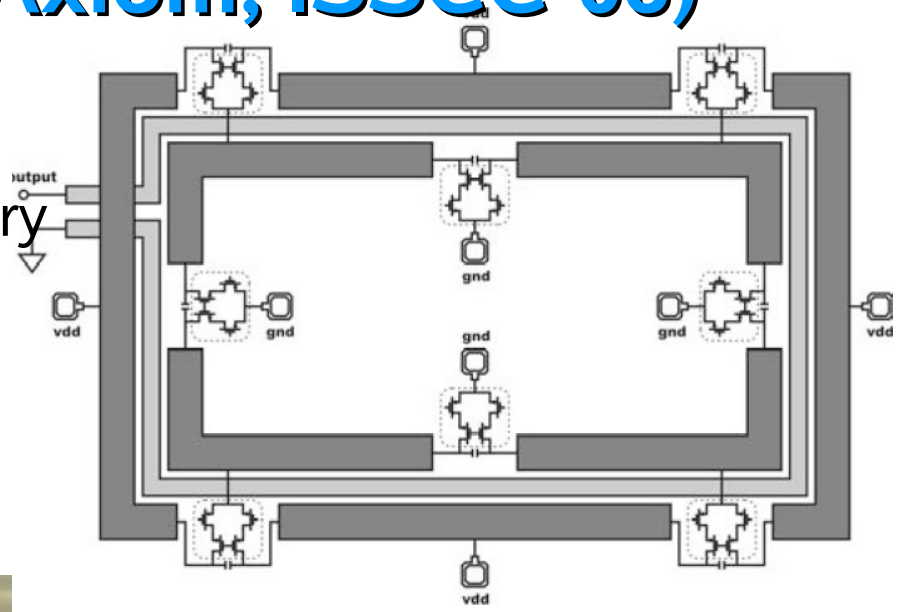
(b)

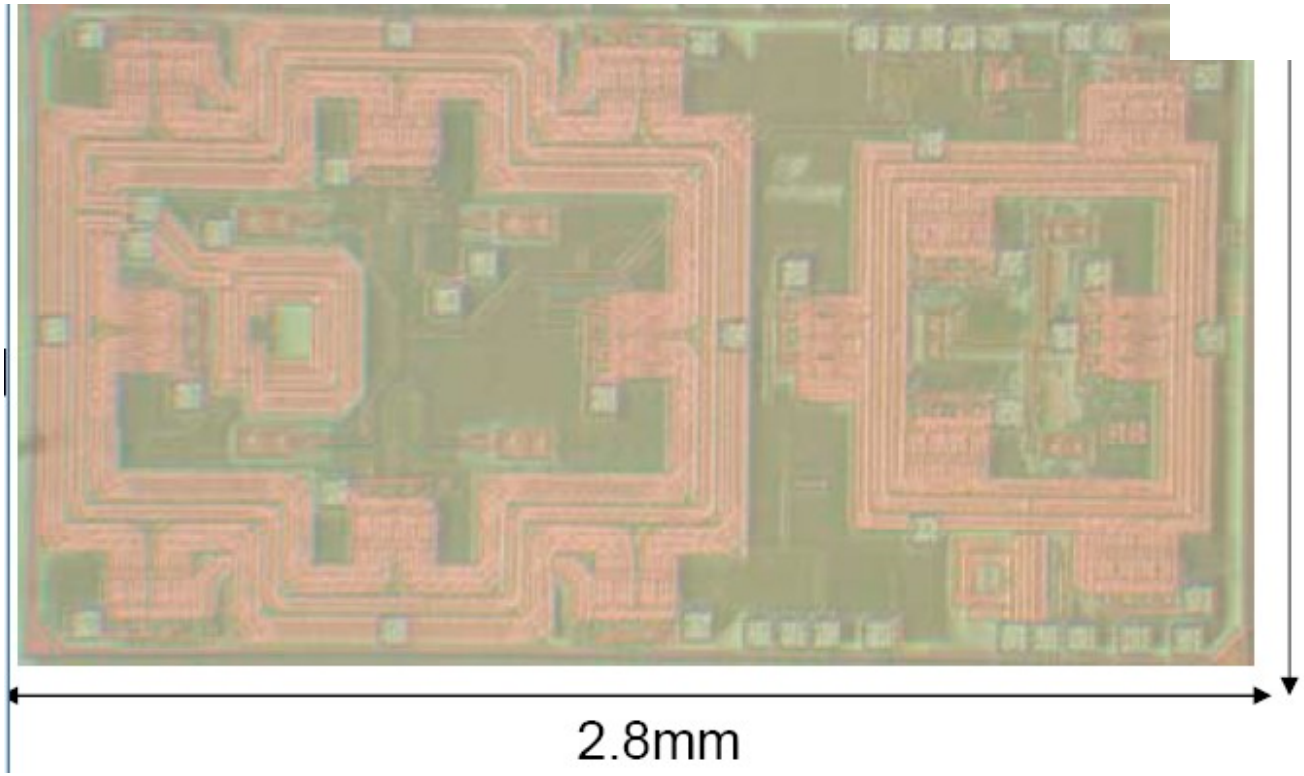




2-GHz Class B, 3W PA (Axiom, ISSCC-08)

- Two (wide) concentric coils for the primary
- One thin (high voltage) coil for the secondary
- 8 differential stages are serially combined

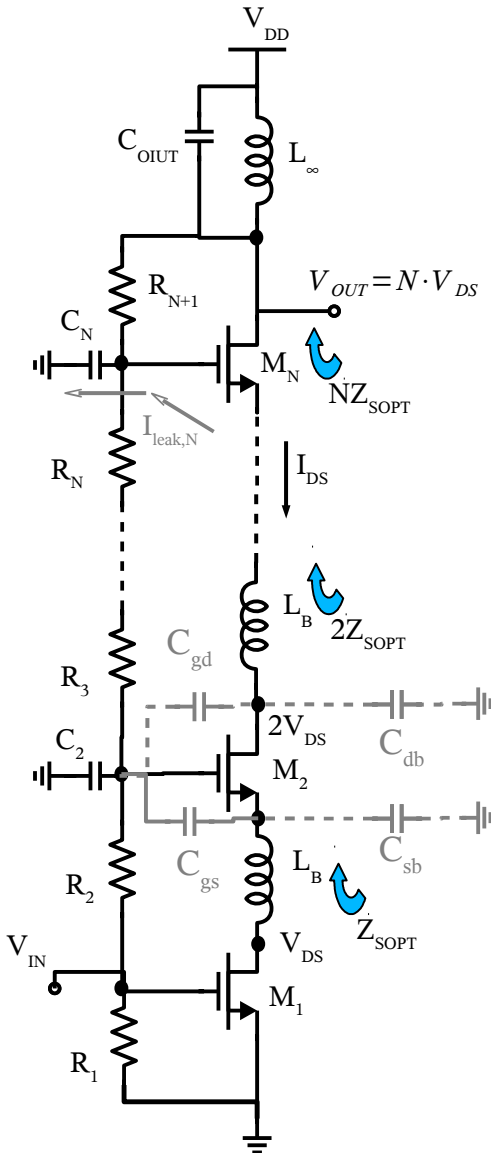




Series stacking of transistors

- M.Shifrin, et al. 1991 with GaAs MESFET
- S. Prompromlikit et al, 2010, SOI n-MOSFET
- I. Sarkas et al., ISSCC 2012 SOI CMOS

$$Z_{source,i} \approx \frac{1}{g_{m,i}}\left(\frac{C_{gs,i}}{C_i}+1\right)\frac{1}{1+j\dfrac{\omega}{\omega_T}} \approx \frac{1}{g_{m,i}}\left(\frac{C_{gs,i}}{C_i}+1\right)$$



Summary

- The most important parameter affecting PAE and P_{sat} is V_{MAX}
- Design of class A, AB PA is scalable through 200 GHz.
- In class A MOSFET PAs, biasing at 0.3-0.4mA/μm ensures maximum linearity and PAE
- Q of matching network is critical (>10. i.e. 1dB loss = 21% power loss)
- Switching PAs (D, E, F) used primarily at GHz frequencies for efficiency but making inroads into mm-waves
- For >1W PAs, special devices are employed: GaAs HBT, LDMOS, GaN HEMTs or stacked SOI MOSFETs