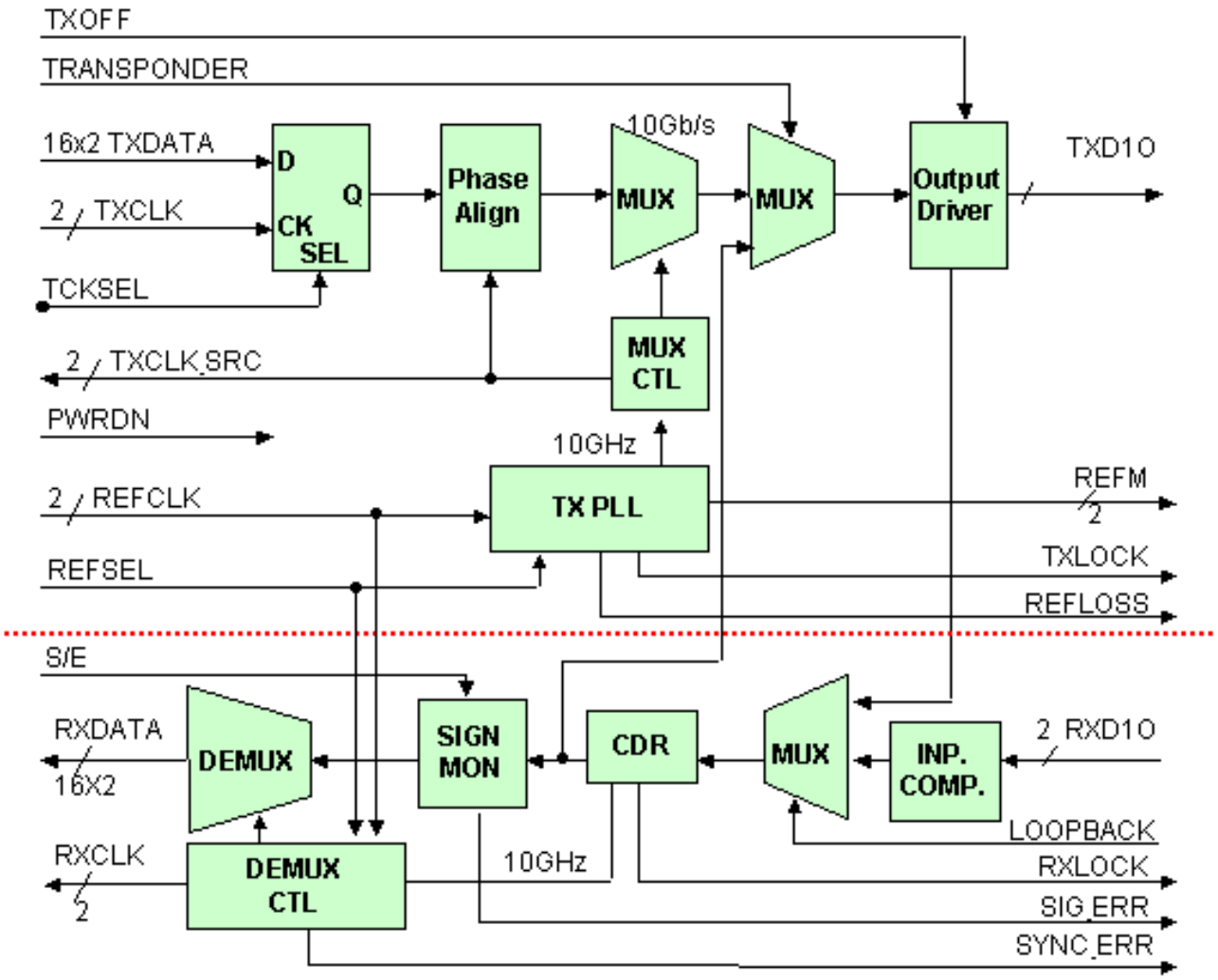
High Speed Digital Blocks

Outline

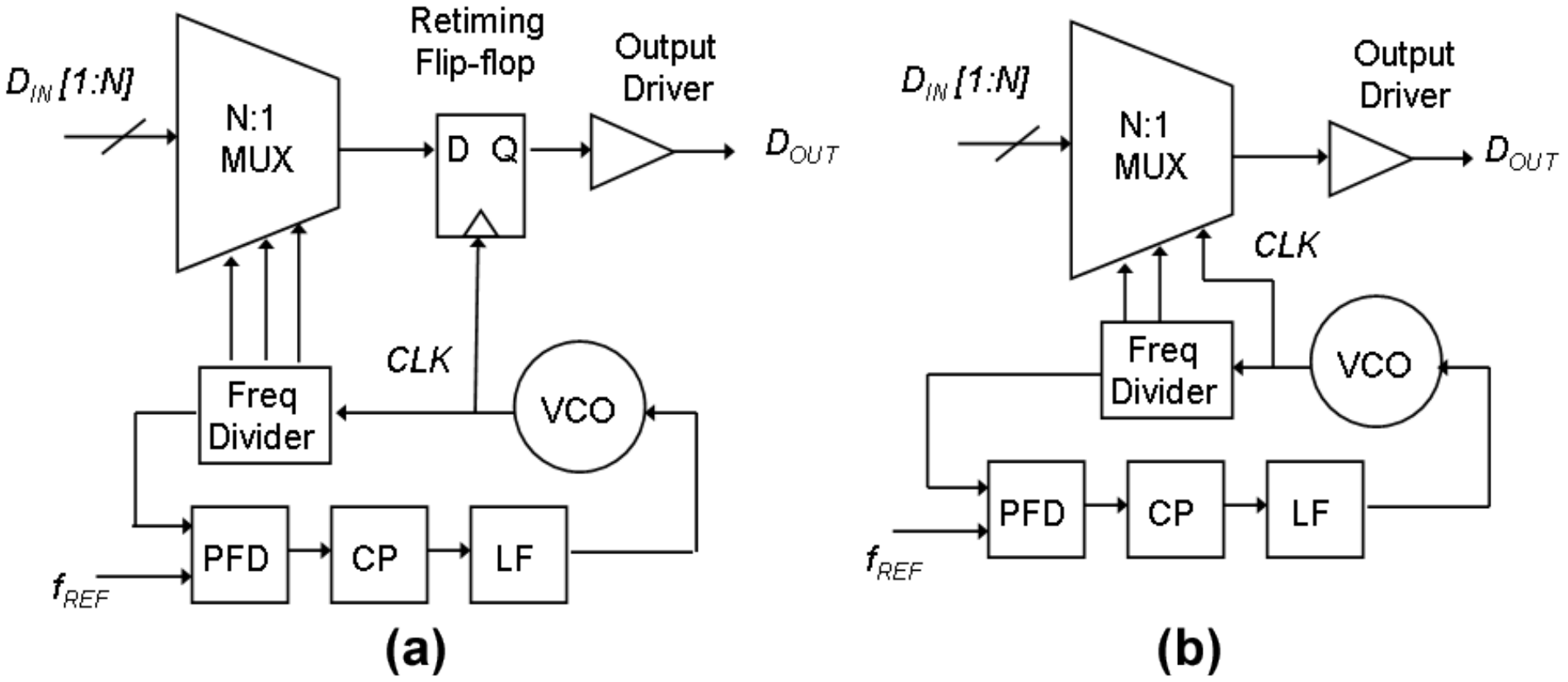
- Systems using high-speed logic
- High-speed logic families
- Frequency response of basic ECL/CML cells
- Design methodology for high-speed logic gates
- Examples of typical high-speed digital gates
  - Selector, AND
  - Latch, latched XOR, DFF
  - Dividers
  - 4:1 MUX
  - 8:1 Transmitter

Example of a fiberoptics SerDes

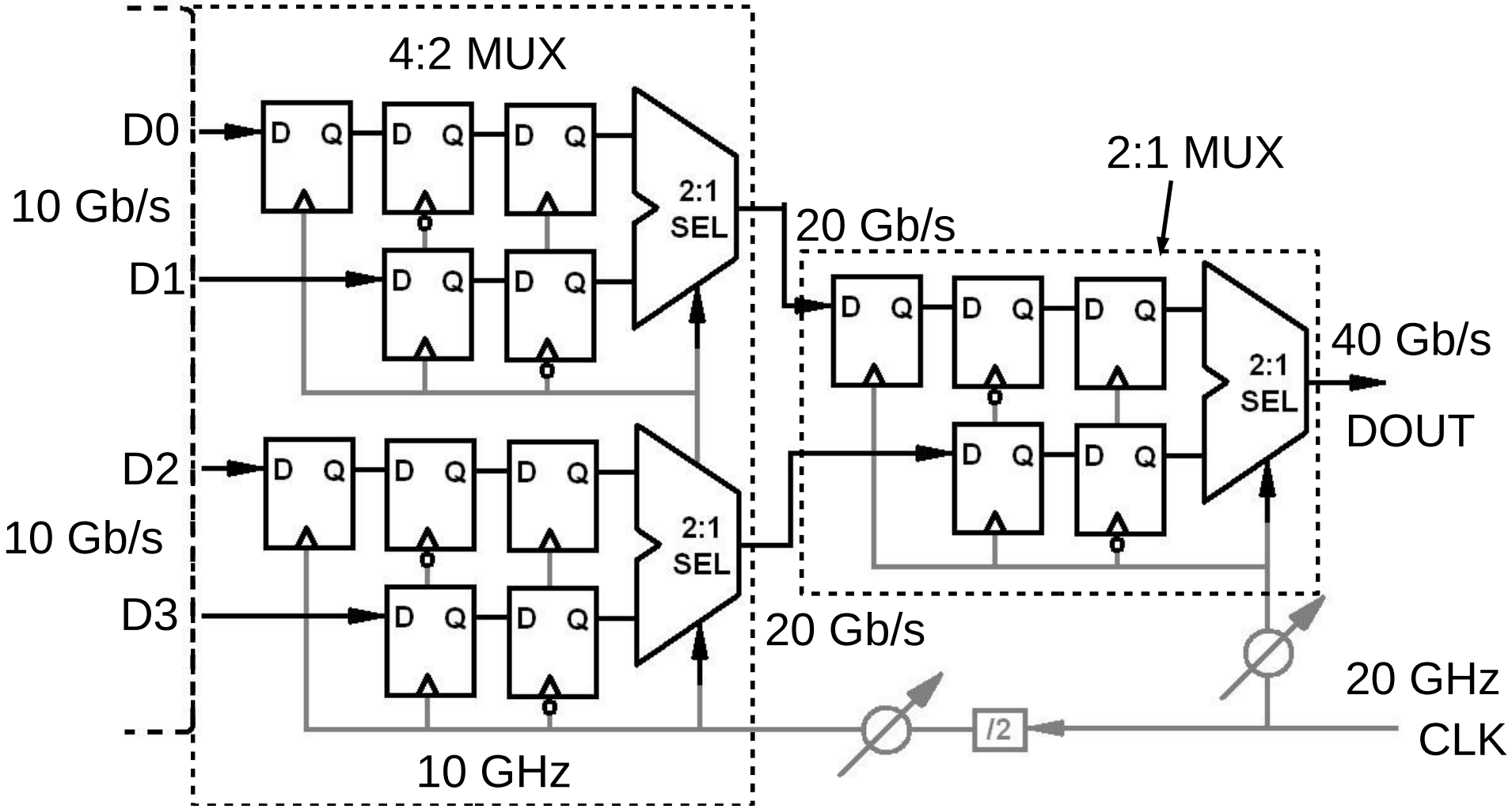


[1]

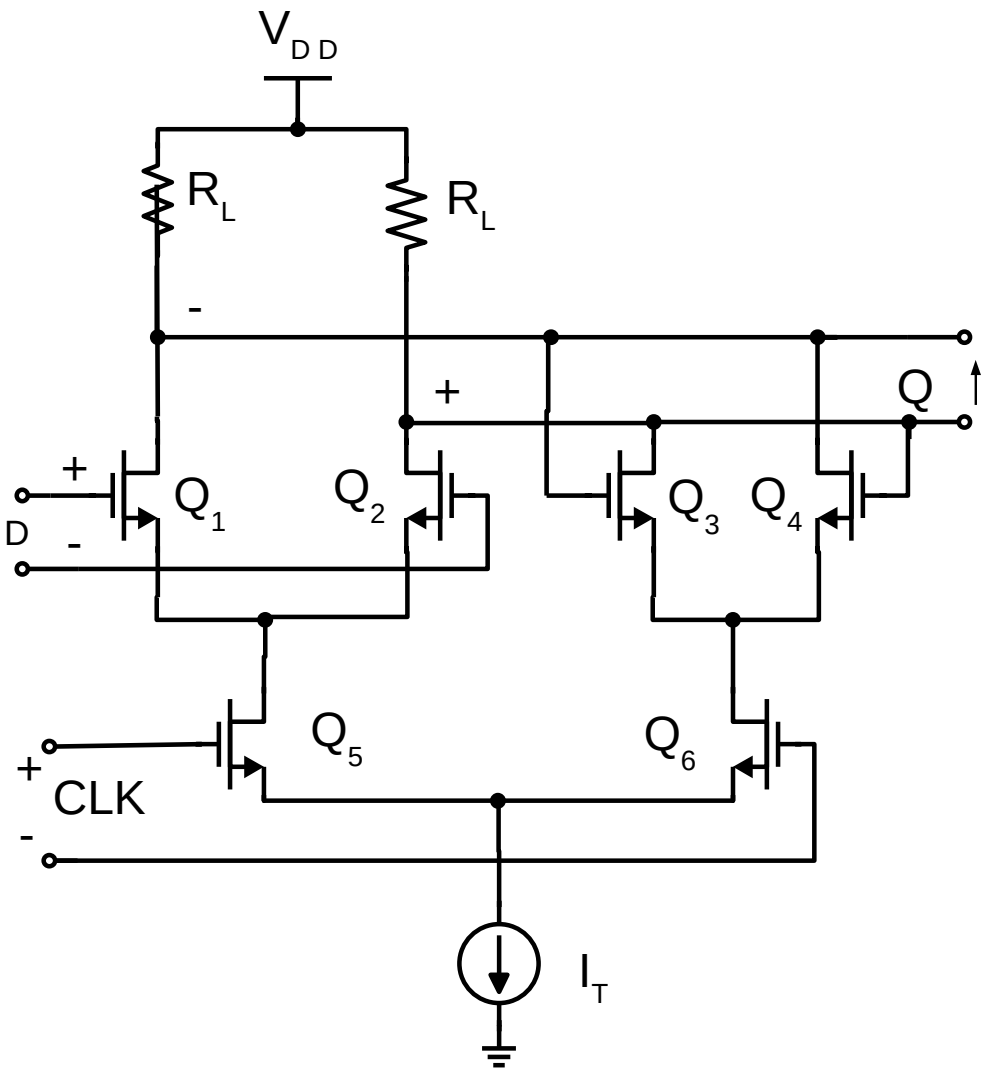
Serializer w/o full-rate retiming

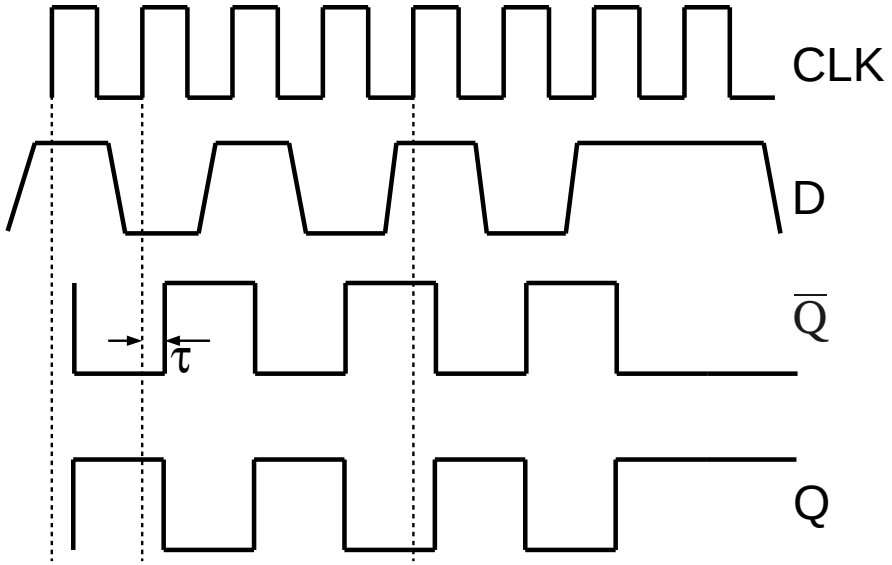


4:1 40-Gb/s Multiplexer

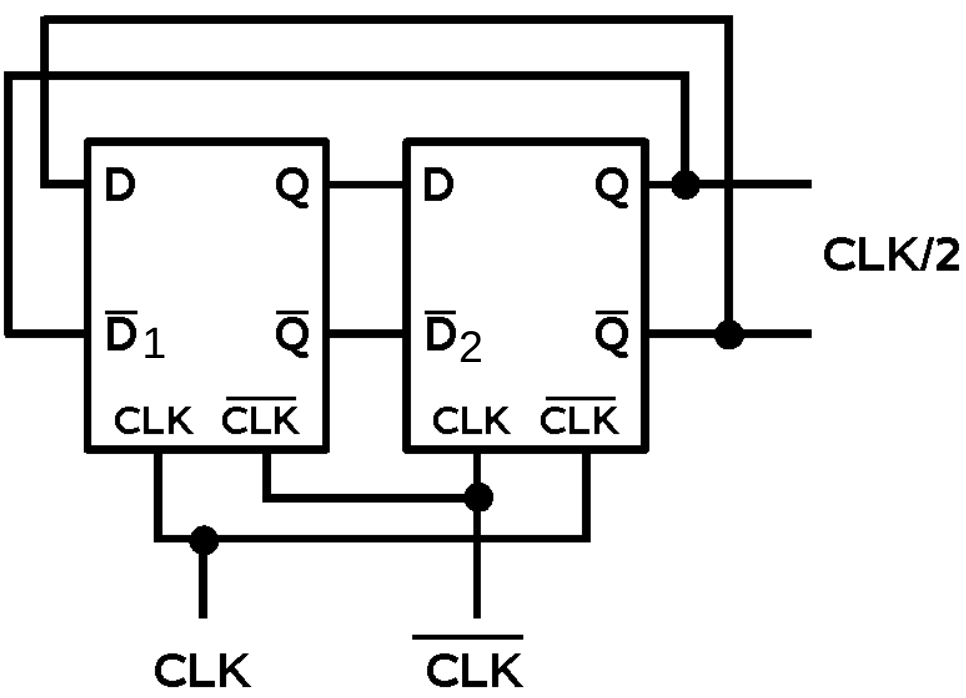


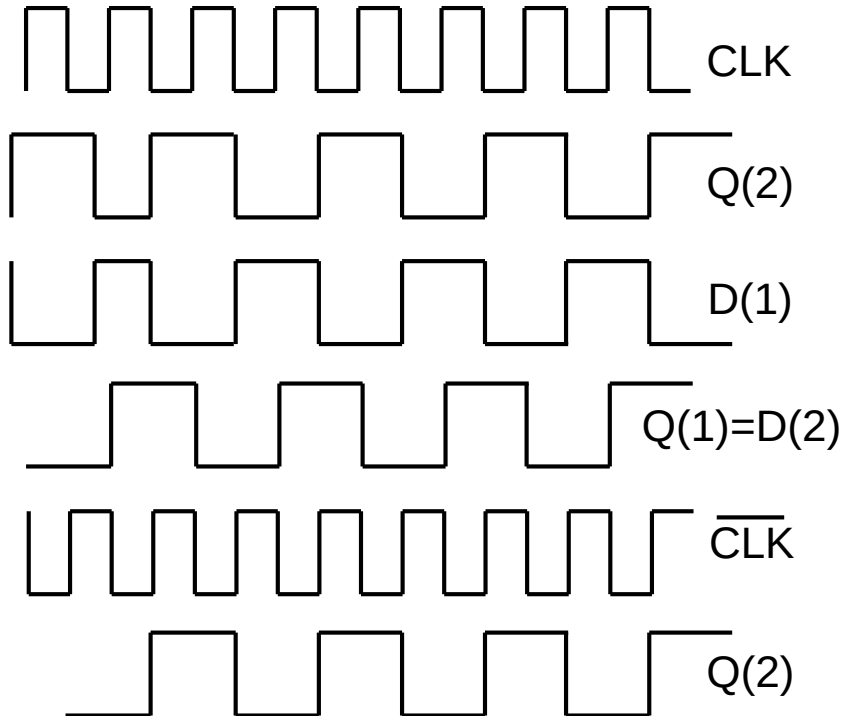
2:1 Selector



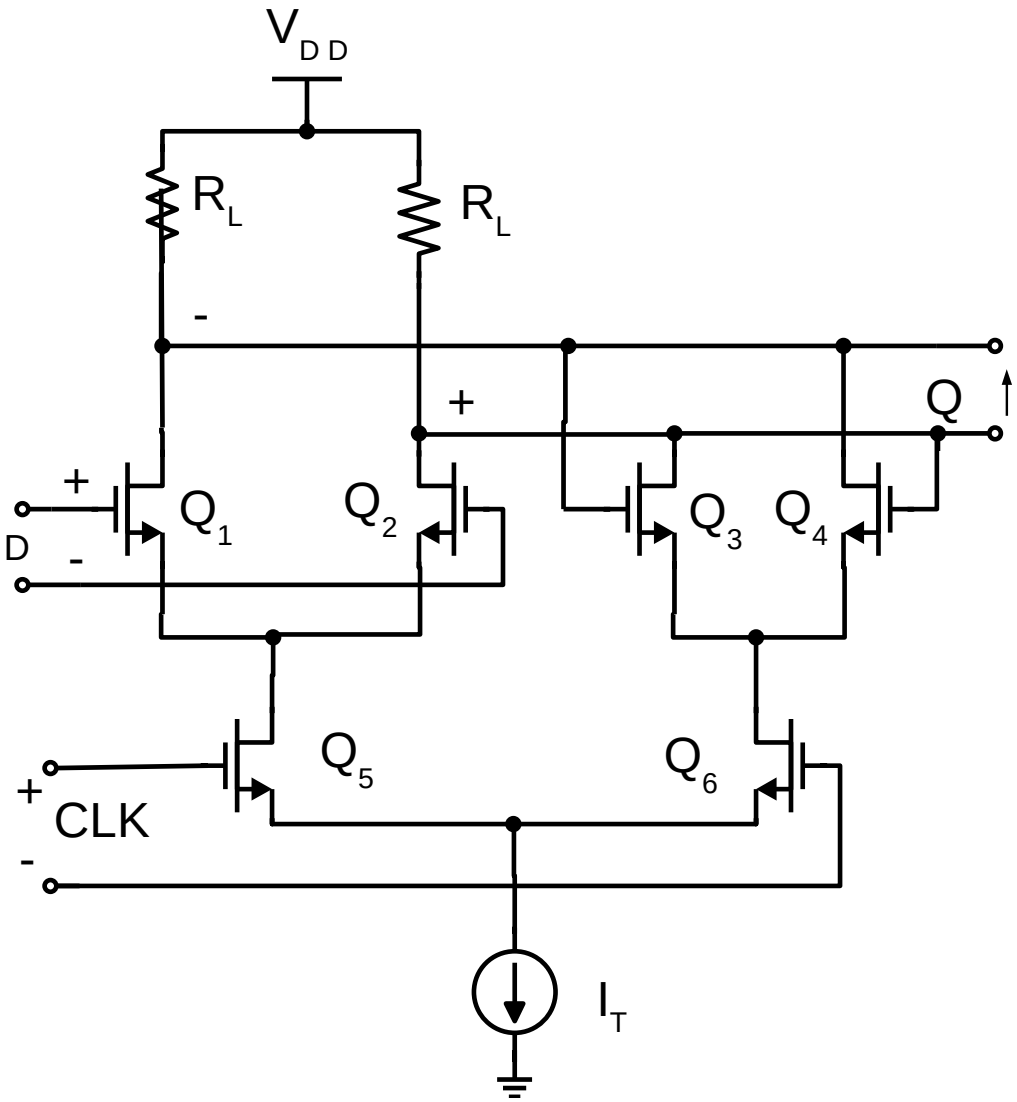


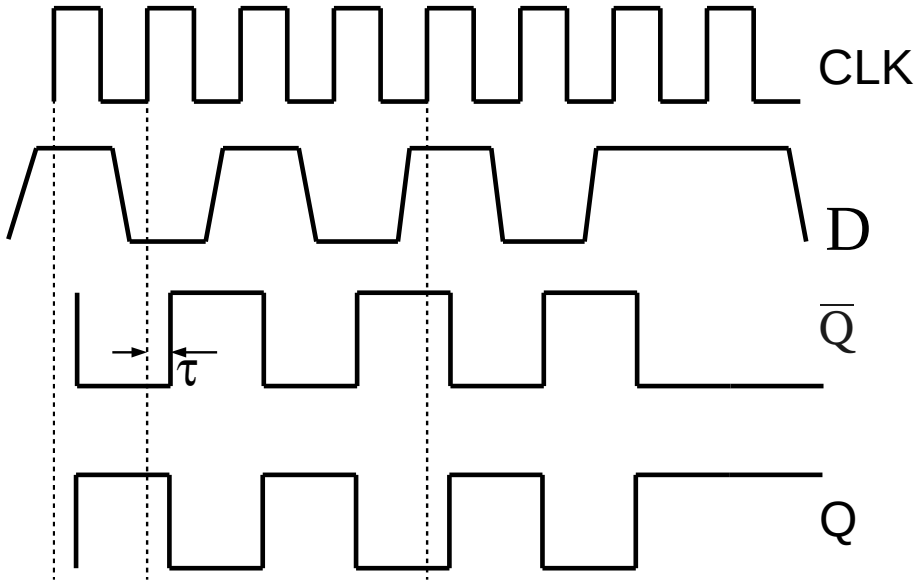
2:1 Static Divider with D-type latches



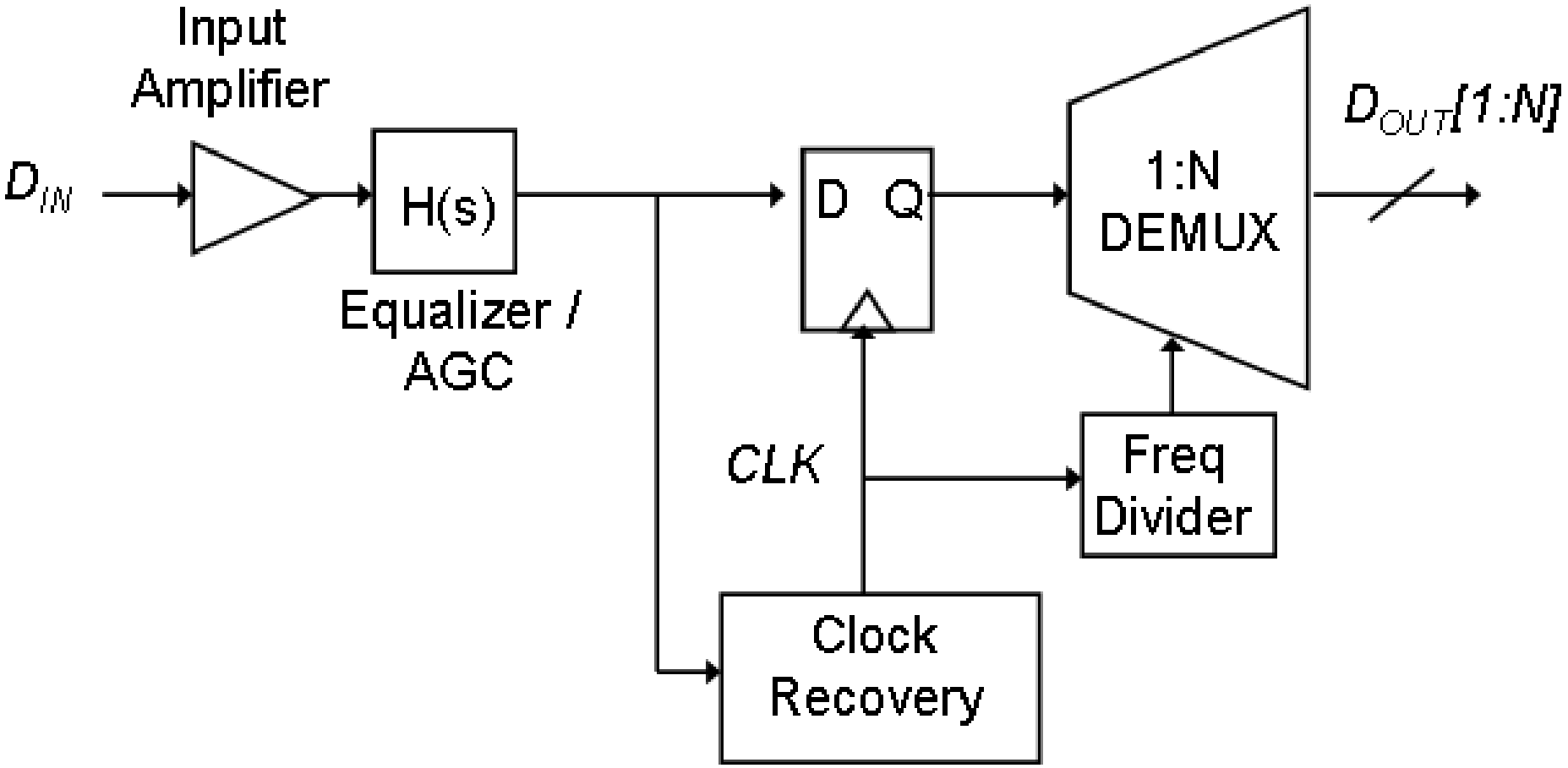


MOS-CML D-type latch

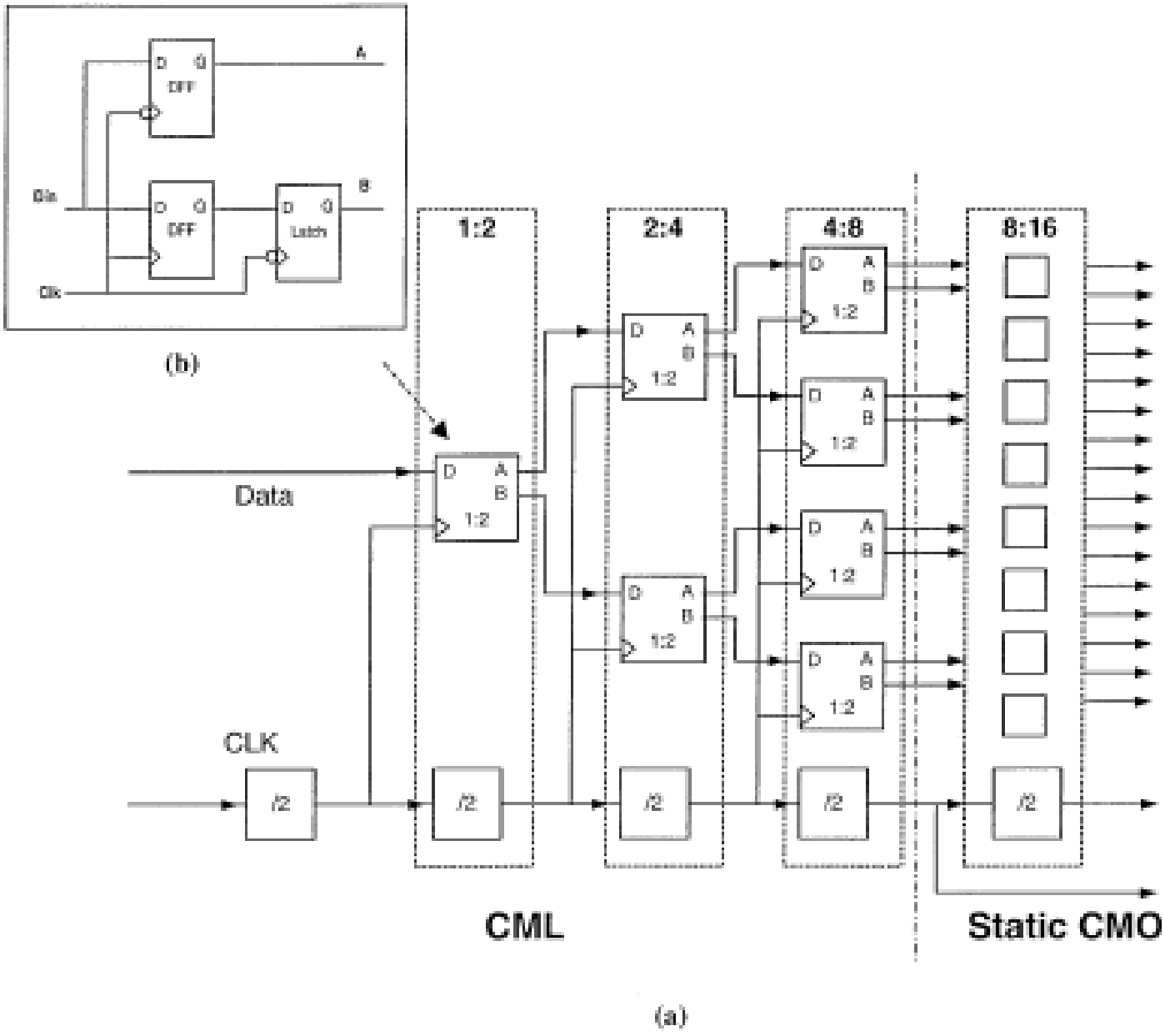




Deserializer Block Diagram

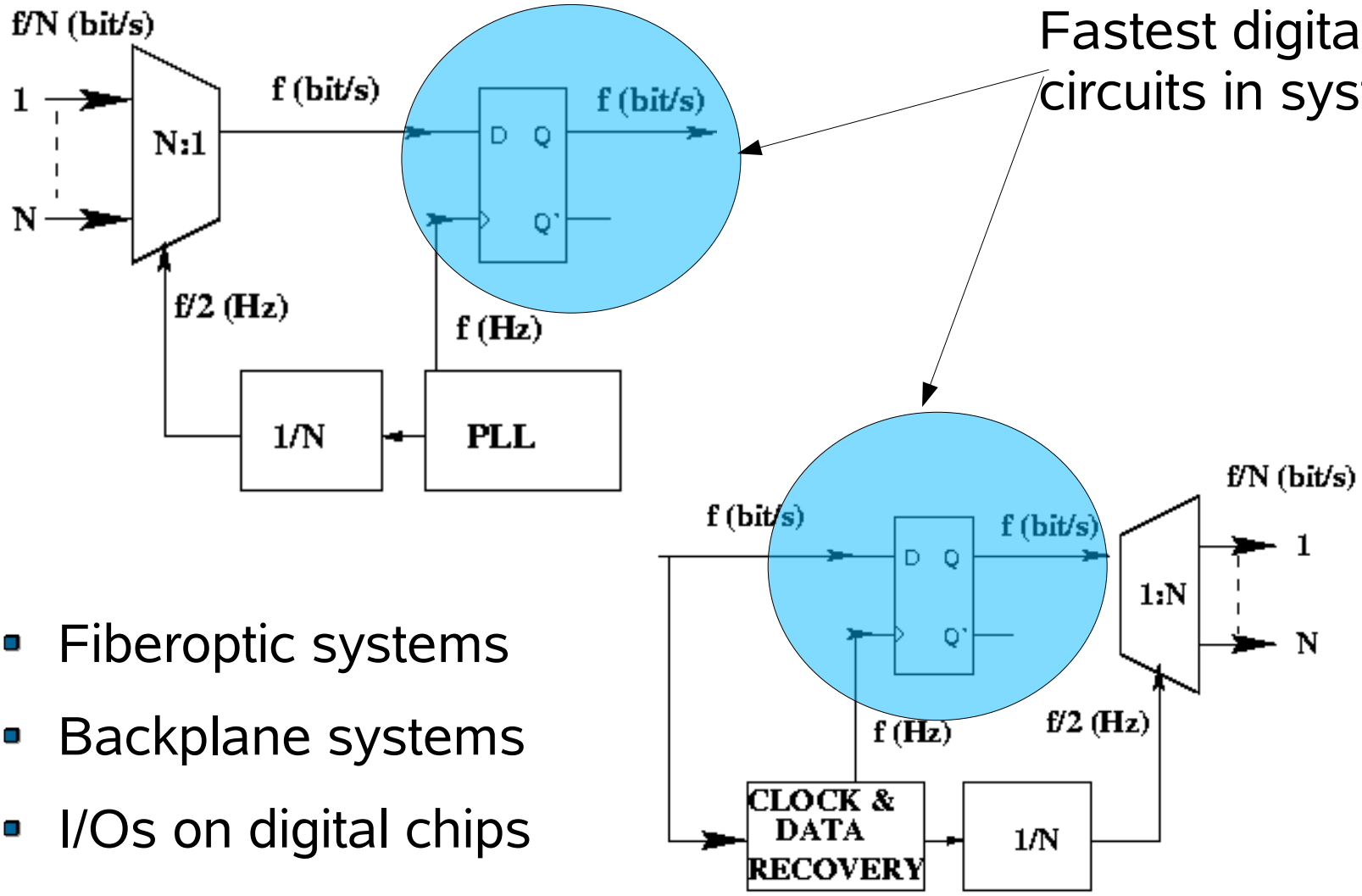


10-Gb/s 1:16 Demultiplexer



[3]

Transceiver with re-timed MUX & DMUX

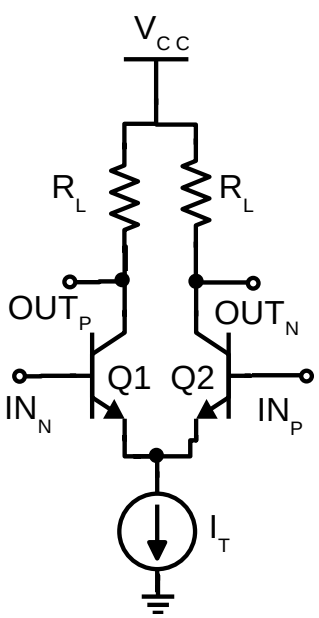


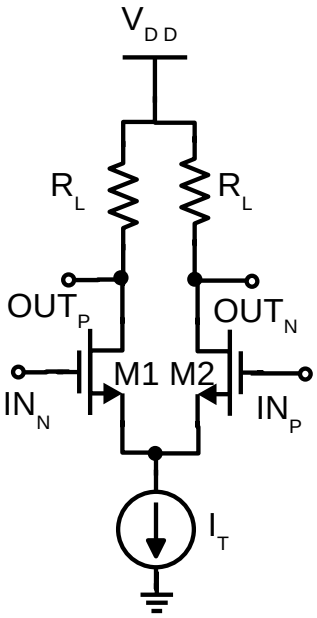
- Fiberoptic systems
- Backplane systems
- I/Os on digital chips

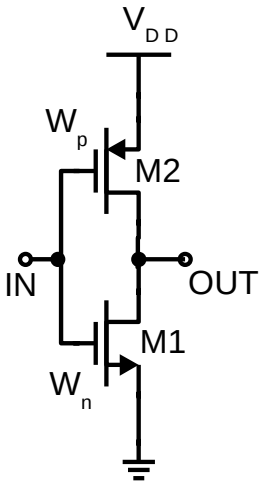
High-speed digital logic families

- All high-speed logic families use diff. topologies
- Current-Mode Logic (CML)
  - Bipolar
  - SCFL (using MESFETs)
  - MOS
  - BiCMOS
- ECL or E^2CL(Emitter-Coupled Logic)
  - Bipolar
  - III-V FET
  - BiCMOS

CML vs. CMOS





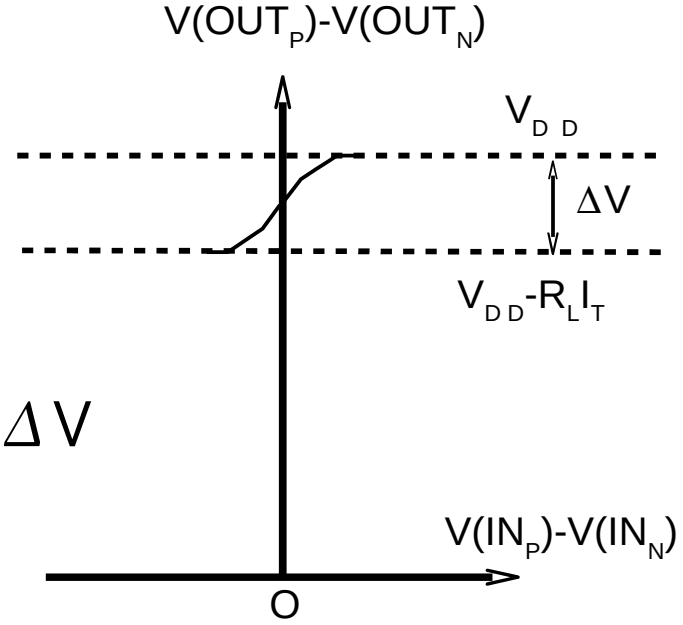


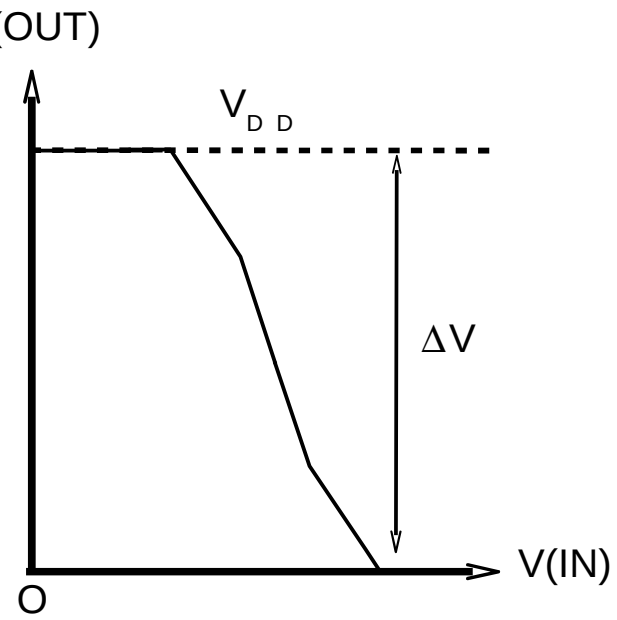
$$P_D = I_T V_{DD}$$

$$\Delta V = I_T R_L$$

$$V_{OH} = V_{DD}$$

$$V_{OL} = V_{DD} - \Delta V$$





General Characteristics of CML

- Operate in the active region for highest speed

  i.e. triode region avoided

- All high-speed logic families use differential amplifier topologies

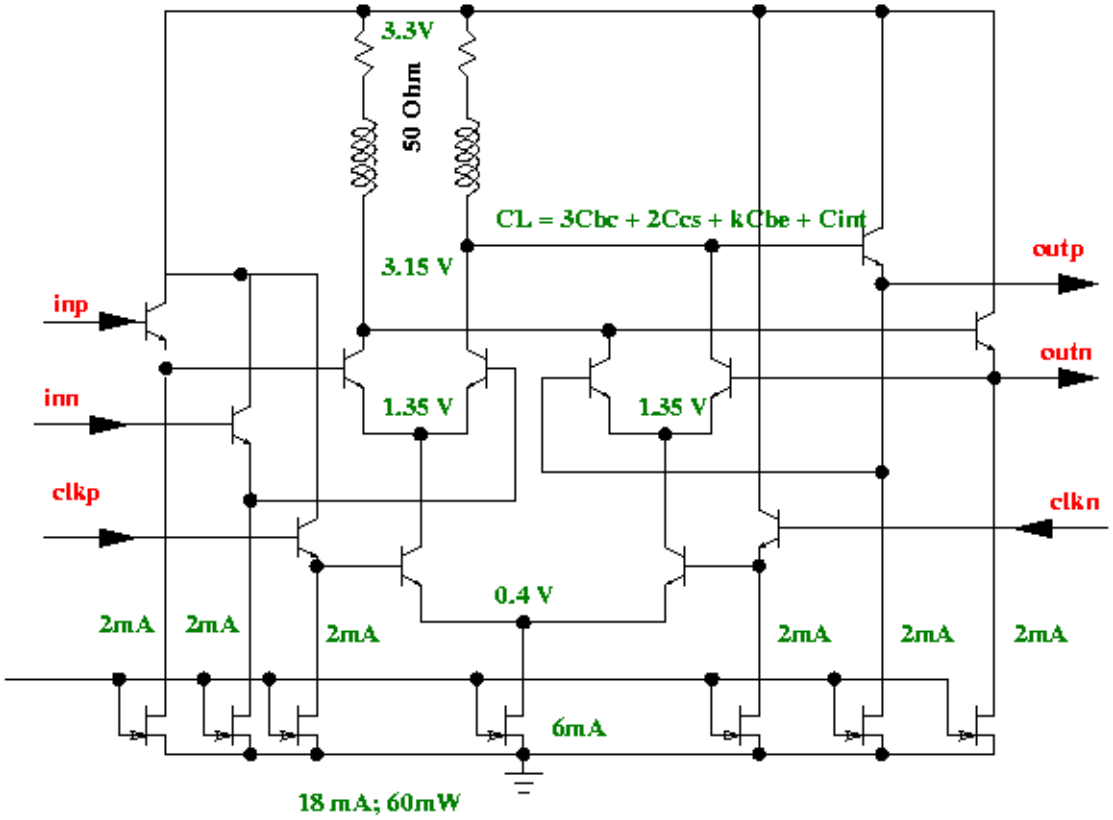
  they typically consist of inverters, cascodes, SF/EF+INV

- Static power only

  i.e. for a given gate, power dissipation does not depend on switching speed

ECL Cells

- Inverter (emitter/source coupled pair)
- Emitter/source follower
- Cascode
- Ind. peaking
- All of the above



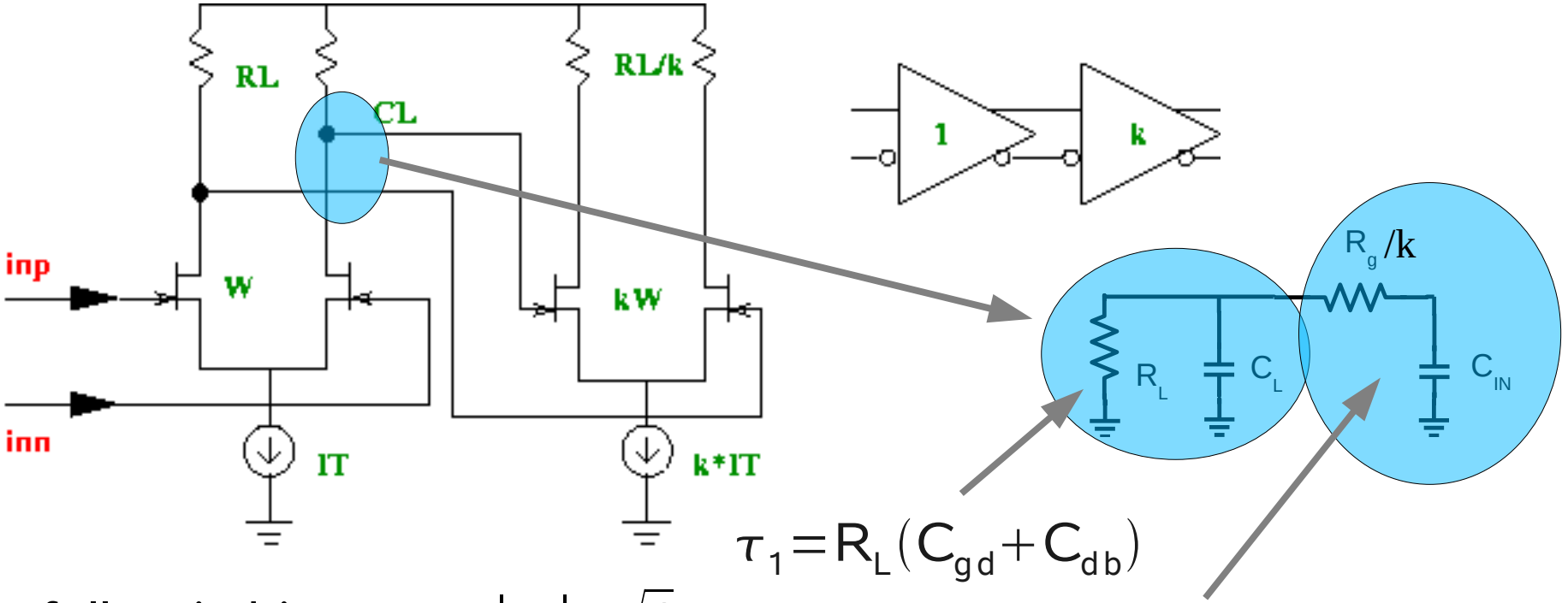
Design goals in high-speed digital blocks

- Maximize speed:
  - topology optimization (inv, cascode, EF..)
  - transistor biasing & sizing ($\mathbf{I_T}$, $\mathbf{I_E}$, $\mathbf{W_f}$, $\mathbf{N_f}$)
- Minimize power dissipation:
  - Lowest tail current for given speed
  - Lowest bias supply (related to topology)
  - Optimal inter-stage scaling (current & size)
- Achieve output swing in matched 50Ω load.

Switching speed analysis

- Digital gates can be treated as small signal amplifiers
- The open circuit time constant technique (Elmore delay) can be used to analyze the small signal frequency response

Analysis of fanout-of-k MOS-CML inverter stages



$$\tau_1 = R_L(C_{gd} + C_{db})$$

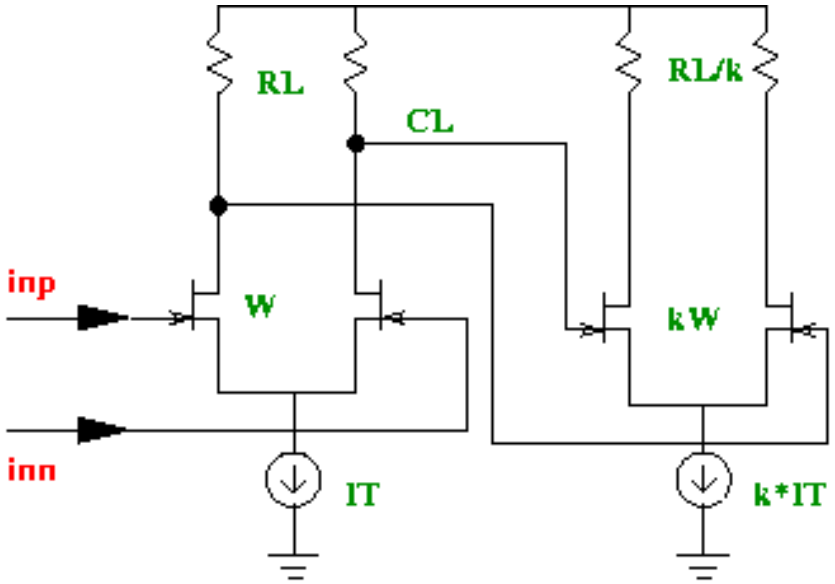
For full switching: $|A_V| > \sqrt{2}$

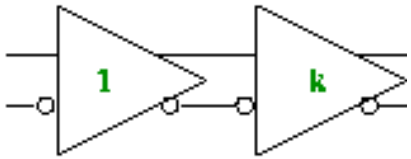
$$\tau_2 = \left(R_L + \frac{R_g}{k}\right)\left[k\,C_{gs} + (1 + g_m R_L)\,k\,C_{gd}\right]$$

$$\tau = \tau_1 + \tau_2 = R_L(C_{gd} + C_{db}) + R_L\left(k + \frac{R_g}{R_L}\right)\left[C_{gs} + (1 + g_m R_L)C_{gd}\right]$$

$$A_V = -R_L g_m; \quad g_m = \frac{I_T}{V_{eff}}; \quad R_L = \frac{\Delta V}{I_T}; \text{ hence } A_V = \frac{-\Delta V}{V_{eff}}$$

Cascading MOS-CML inverter stages

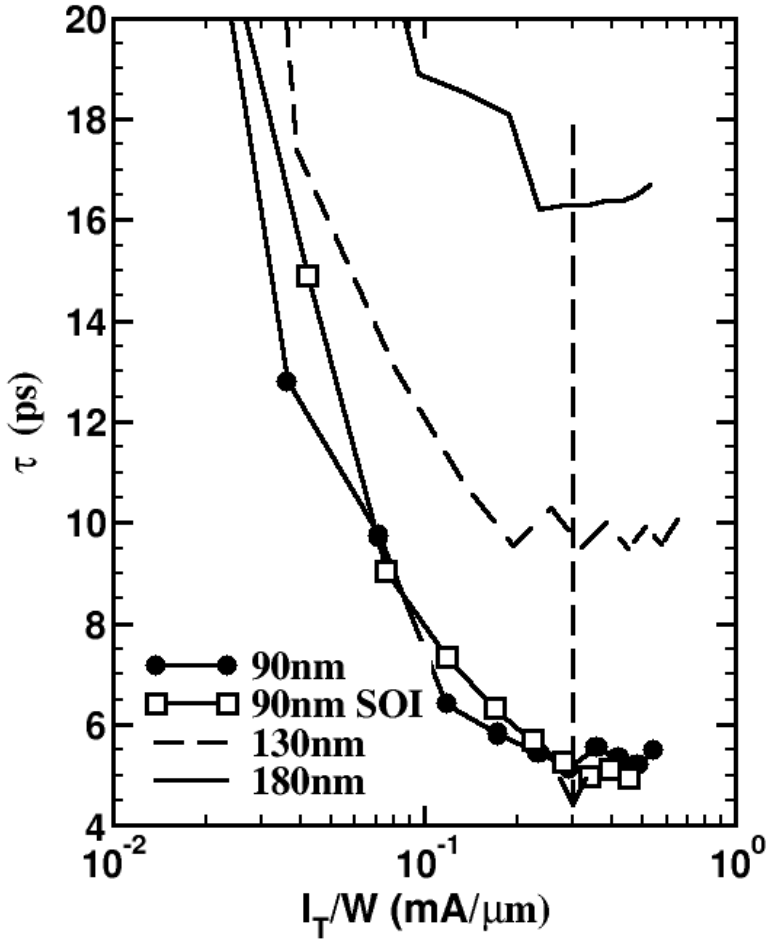




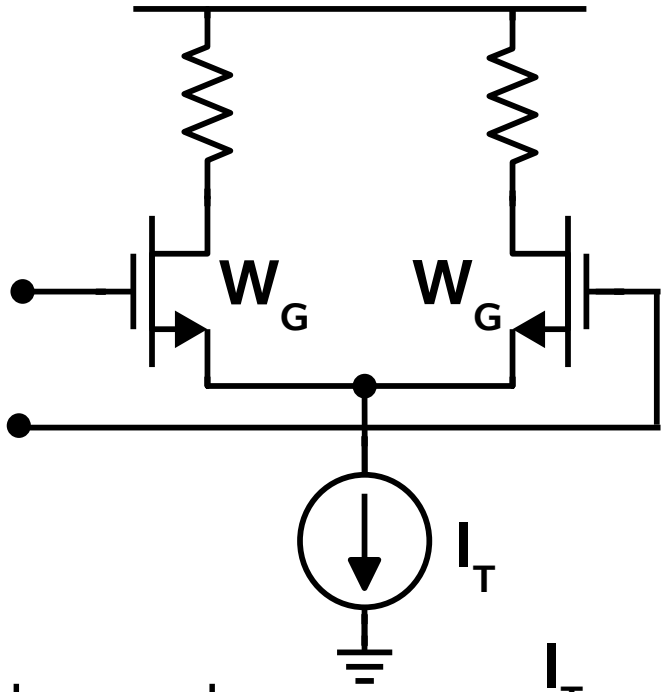
$$\tau_1 = \Delta V \frac{C_{gd} + C_{db} + C_{int}}{I_T} + \left(k + \frac{R_g}{R_L}\right) \Delta V \frac{C_{gs} + (1 - A_V) C_{gd}}{I_T}$$

Keep $R_g < 0.1 \times R_L$ Not difficult to do!

Quasi-Large Signal Analysis of Gate Delay



J_{peakfT} = 0.3 mA/μm and remains constant over technology nodes

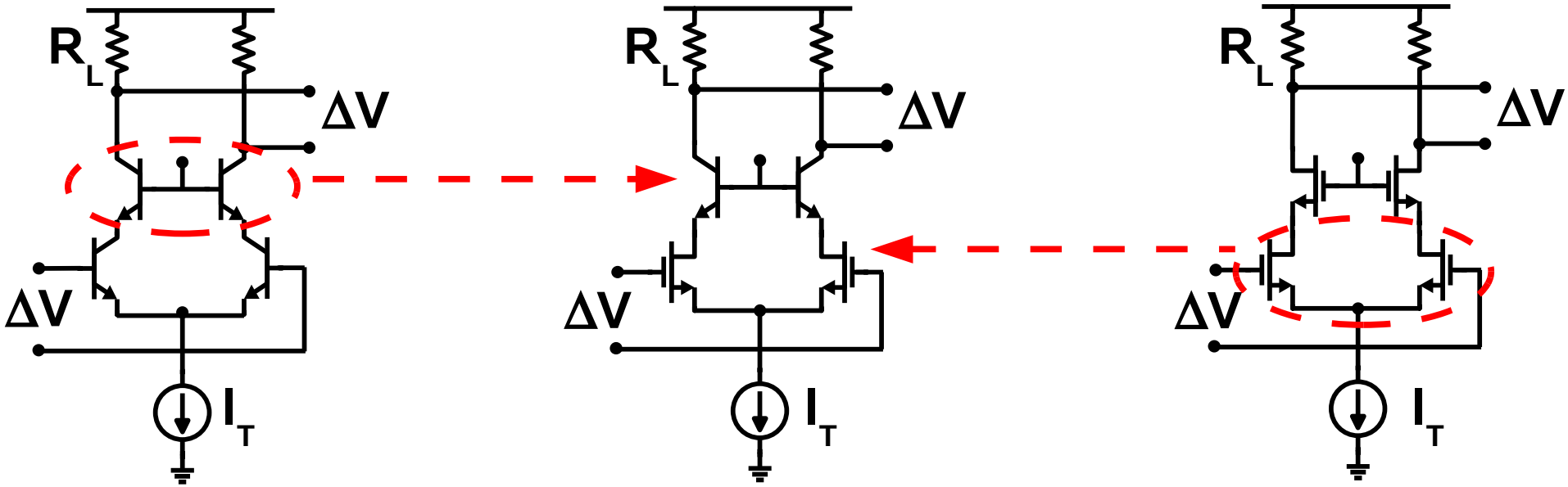


- There is no improvement in delay beyond I_T= 0.3 mA/μm

$$W_G = \frac{I_T}{0.3\ \text{mA}/\mu\text{m}}$$

$\Delta V_{MIN} = 2 \times \left[V_{GS}(I_{DS} = 0.15\,\text{mA}/\mu\text{m}) - V_T \right]$ scales with L

BiCMOS Current-Mode Logic



- ✔ High slew rate
- ✗ High $R_B C_{BC}$
- ✗ Lower yield
- ✗ High V_{CC}

$$\tau_{BiCMOS} \approx \Delta V \frac{C_{BC} + C_{CS}}{I_T} + \left(k + \frac{R_G}{R_L}\right) \Delta V \frac{C_{GS} + C_{GD}}{I_T}$$

- ✔ MOS low input time constant
- ✔ HBT low output time constant

- ✗ High C_{DB}
- ✔ Low $R_G C_{GD}$
- ✔ High Yield
- ✔ Low V_{DD}

BiCMOS cascode gate delay

$$SL_{HBT} = \frac{I_{CpeakfT}}{C_{bc} + C_{cs}} \qquad SL_{FET} = \frac{I_{DpeakfT}}{C_{gd} + C_{db}}$$

$$\tau_{HBT} \approx \Delta V \frac{C_{bc} + C_{cs}}{I_T} + \left(k + \frac{R_b}{R_L}\right) \Delta V \frac{C_\pi + (1 - A_V) C_{bc}}{I_T}$$

$$\tau_{FET} \approx \Delta V \frac{C_{gd} + C_{db}}{I_T} + \left(k + \frac{R_g}{R_L}\right) \Delta V \frac{C_{gs} + (1 - A_V) C_{gd}}{I_T}$$

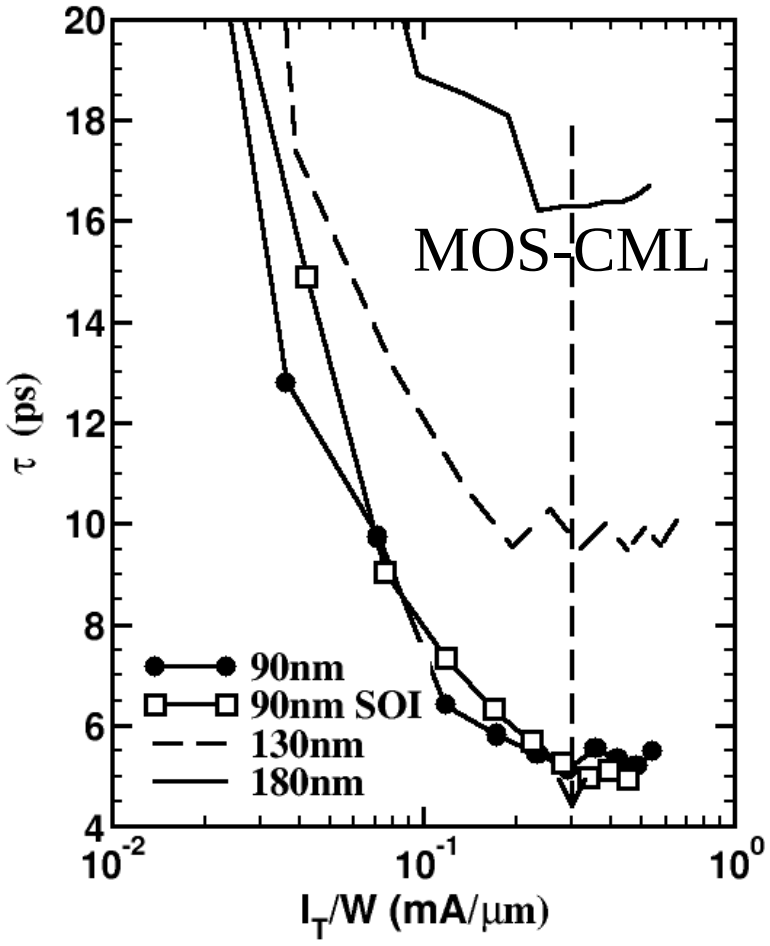
$$\tau_{BiCMOS} \approx \Delta V \frac{C_\mu + C_{cs}}{I_T} + \left(k + \frac{R_g}{R_L}\right) \Delta V \frac{C_{gs} + C_{gd}}{I_T}$$

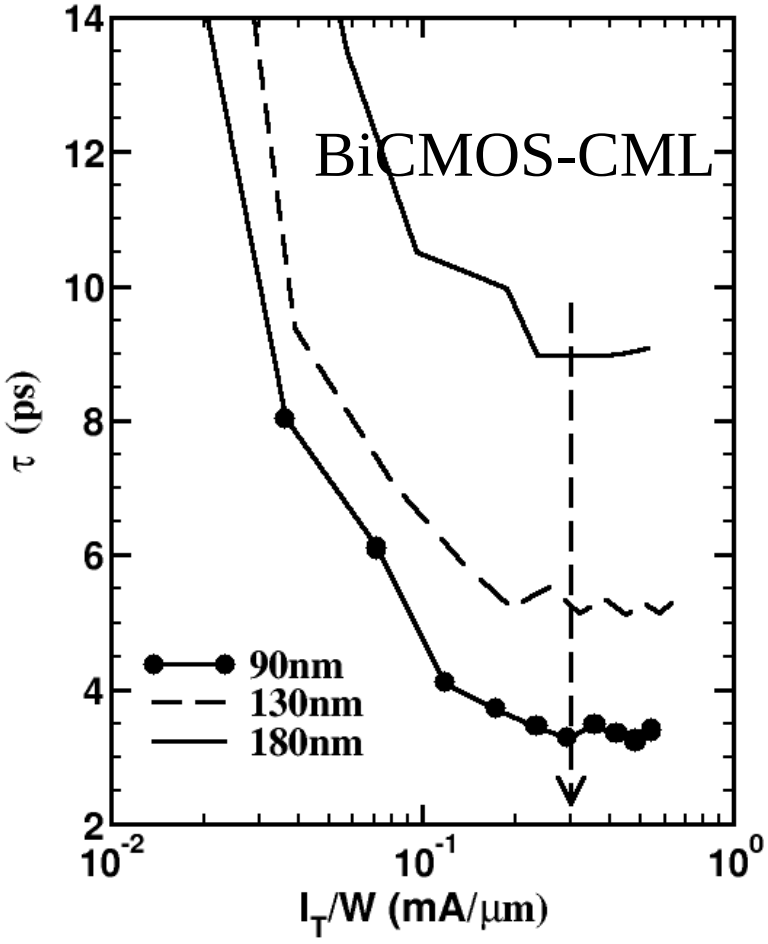
BiCMOS CML Logic

Main ideas:

- Use MOSFETs on clock path only to reduce $R_g \times C_{in}$ time constant
- Use HBT in upper levels to reduce output time constant
- Logic swing remains that of the bipolar CML at 250 mV_{pp}, hence speed
- Only clock path needs to have MOS-CML swing

MOS vs. SiGe BiCMOS CML Delay





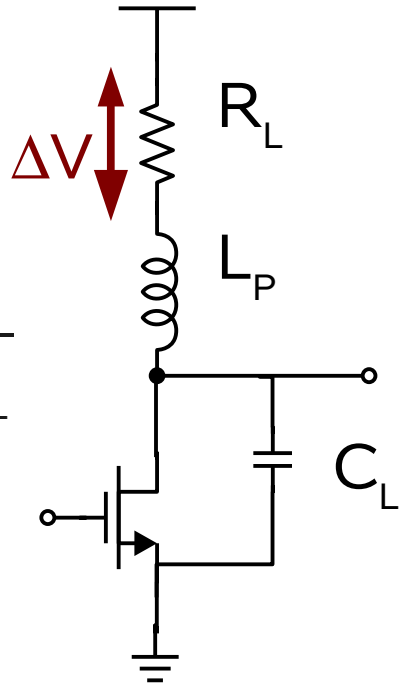
- Speed improvement as FETs scale is due to ΔV scaling.
- Adding a SiGe HBT to a CMOS process almost doubles the speed

Using Inductive Peaking to Improve Bandwidth or Reduce Power

- ΔV is set when technology choice is made

Design equations without peaking:

$$BW_{3dB}=\frac{1}{2\pi R_L C_L};\quad R_L=\frac{\Delta V}{I_T};\quad BW_{3dB}=\frac{I_T}{2\pi \Delta V C_L}$$



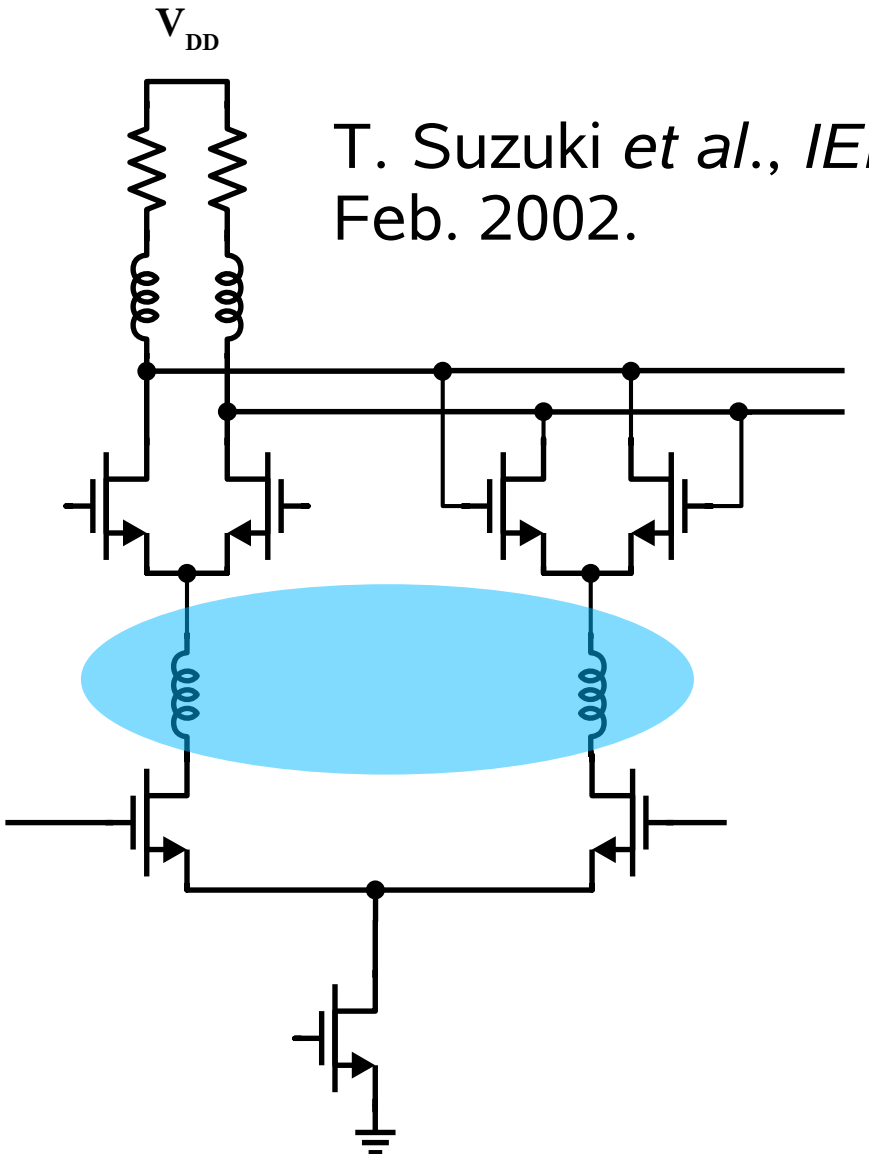
- Design equations with peaking and constant group delay

$$L_p=\frac{C_L R_L^2}{3.1}\qquad L_p=\frac{C_L}{3.1}\frac{\Delta V^2}{I_T^2}\qquad BW_{3dB}=\frac{1.6\times I_T}{2\pi \Delta V C_L}$$

- For a given speed and technology there is maximum realizable inductor L_{PMAX} and a minimum I_T and power that are needed to achieve that speed

$$I_{Tmin}=\Delta V\sqrt{\frac{C_L}{3.1 L_{pmax}}}$$

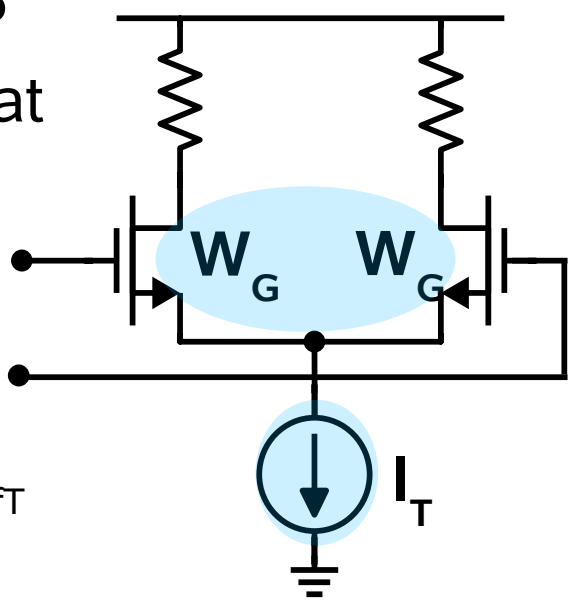
Inductive Broadbanding in Latches and Selector



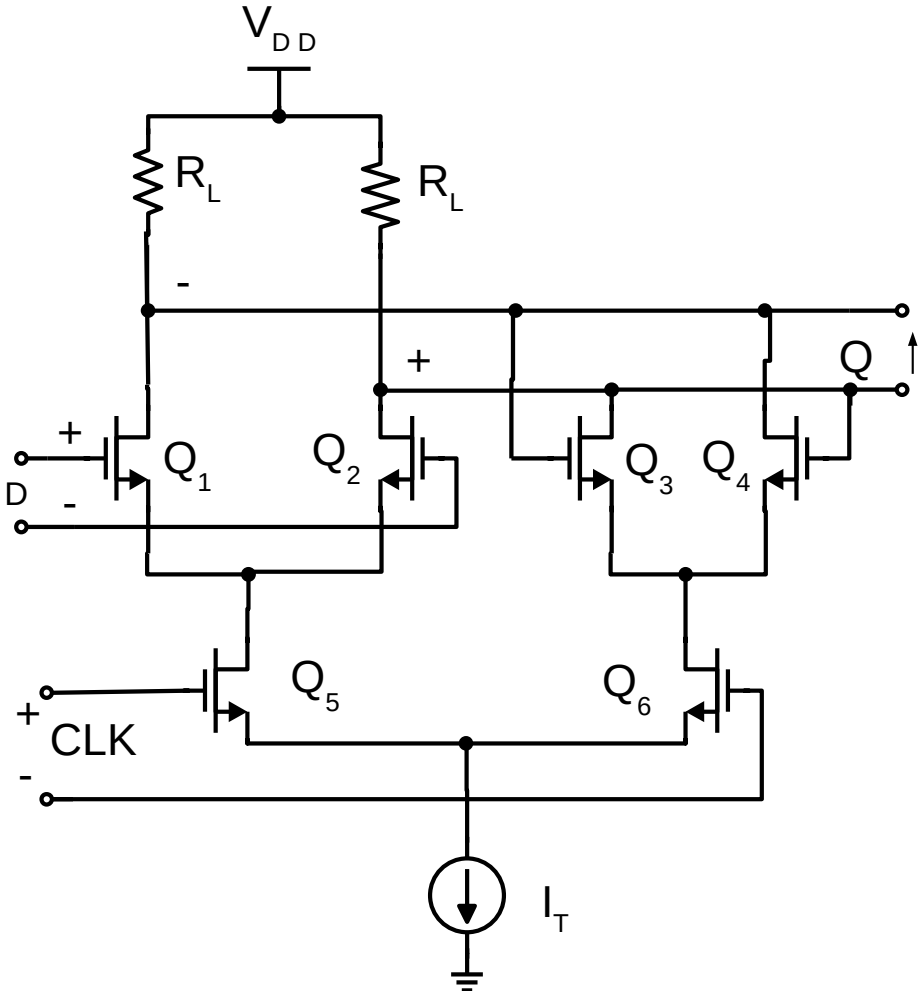
T. Suzuki *et al.*, *IEEE ISSCC Proc.*, pp.192-193, Feb. 2002.

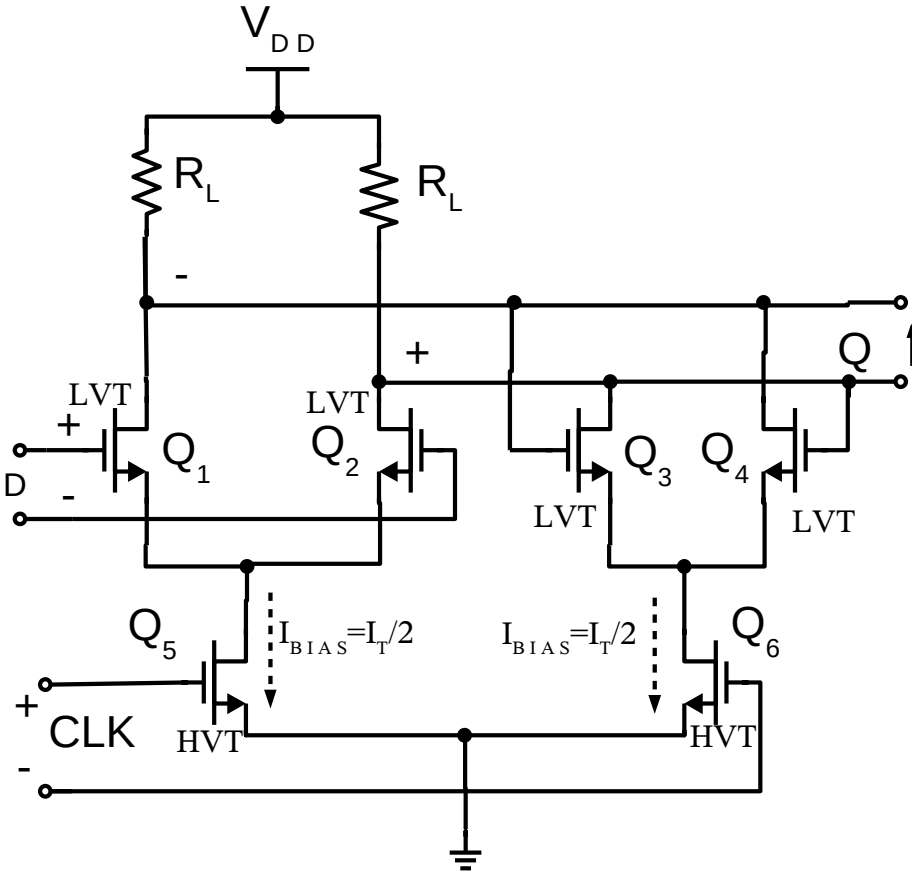
Design Methodology for Max. Speed

- Set $\Delta V = 1.5 \times \Delta V_{MIN}$ (600 mV in 130 nm, 400 mV in 90 nm, 250mVpp in BiCMOS)
- Set I_T as low as possible for given speed
- Size MOSFETs to be biased at $J_{pT}/2 = 0.15$ mA/μm with I_T at 0.3 mA/μm. HBTs biased at $3J_{pfT}/2$
- Start with inverters, add peaking and broadbanding,
- Add (if needed) EF/SF biased at 1/3 .. ½ J_{pfT}
- Optimize scaling ratio between stages: a 1.5 .. 2 ratio is a good start.



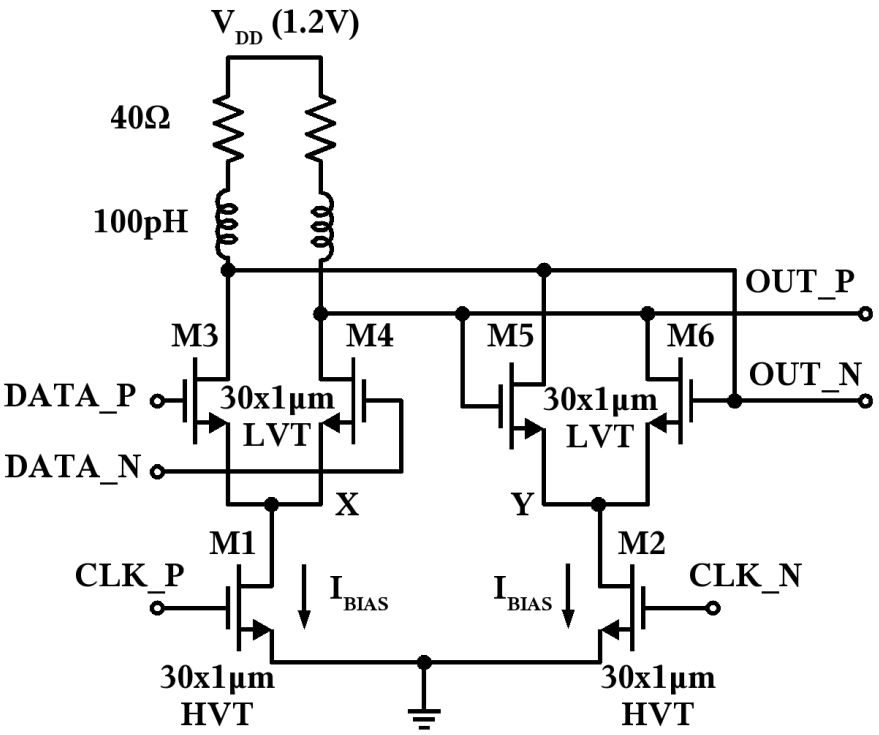
Pseudo-CML





- Need V_{DS} > 0.5 V to operate at 40+Gb/s => remove I_T
- V_{GS} of data-path FETs determines V_{DS} of clock-path FETs => LVT+HVT

Design Ex.: 1.2-V 90-nm CMOS latch



- No current source in clock-path
- High-V_T devices on clock path.
- $I_{BIAS}=I_{pfT}/2$ =0.15 mA/µm.
- To fully switch the 90-nm MOS diff pair at 0.15 mA/µm: $\Delta V > 300$ mV
- For I_{BIAS} = 4.5 mA and R_L = 40 Ω:

$$\Delta V=(I_{M1}+I_{M2})R_L=9mA\times 40\,\Omega=360mV$$

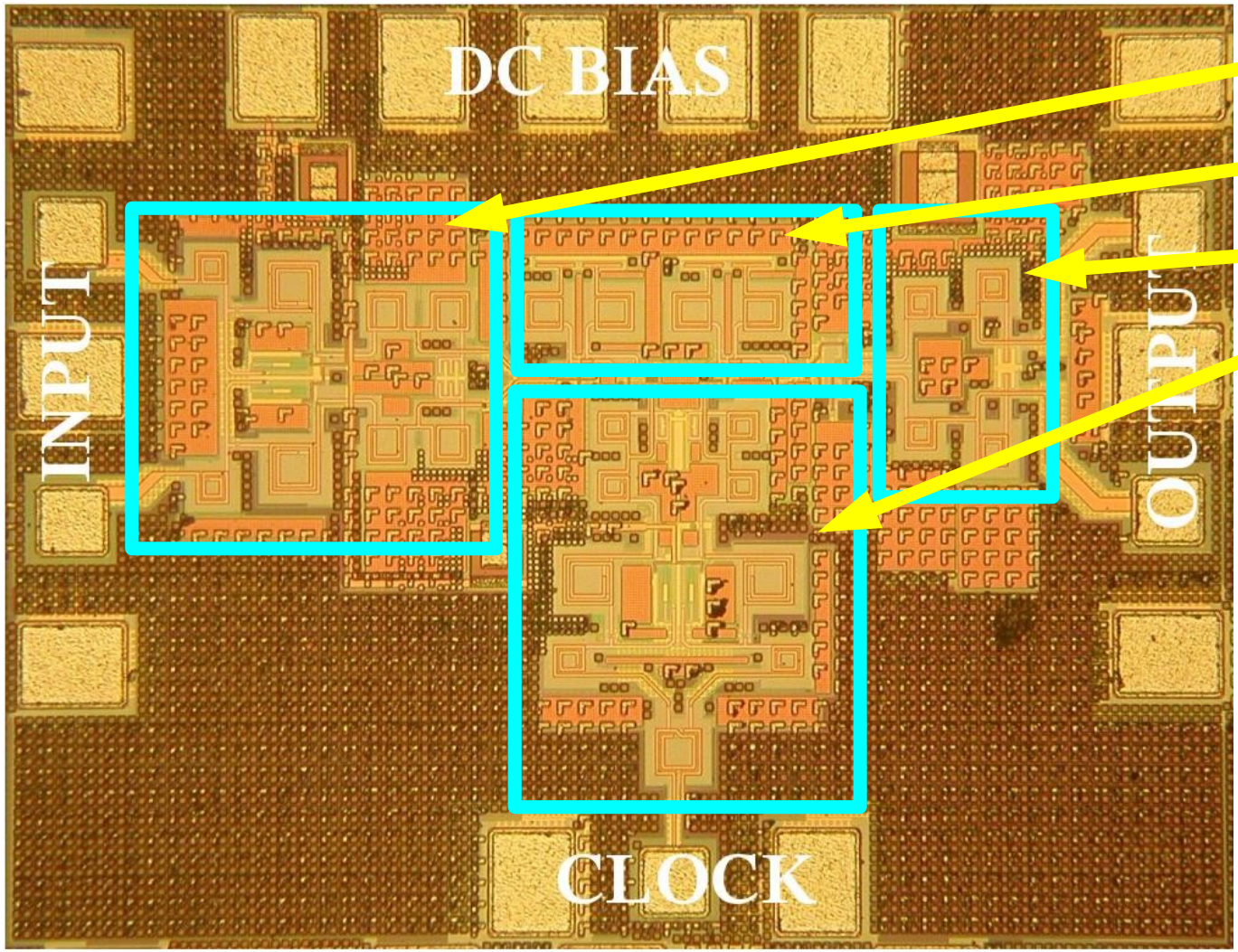
- Total capacitance at the drain of M3 (A_V = -1.2):

$$C_T=C_{db3}+C_{gd3}+C_{gd5}+C_{db5}+C_{gs6}+(1-A_V)C_{gd6}+k(C_{gs6}+(1-A_V)C_{gd})=197fF$$

- L = 100 pH extends the BW to:
- Power consumption: 10.8 mW/latch.

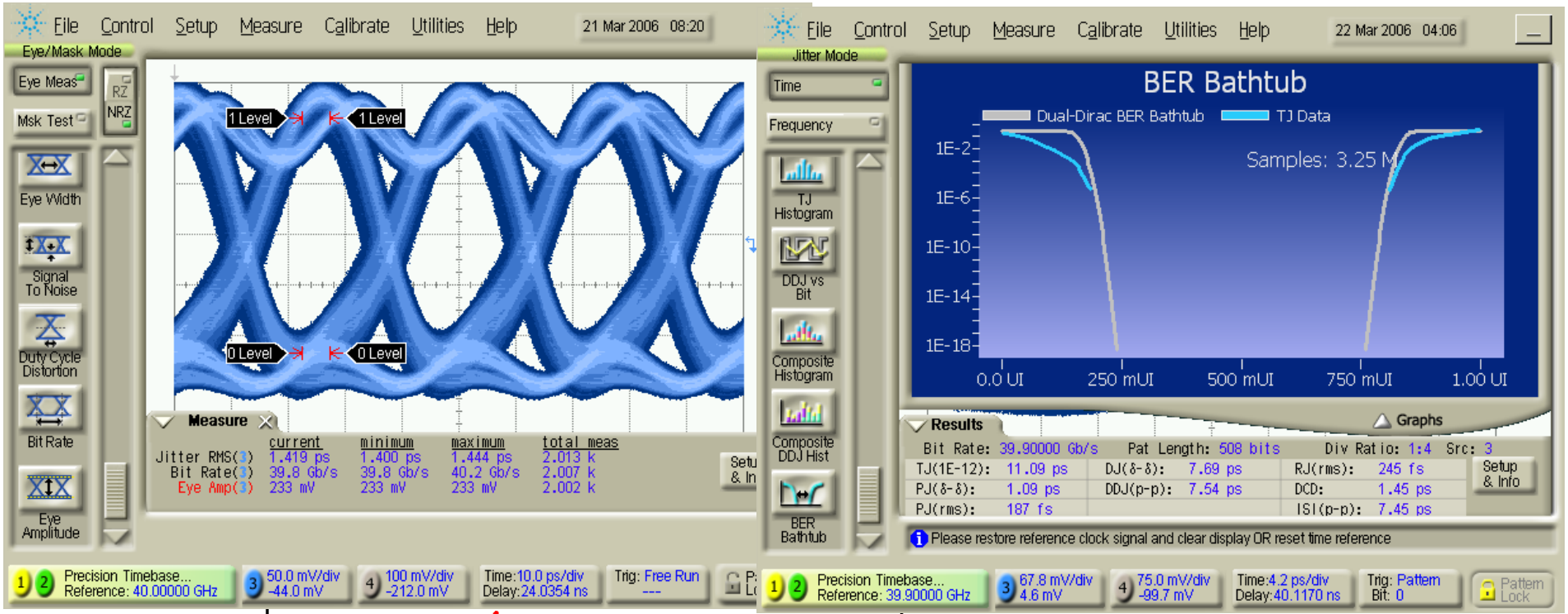
$$BW_{3dB}=\frac{1.6}{2\pi R_L C_T}=32.3GHz$$

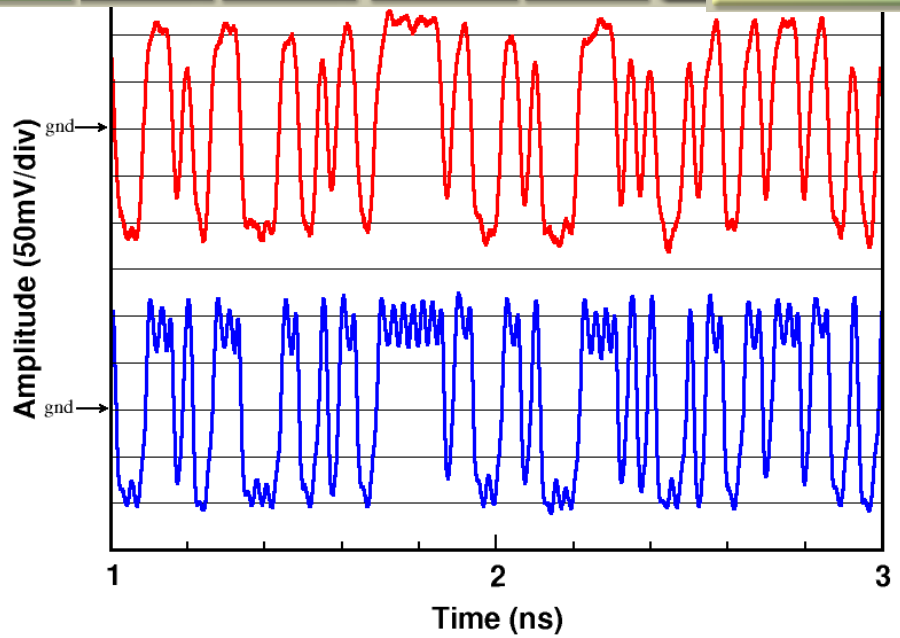
Retiming DFF – Die Photo



- TIA
- DFF
- Output driver
- Clock tree
- P = 130 mW @ V_{DD} = 1.2 V
- Area = 600x800 μm^2

Measurements at 40 Gb/s and 1.5 V



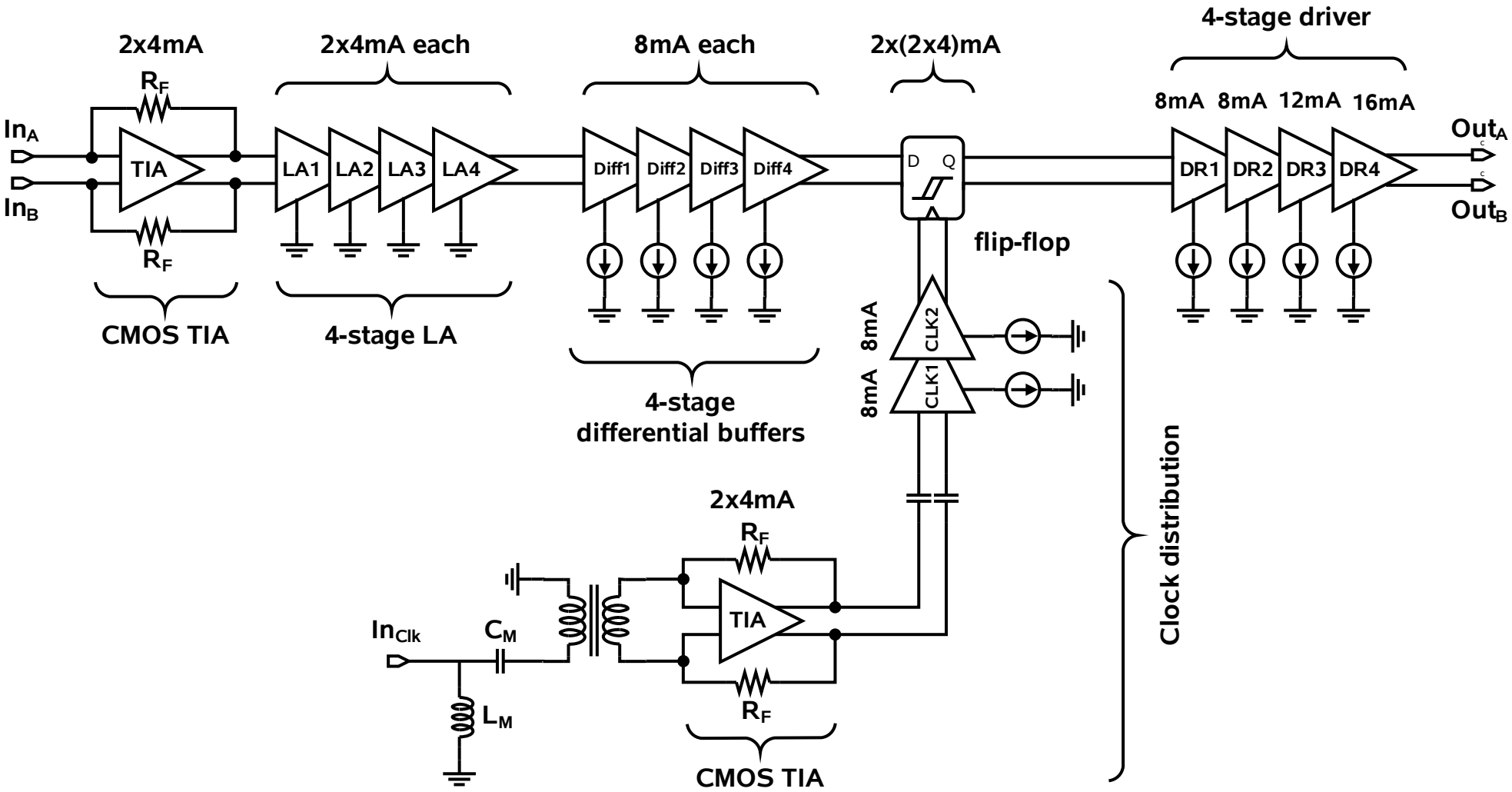


- Error-free 508-bit pattern.
- Input (top), output (bottom).
- BER not measured due to limitations of test setup.

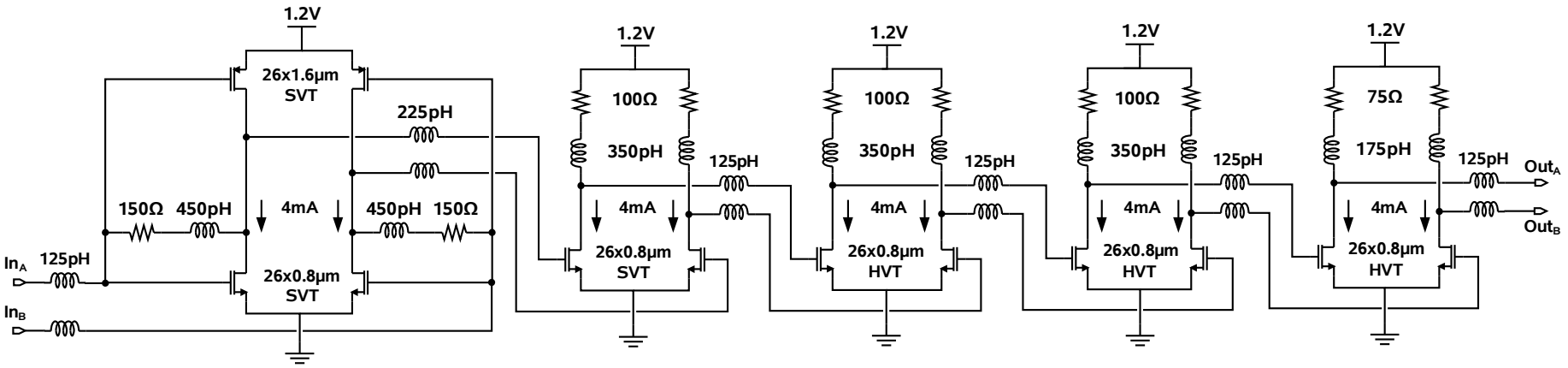
An 81Gb/s, 1.2V TIALA-Retimer in Standard 65-nm CMOS

Shahriar Shahramian et al.
IEEE CSICS-2008

Block Diagram

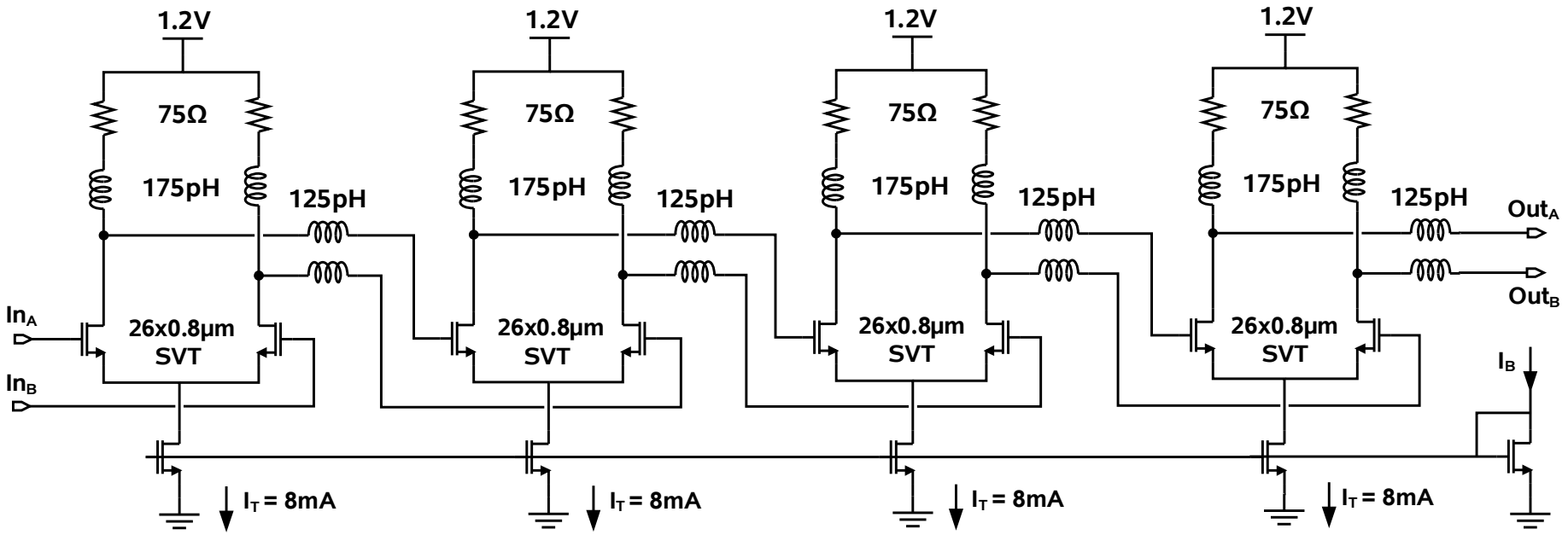


TIALA schematics



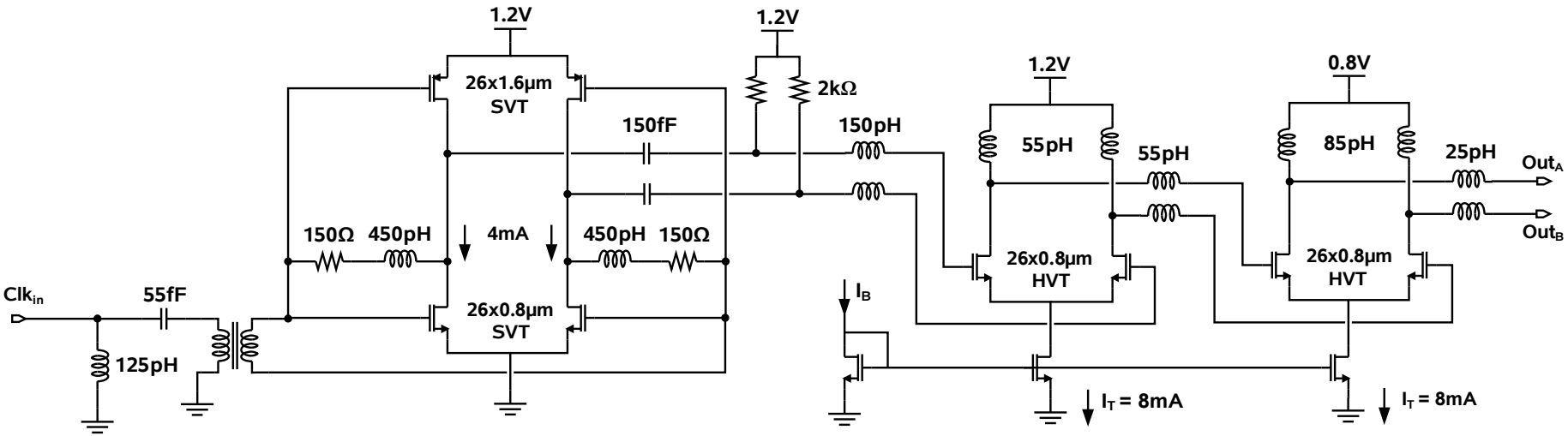
- Simulated small-signal gain is 20.5dB with a 3dB bandwidth of 44GHz.

Single-ended to differential conversion



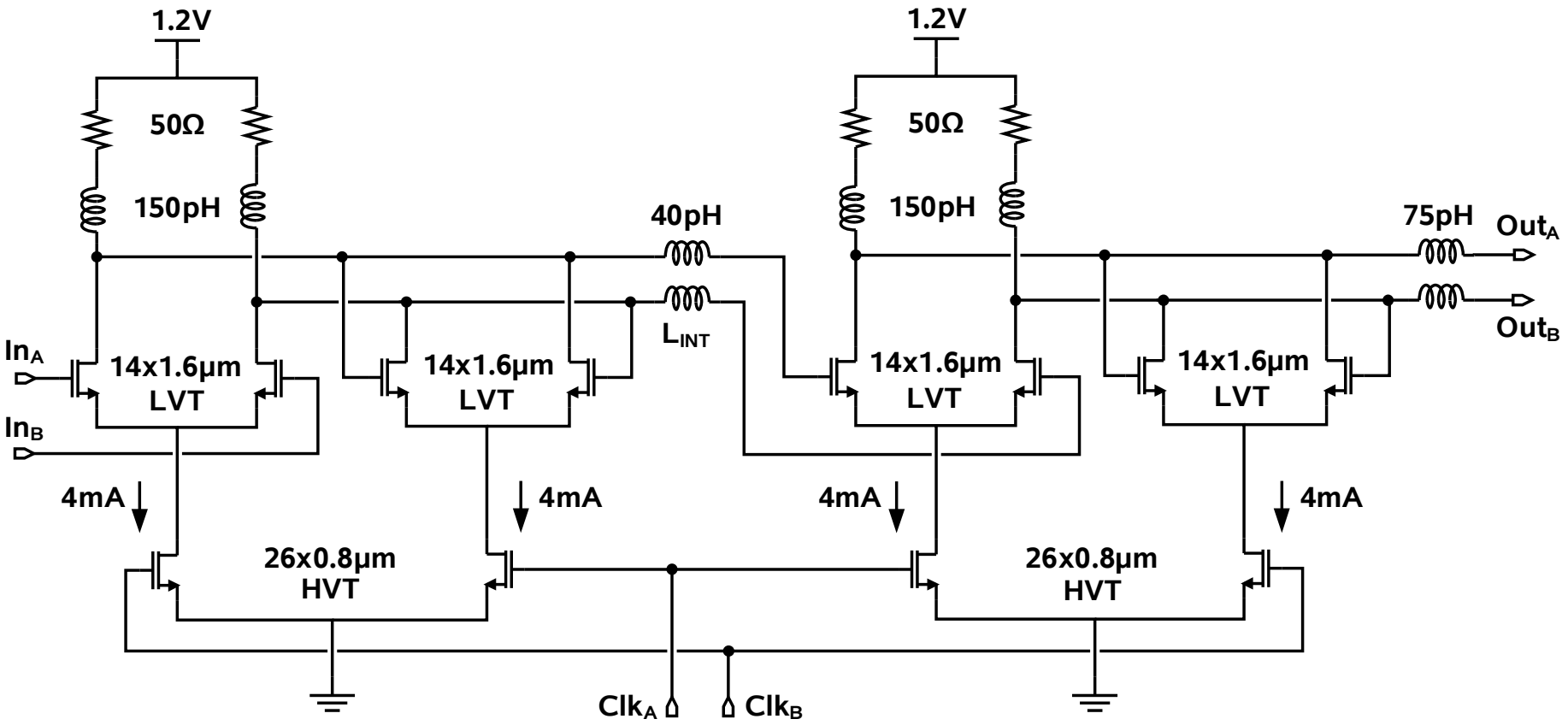
- Differential pairs with active current sources provide single-ended to differential conversion.

Clock distribution network



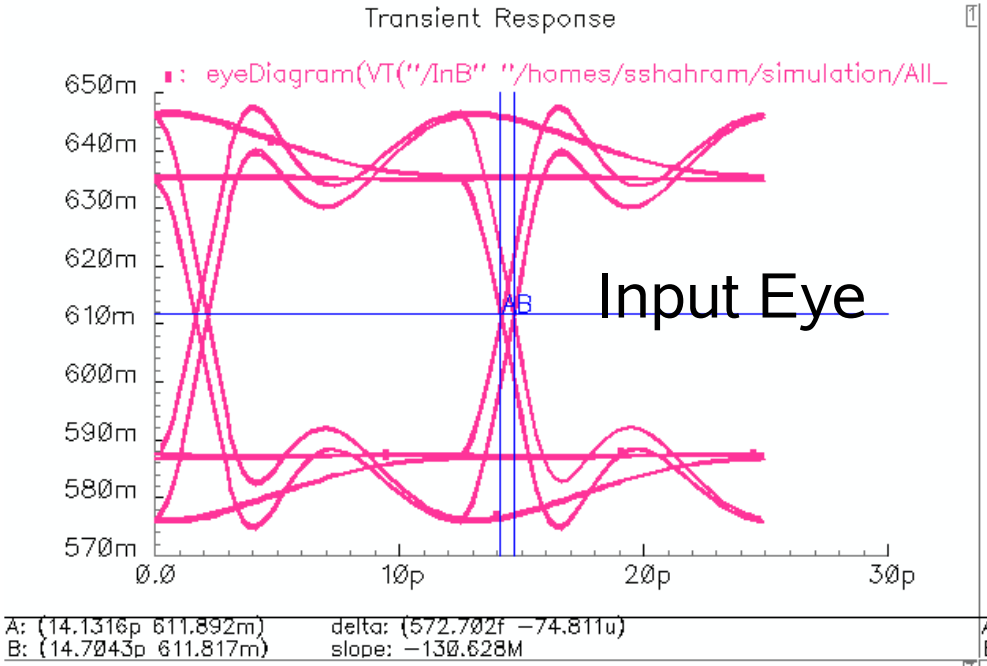
- Simulated differential, small-signal gain of 6dB between 50GHz and 85GHz.

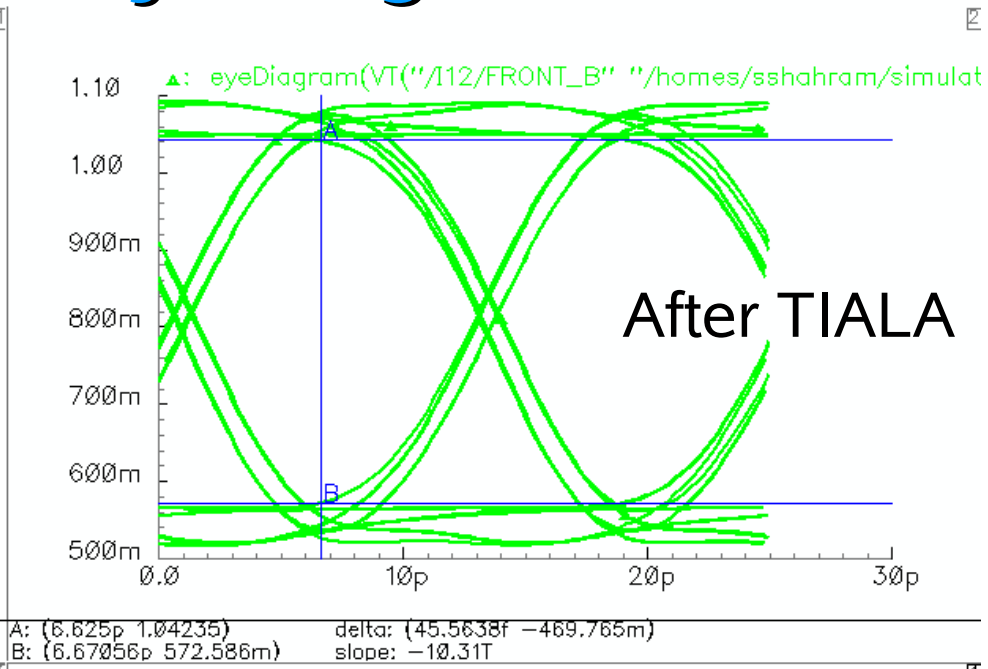
81-Gb/s flip-flop schematic

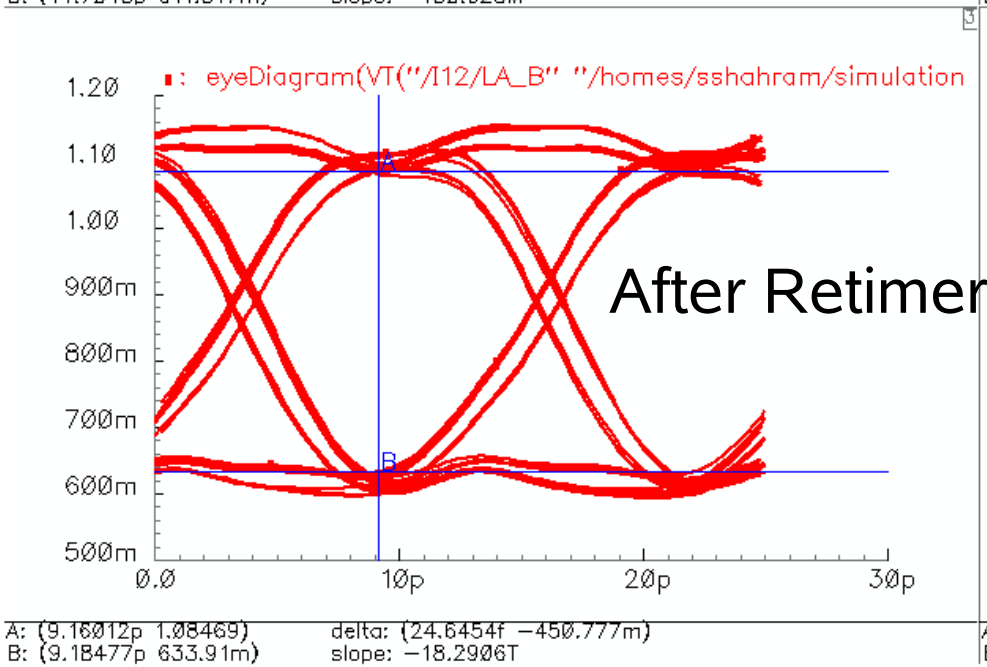


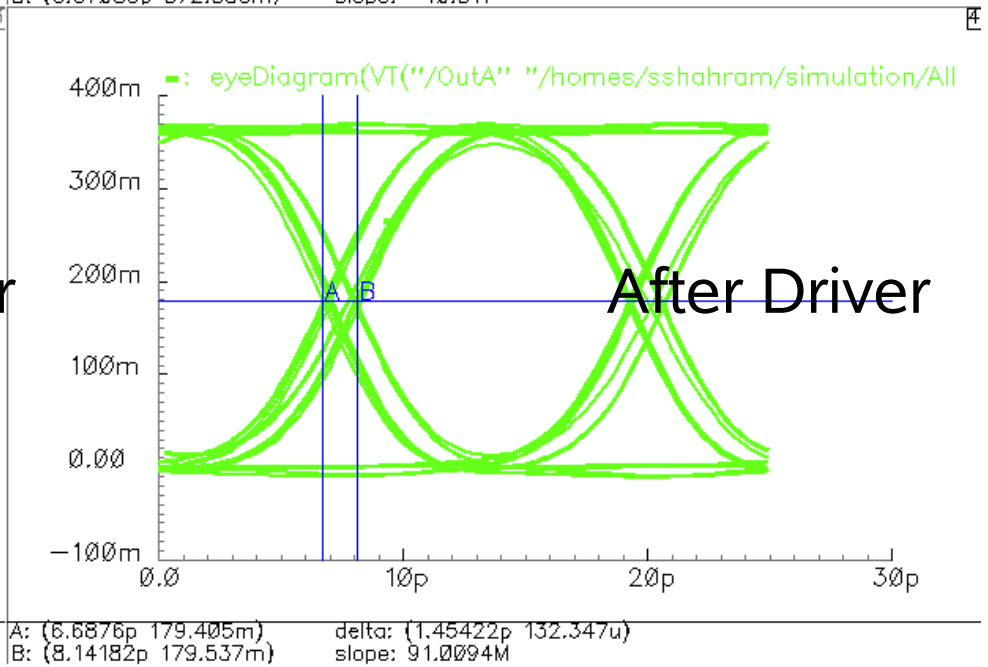
- Combination of HVT and LVT transistors allows for operation from 1.2V.

Simulated 80Gb/s eye-diagrams

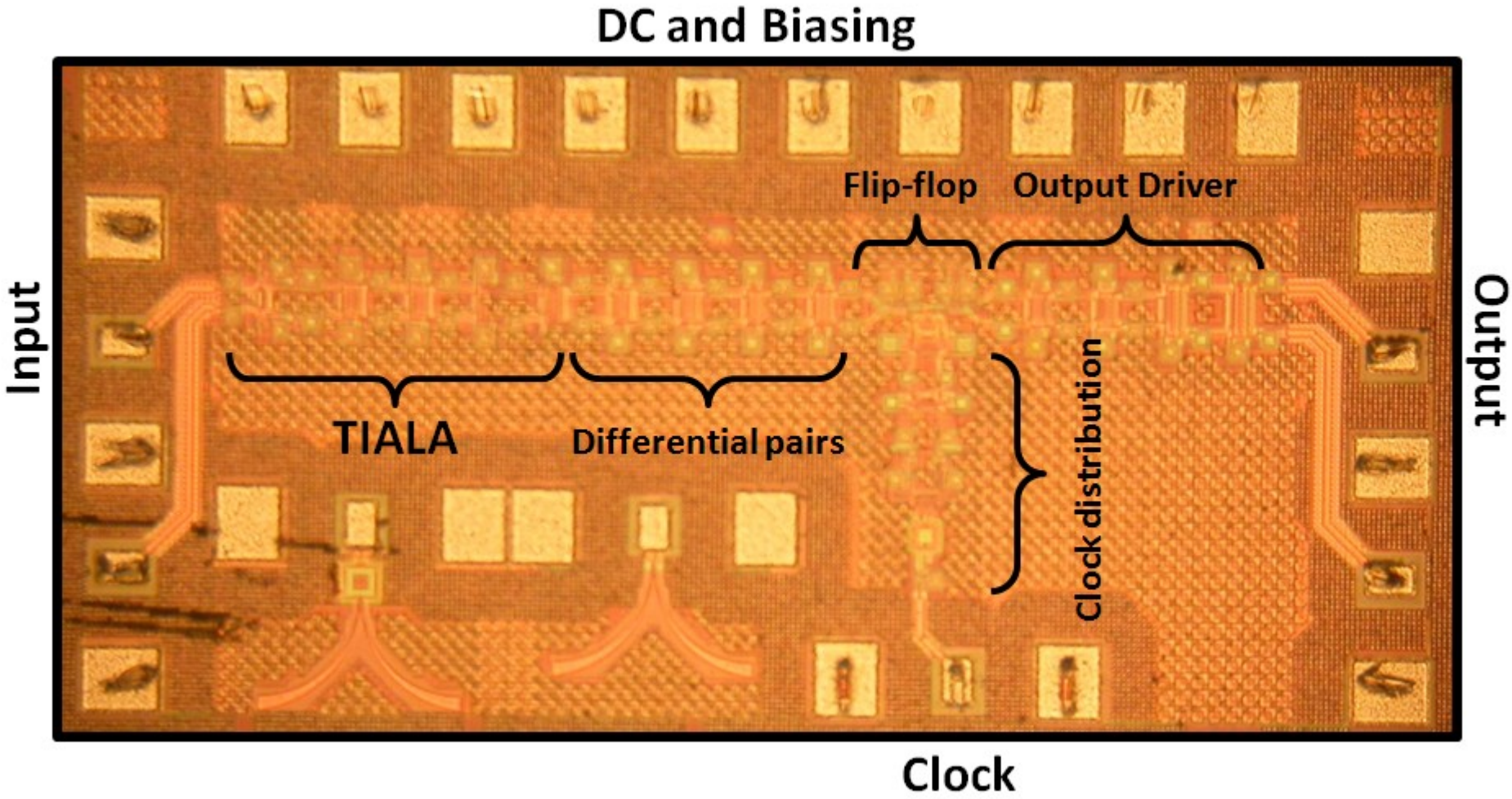






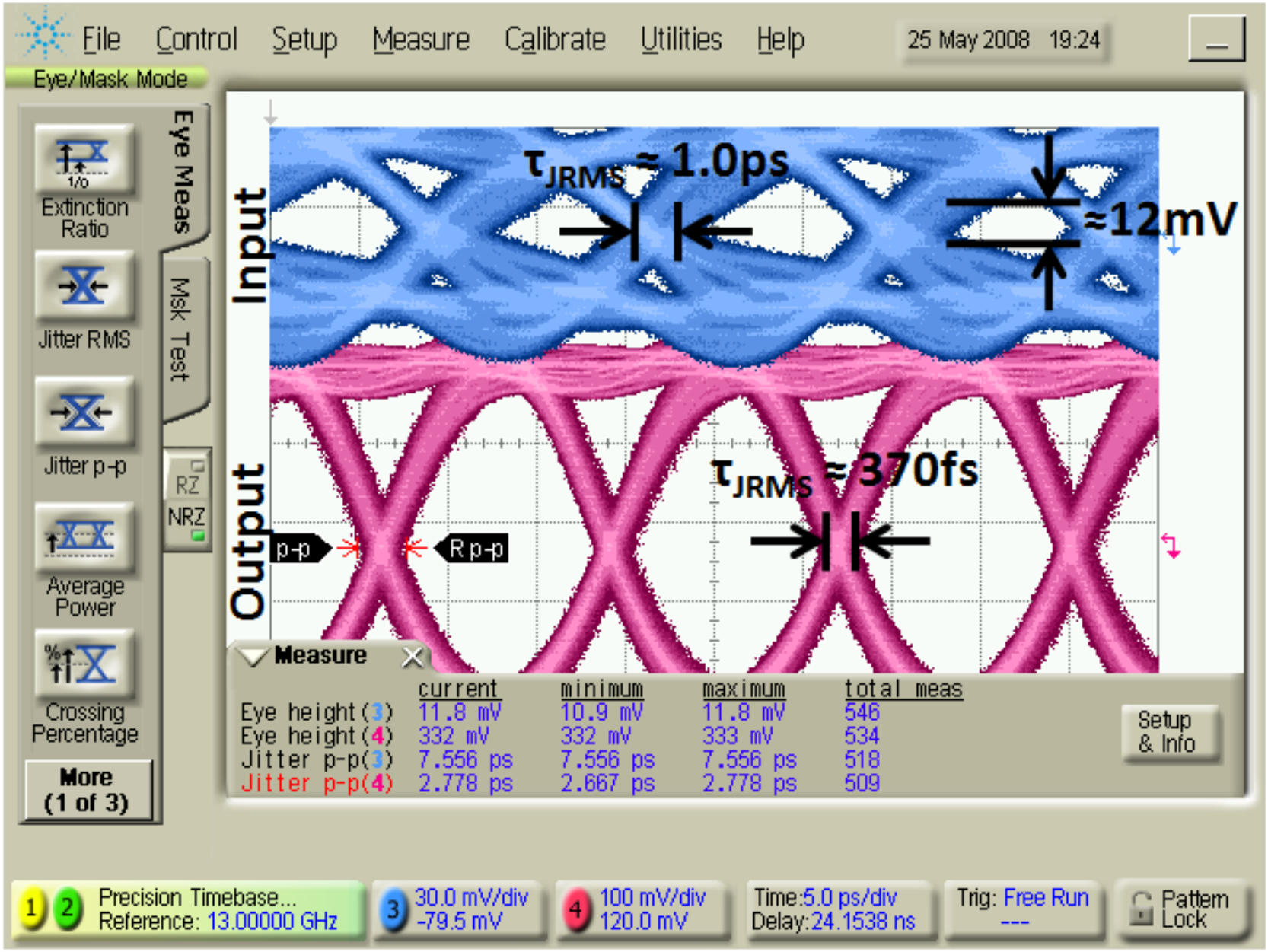


Die photograph

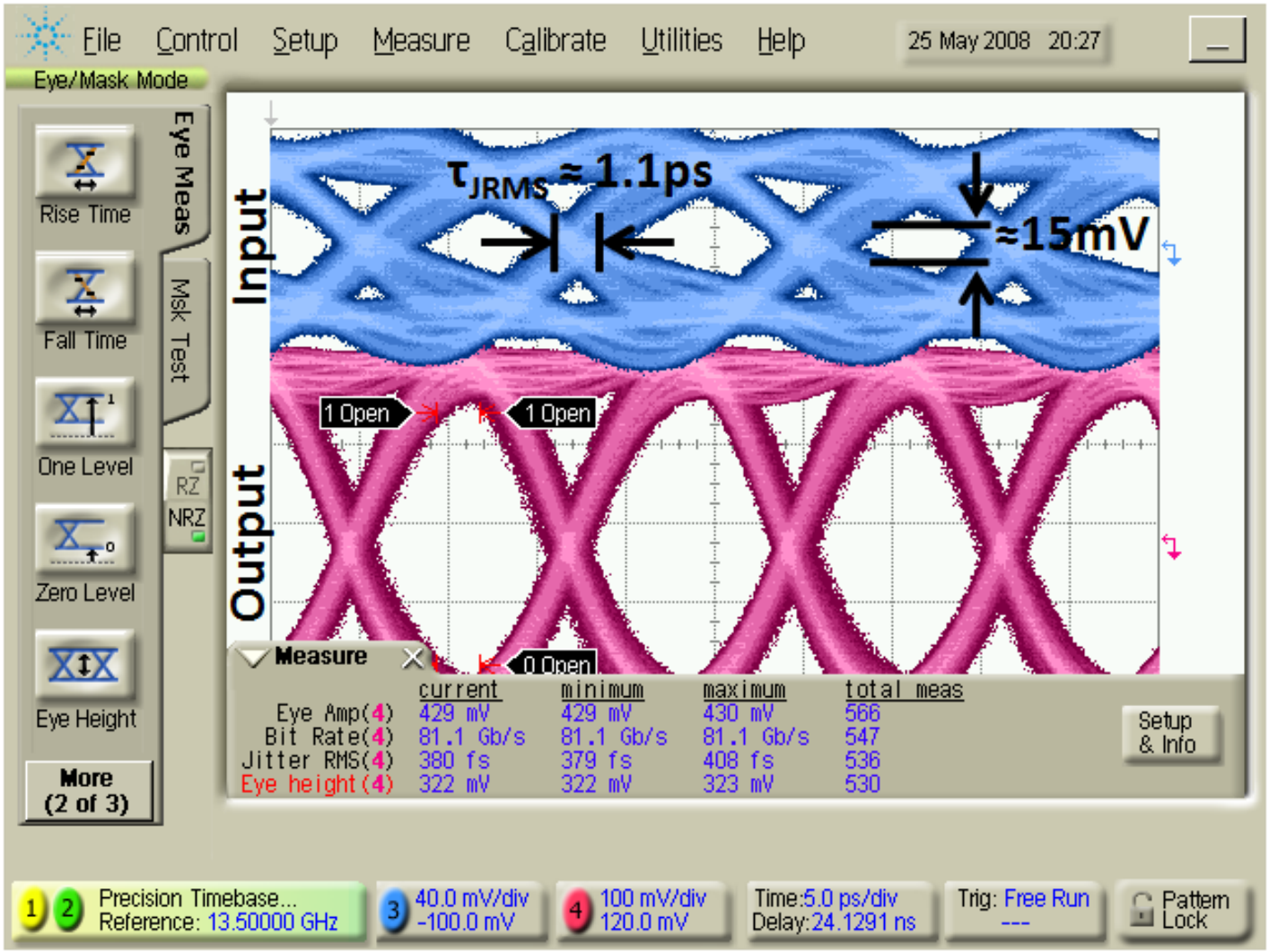


- 0.57mm x 1.2mm
- Vdd = 1.2V, Total Power = 200mW

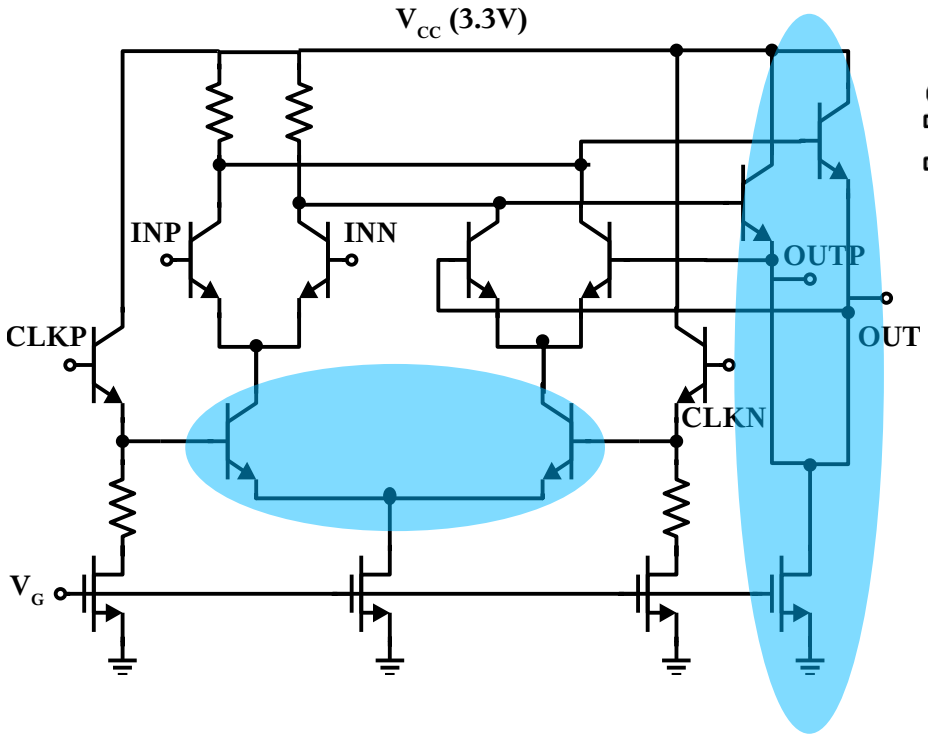
Measurement result: 78Gb/s

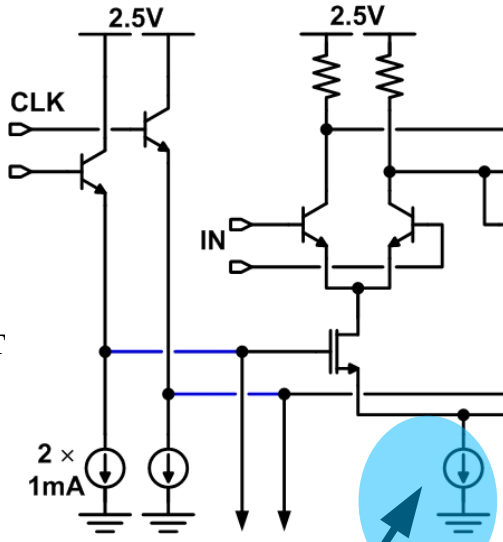


Measurements: 81Gb/s with 80 mV_{pp} input

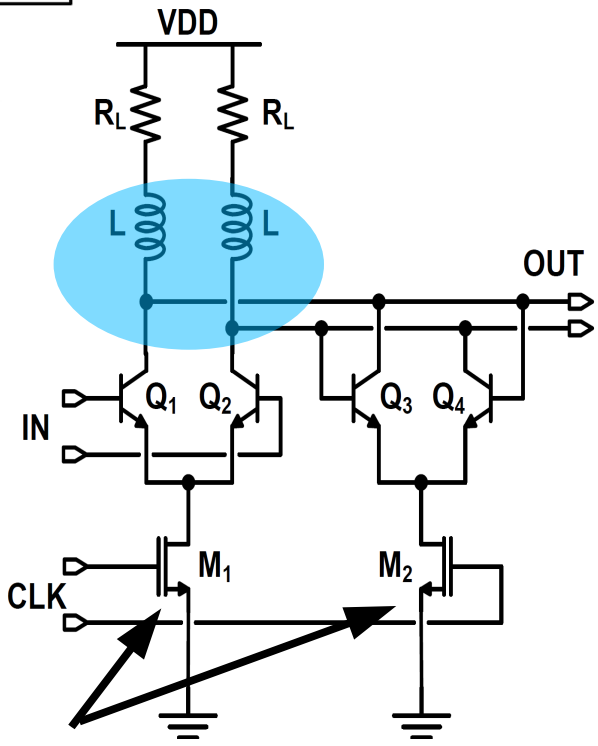


MOS-HBT (pseudo) CML





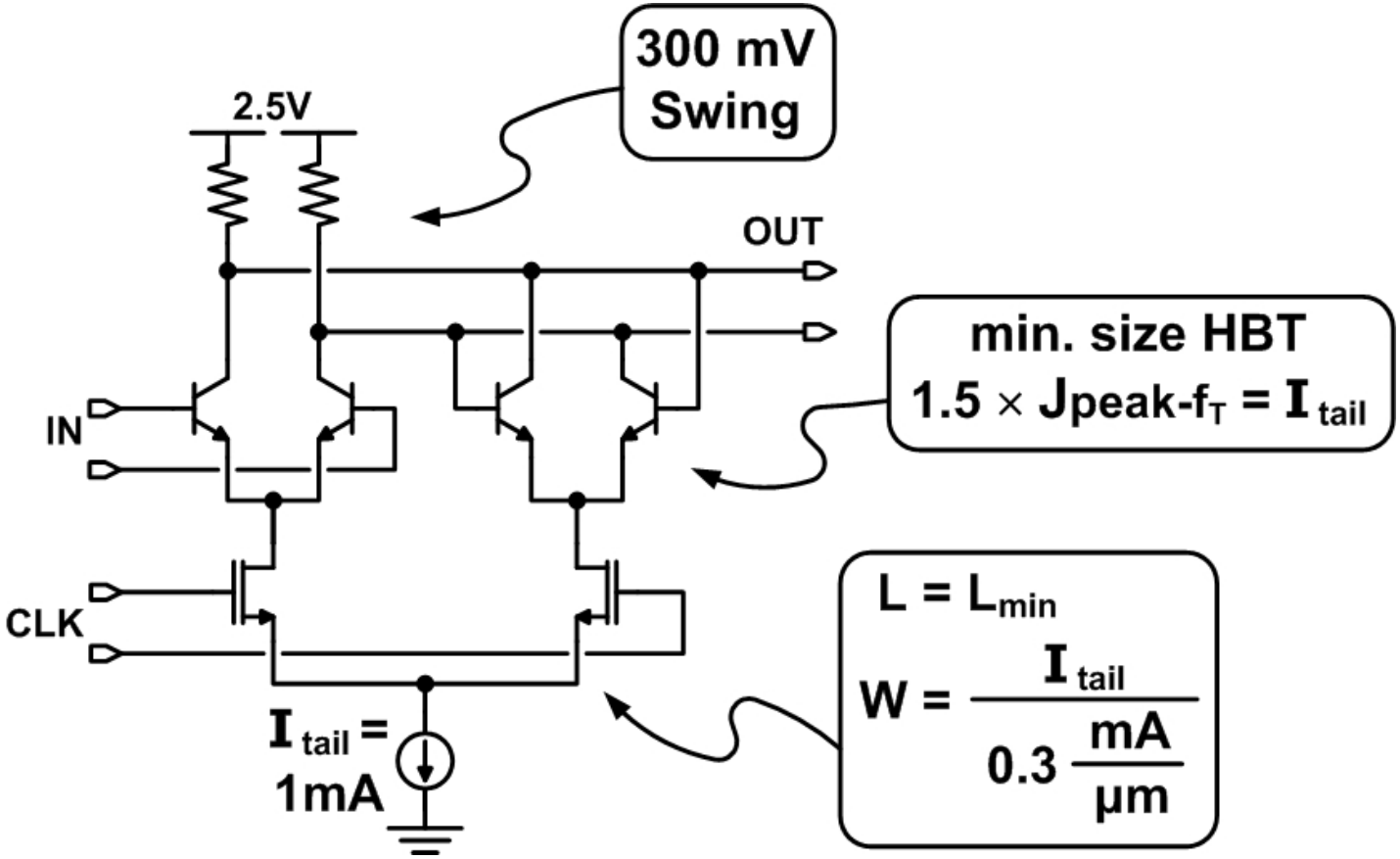
0.3mA/μm



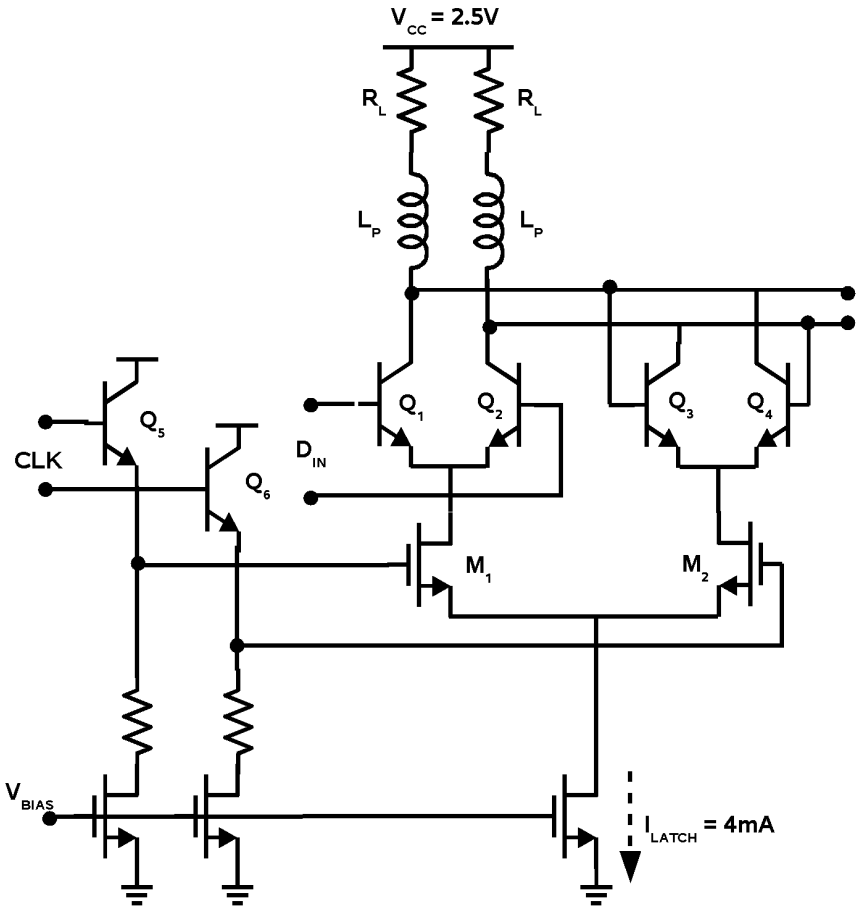
0.15mA/μm

- HBT ECL to BiCMOS CML
- 3.3 V to 2.5 V and reduced number of tails
- 1.8 V (lower power) at same speed
- Inductive peaking to increase speed

12-GHz Latch Design (E Laskin, CSICS-2005)



43-Gb/s BiCMOS CML Latch Design Example



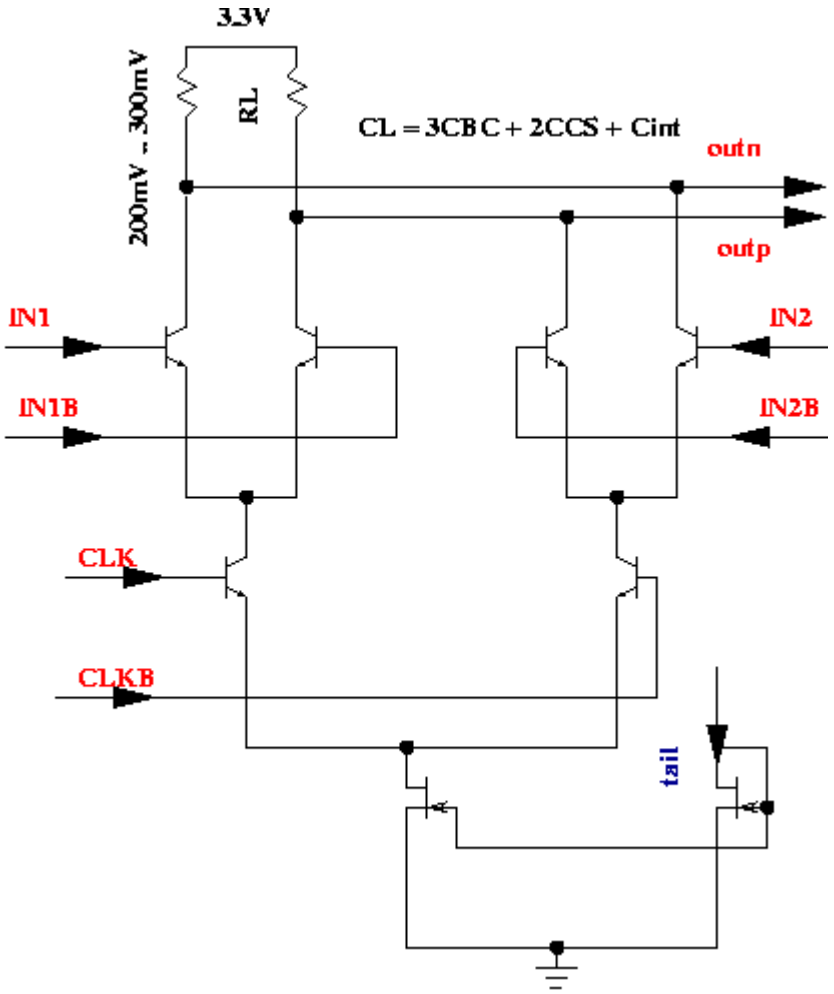
- J_{pfT}= 8mA/μm, C_{be}=23.2pF×I_C, C'_{cs} =1.1fF/μm, $C_{'bc}$=11fF/μm^2, A_V=2.85
- W(M1,M2) = I_T/0.3mA/μm = 4mA/0.3=13μm
- I_E(Q1-Q4) = 4mA/(0.17μm×12mA/μm)=2μm
- I_E(Q5-Q6) = 2mA/(0.17μm×4mA/μm)=3μm
- R_L = ΔV/I_T = 300mV/4mA = 75Ω
- L=130pH for k=1 & 184pH for k=2

$$C_T = C_{cs1} + C_{bc1} + C_{bc4} + C_{cs4} + C_{be3} + (1 - A_V)C_{bc3} + k\left(C_{be} + (1 - A_V)C_{bc}\right) = 72\text{fF}$$

$$BW_{3dB} = 1.6 \times \frac{1}{2\pi R_L C_T} = 47\text{GHz}\ (33.8\text{GHz for } k = 2)$$

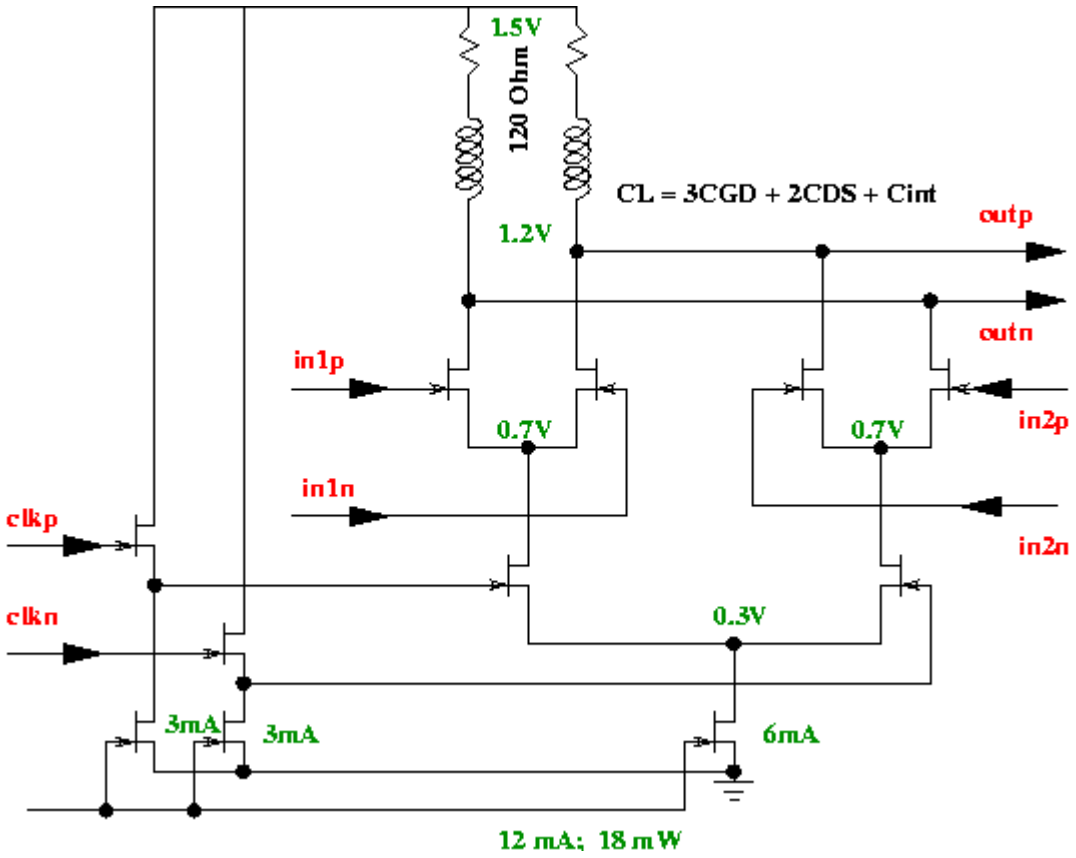
Examples of Logic Gates

Selector: BiCMOS CML



- n-MOS current tails for voltage headroom
- Inductive peaking may be needed

Selector: CMOS CML (60 Gb/s in 90-nm)

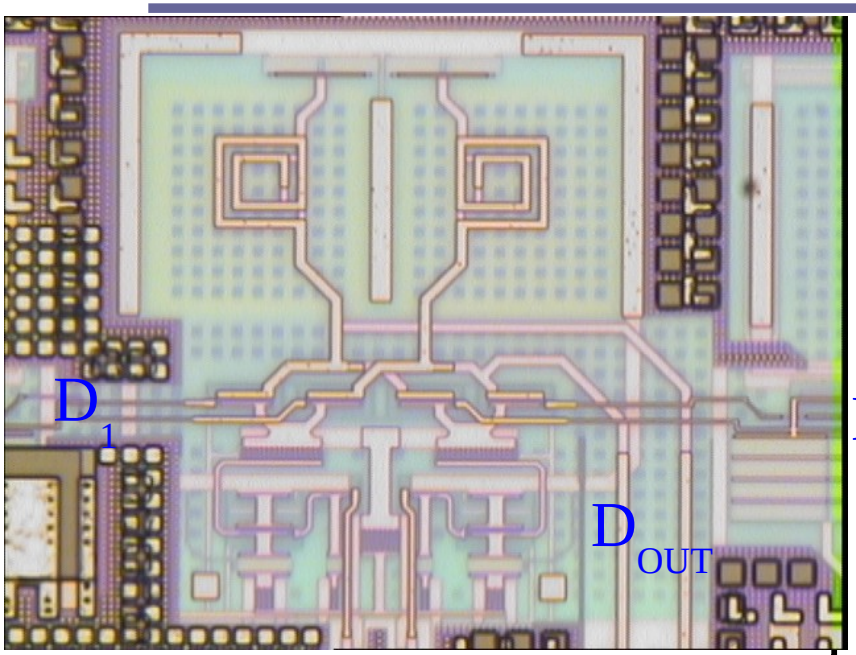


- Inductive peaking
- n-MOS only
- source follower for clock level
- reduced swing for headroom

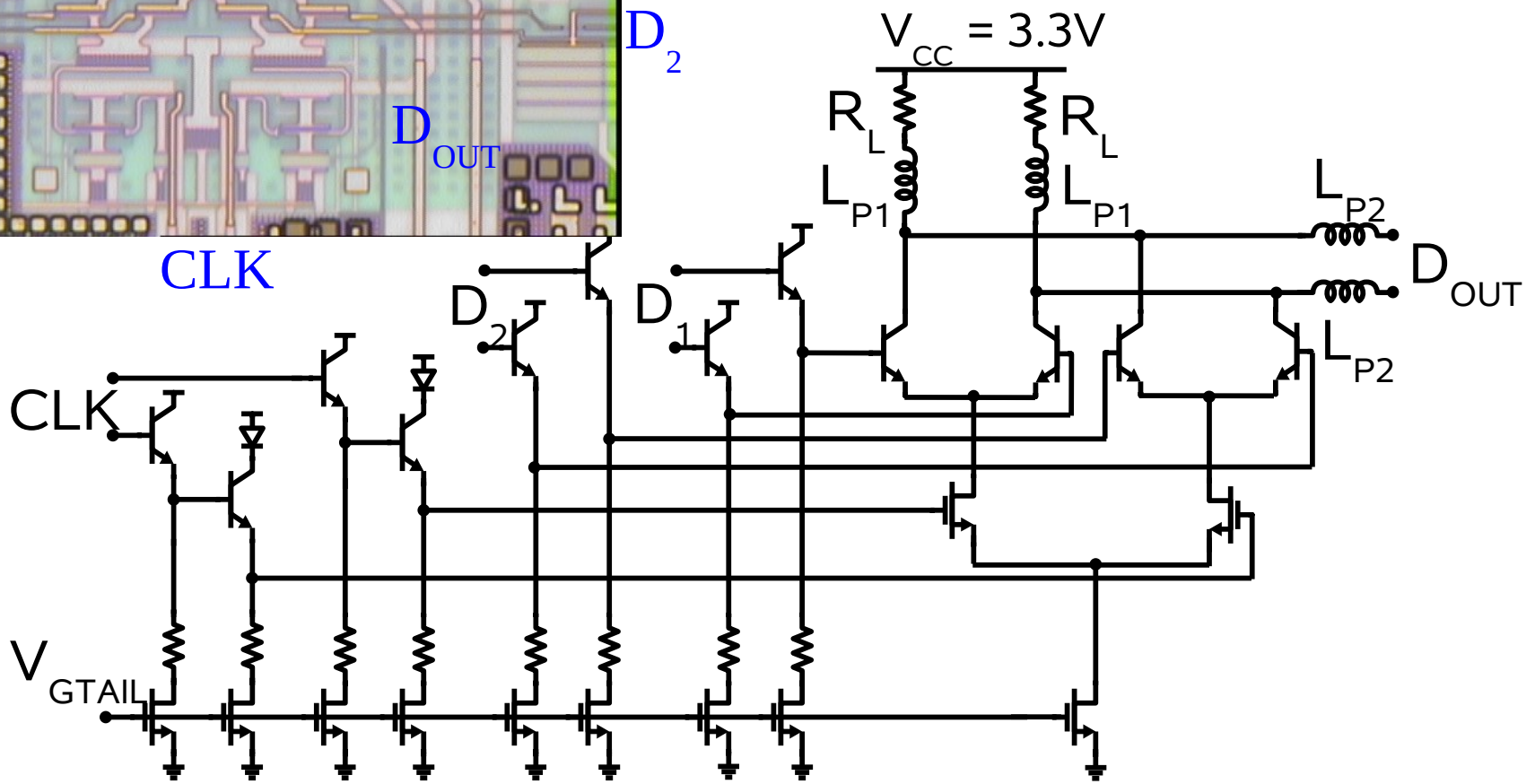
Broadcom patent US 2002/0017921 A1:

"Current-controlled CMOS circuits with inductive ***broadbanding***"

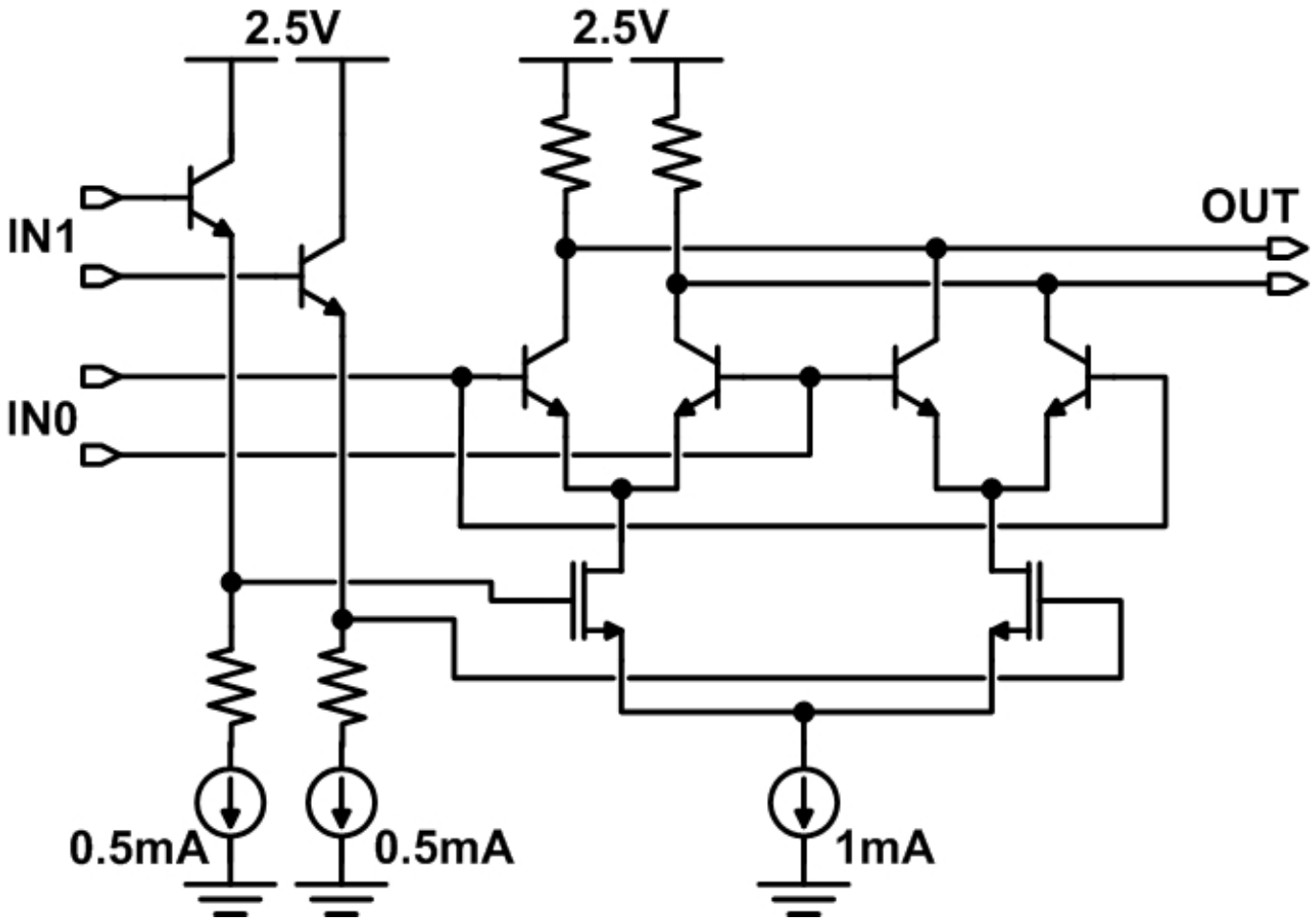
Selector: BiCMOS 80-Gb/s
(T. Dickson et al, ISSCC-2005)



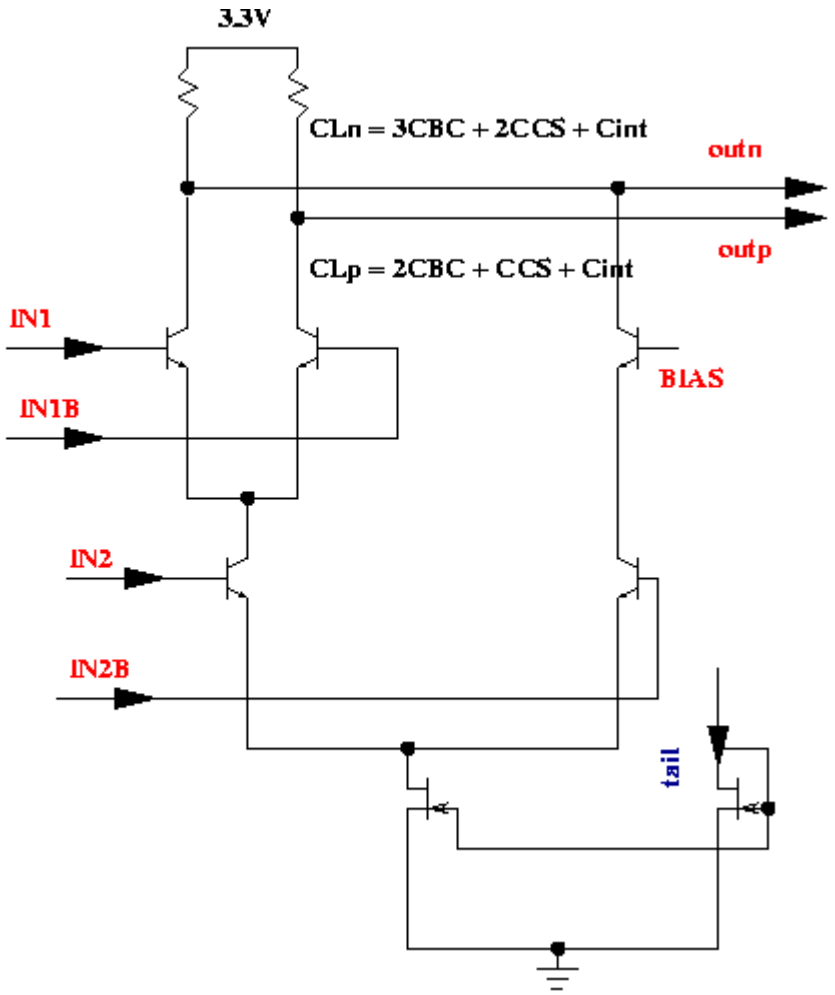
- EF^2 & series-shunt peaking for highest speed
- 3-D stacked inductor



BiCMOS CML XOR Schematic (E. Laskin CSICS-2005)

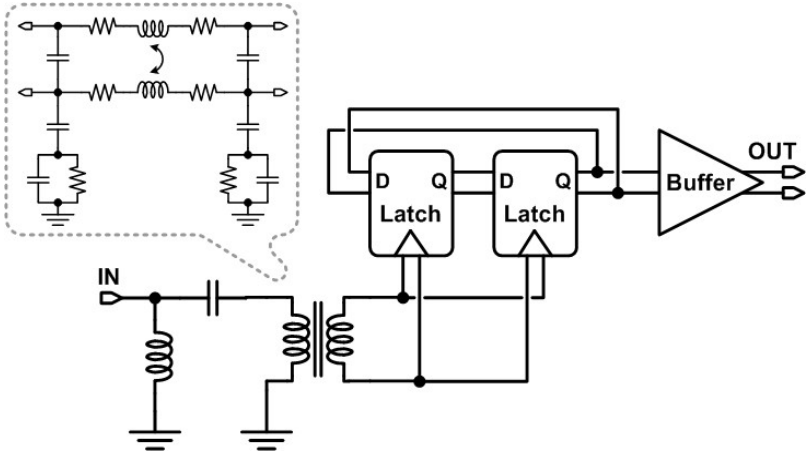


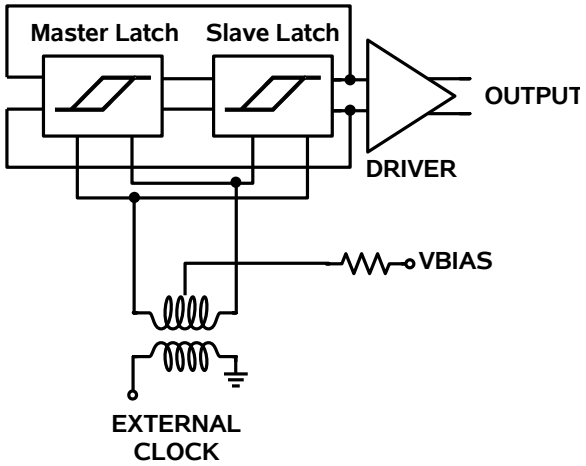
AND: BiCMOS CML

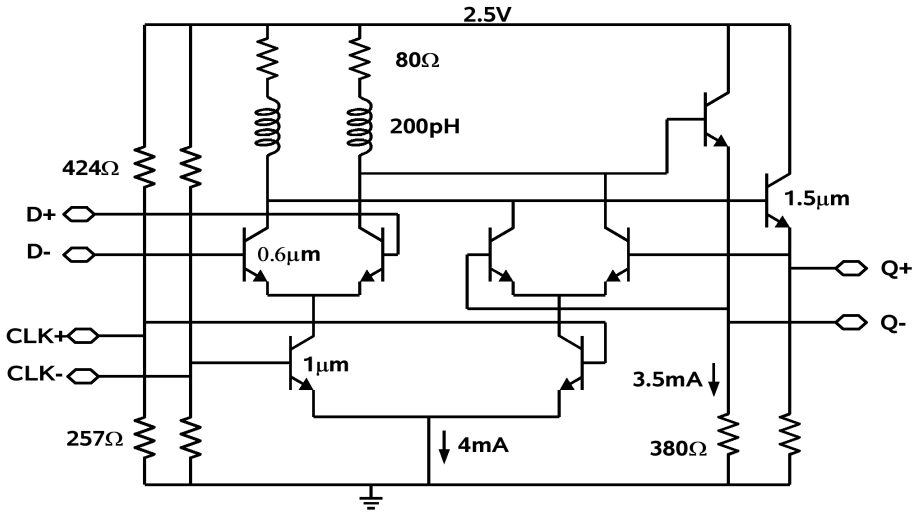


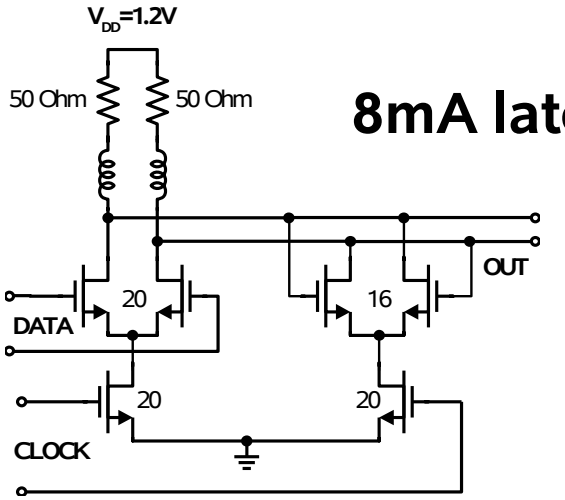
- n-MOS current tails for voltage headroom
- Cascode for good isolation and symmetry

Divide-by-2 block diagram and latch schematics



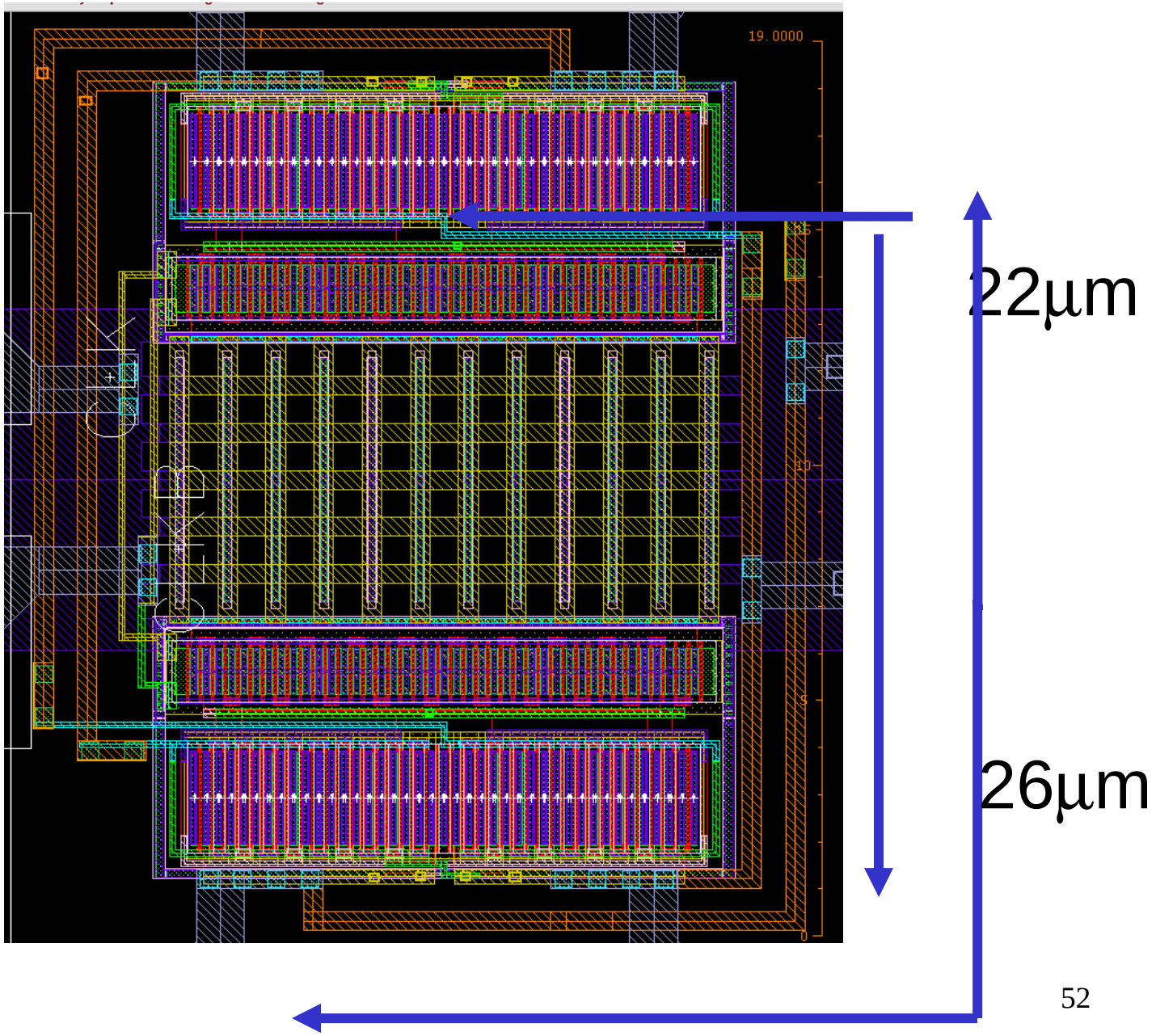




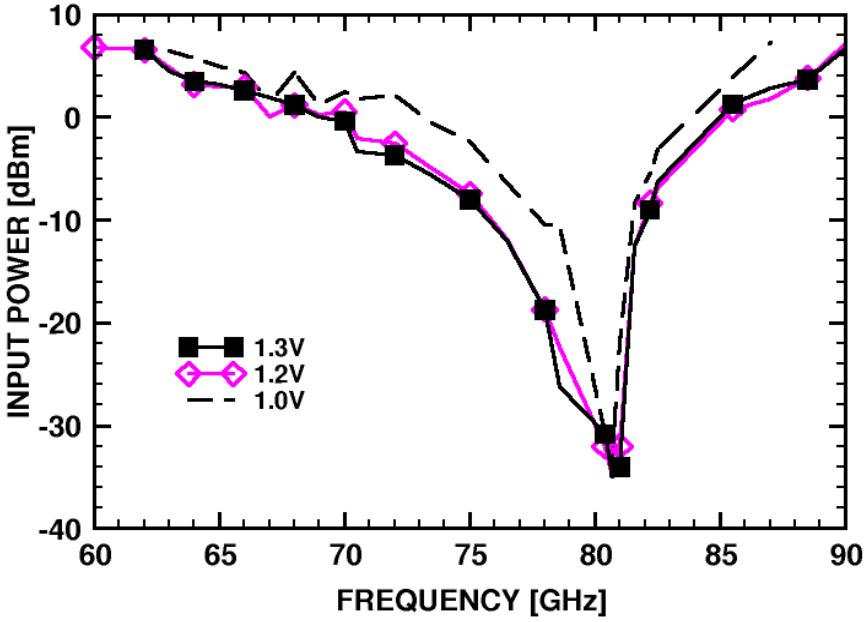


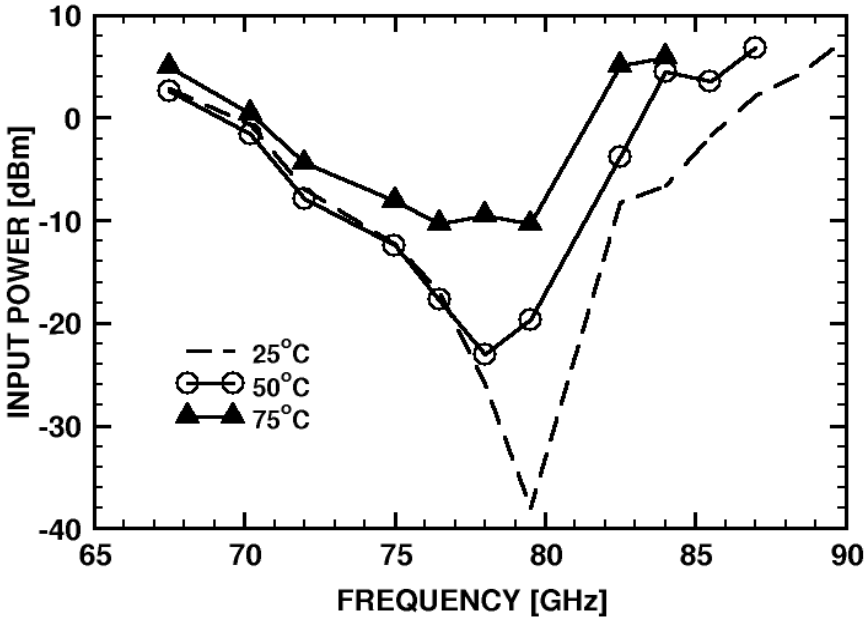
8mA latch

Divider layout (20 x 16 µm²)



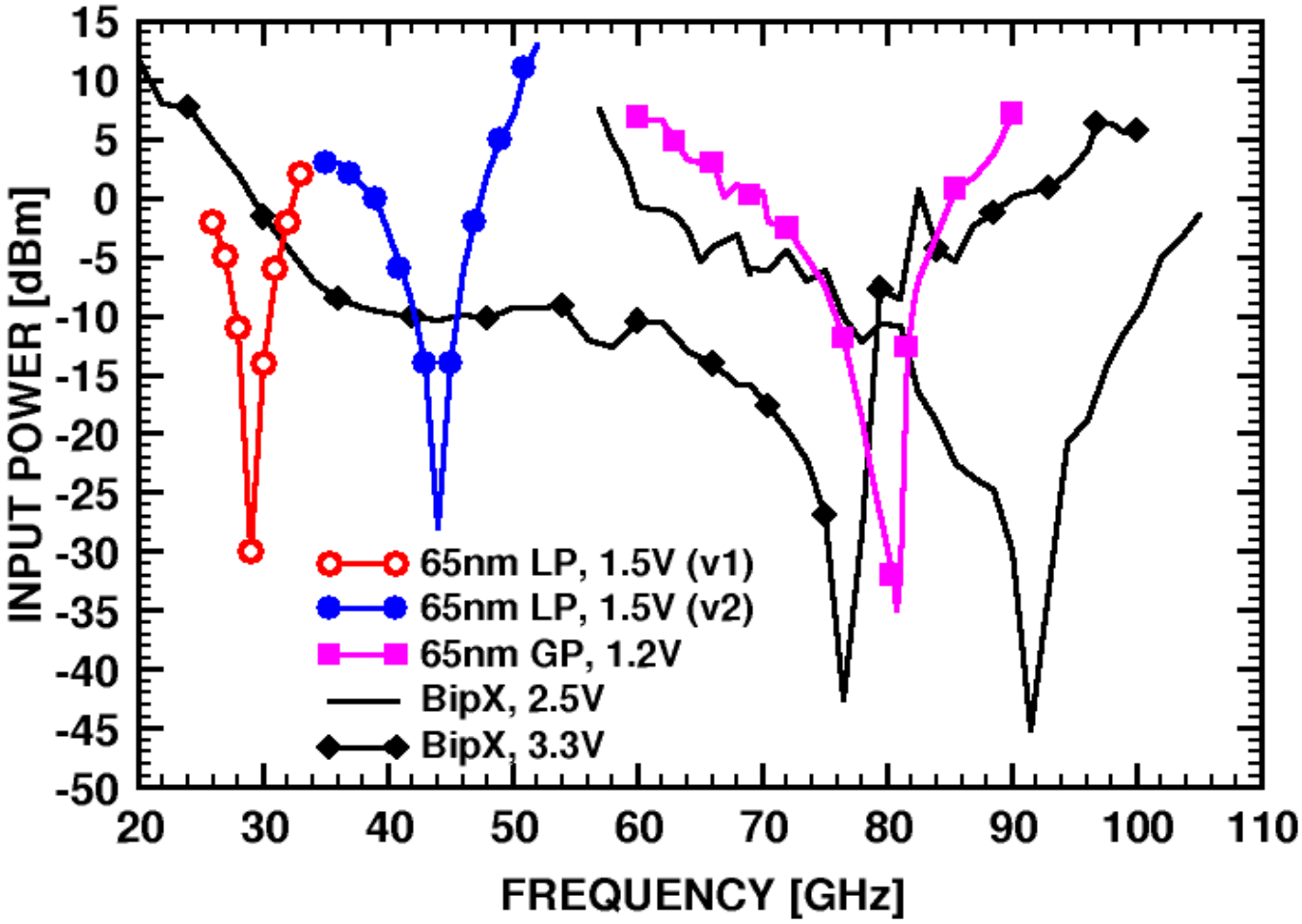
PVT performance of 65-nm GP CMOS divider



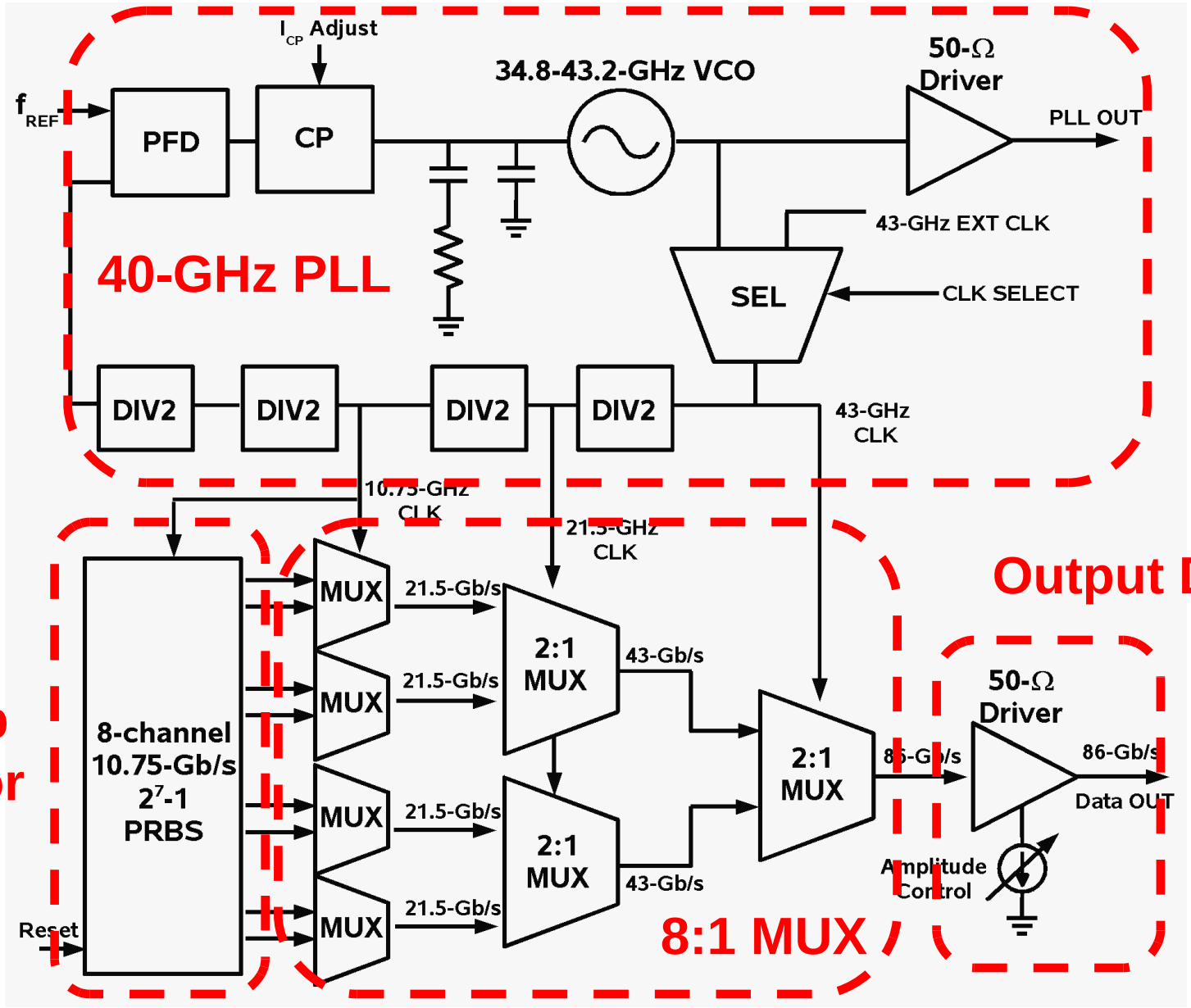


- Operates up to 78.5 GHz at 100 ^{0}C from 1.1V supply and at 80 GHz at 125 ^{0}C from 1.4 V
- Does not divide below 57GHz

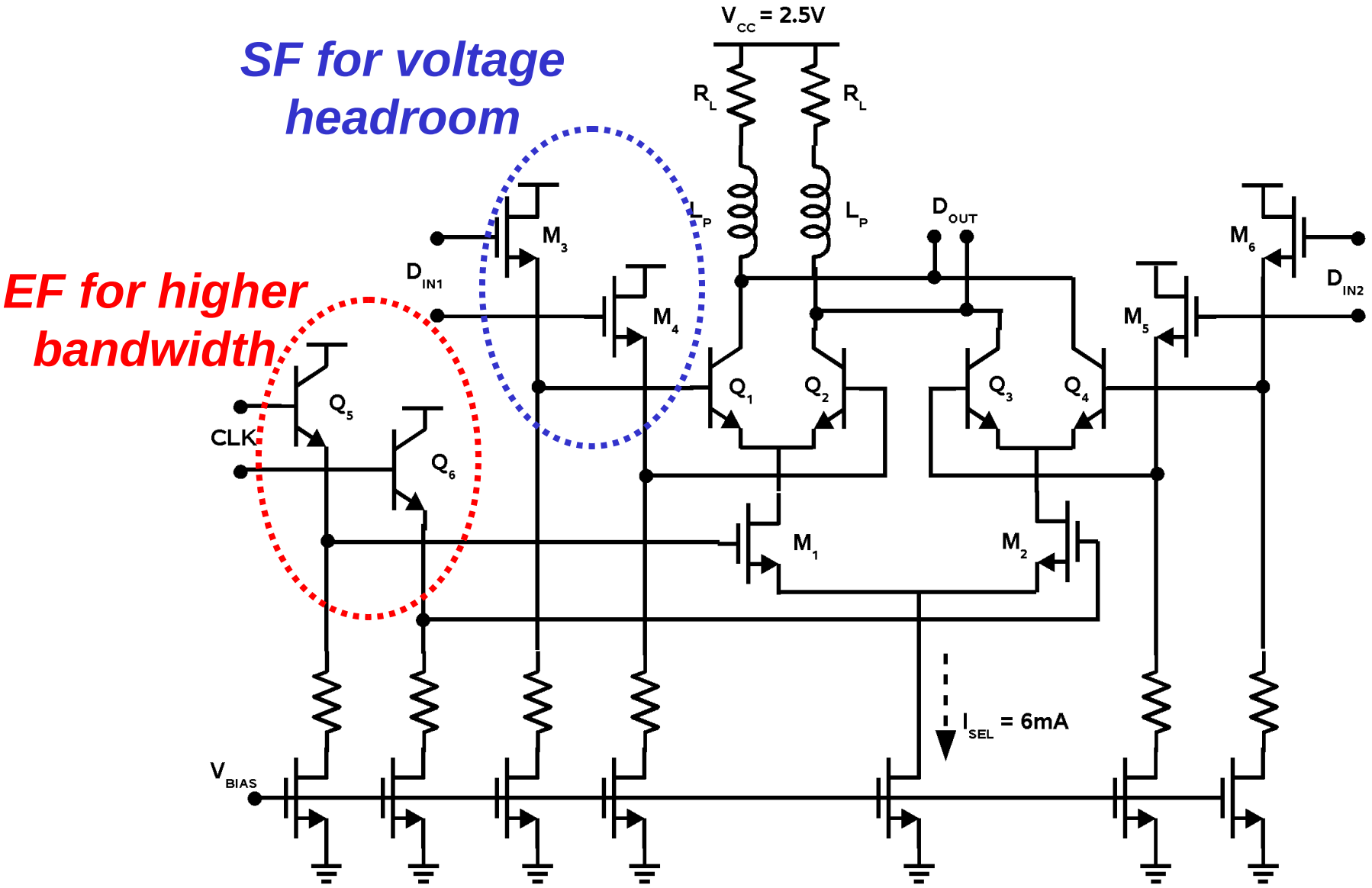
65-nm GP/LP CMOS vs. SiGe HBT and BiCMOS dividers



2.5-V, 1.4-W, 90-Gb/sTransmitter

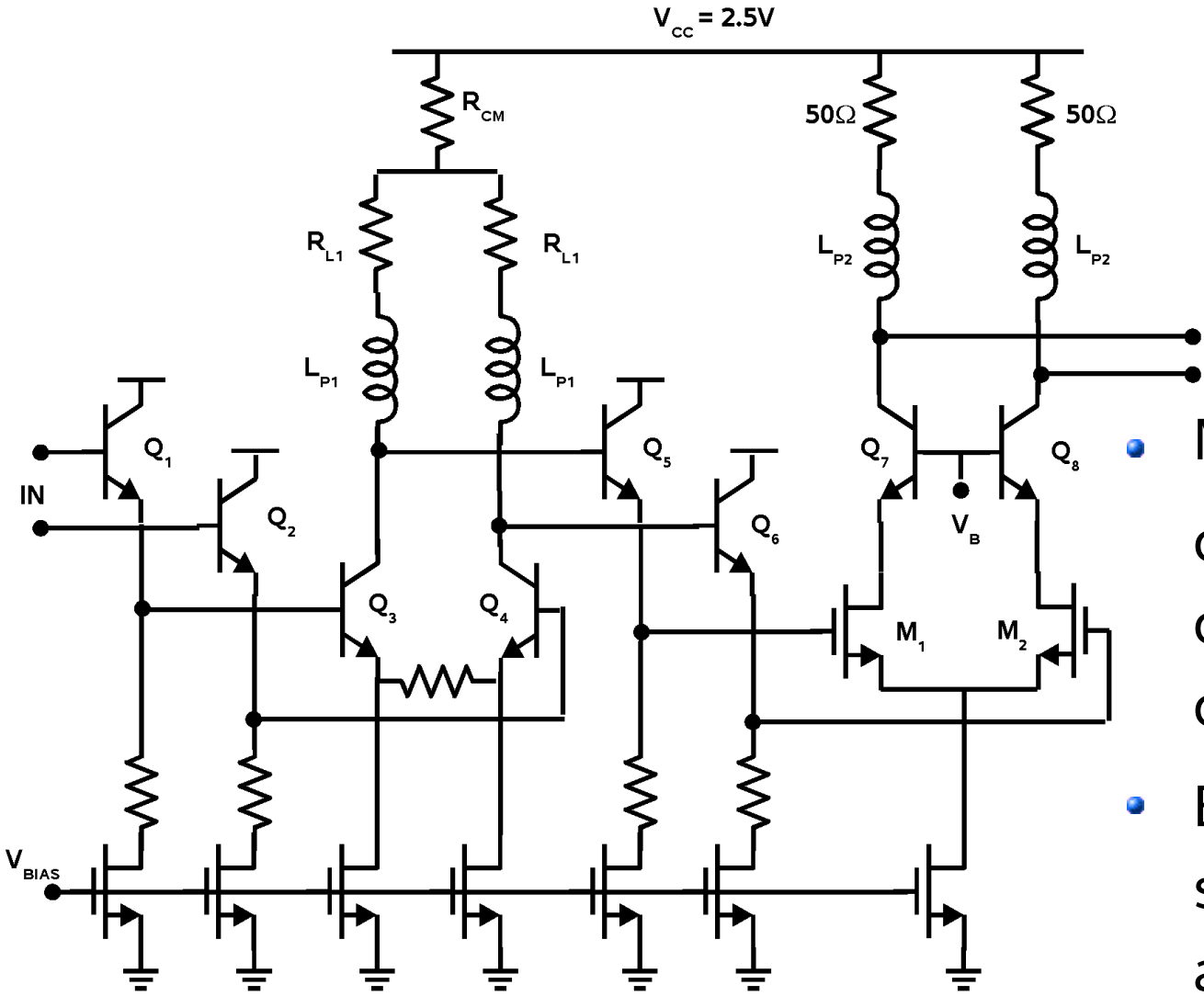


2.5-V, 90-Gb/s BiCMOS Selector



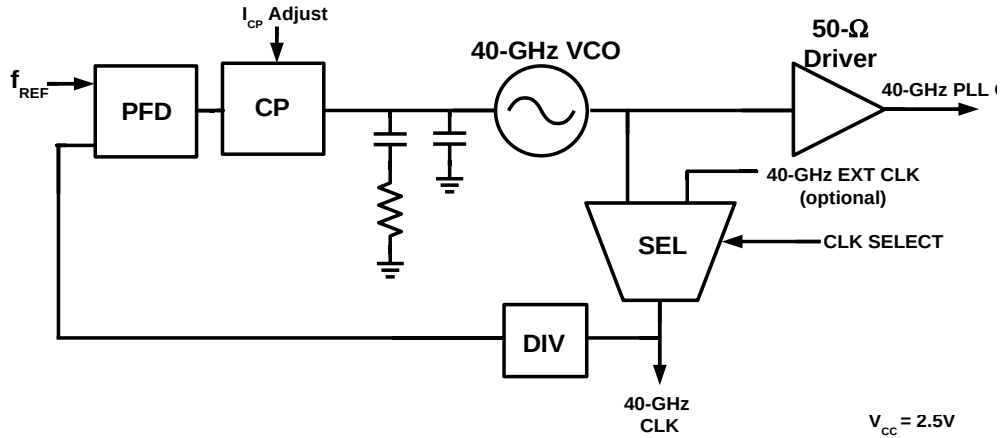
90-Gb/s selector consumes 60mW

2.5-V, 90-Gb/s BiCMOS Output Driver

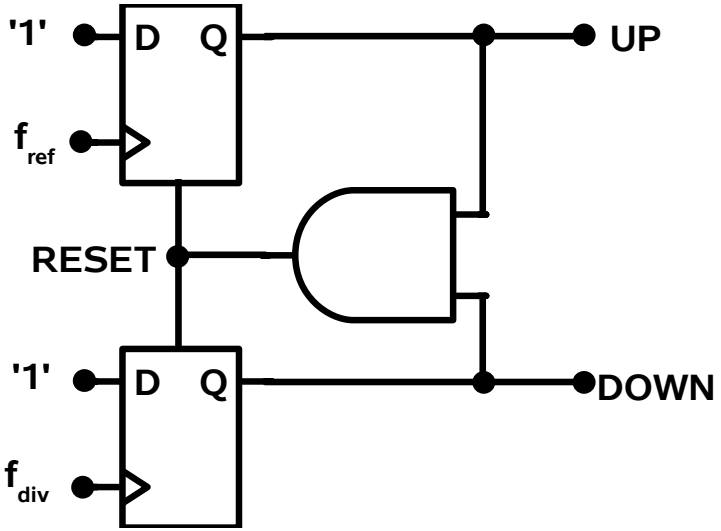


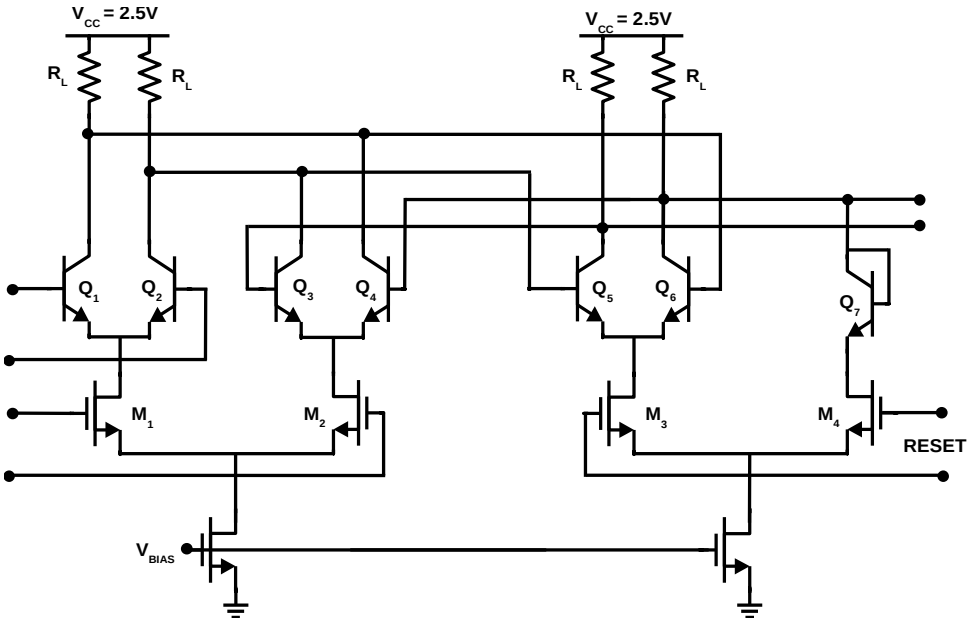
- MOS g_m and input capacitance relatively constant as bias current changes.
- Excellent for output stages with adjustable amplitude control.

2.5V, 40-GHz PLL with Resettable BiCMOS latch

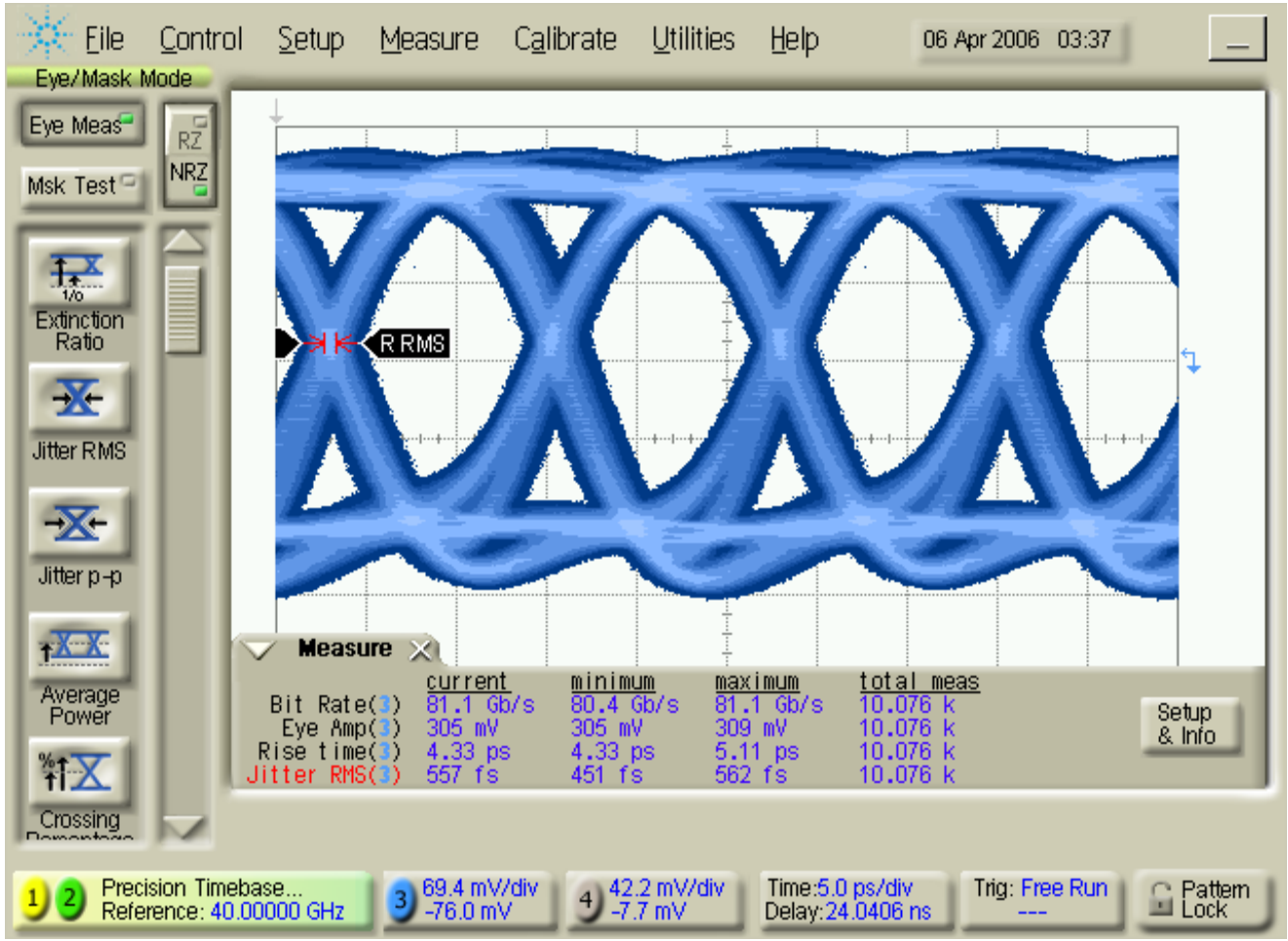


- 38-42 GHz lock range



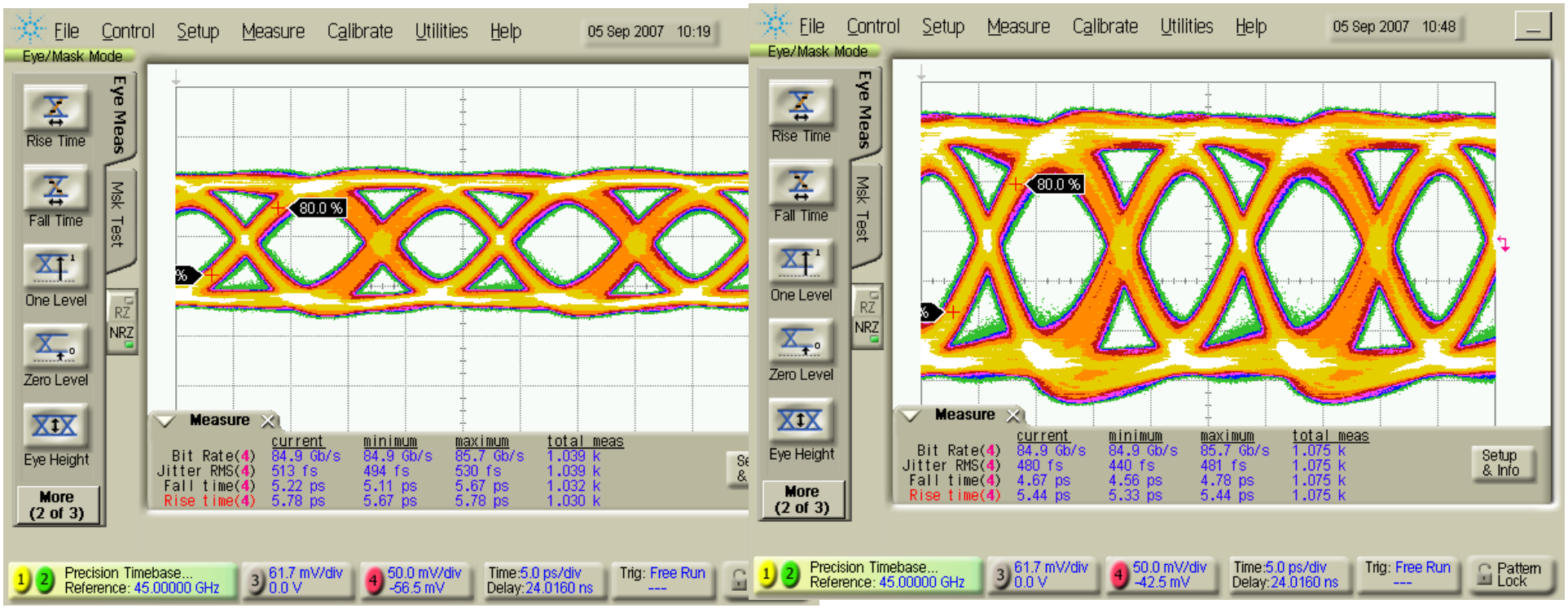


Measured Results: 80 Gb/s



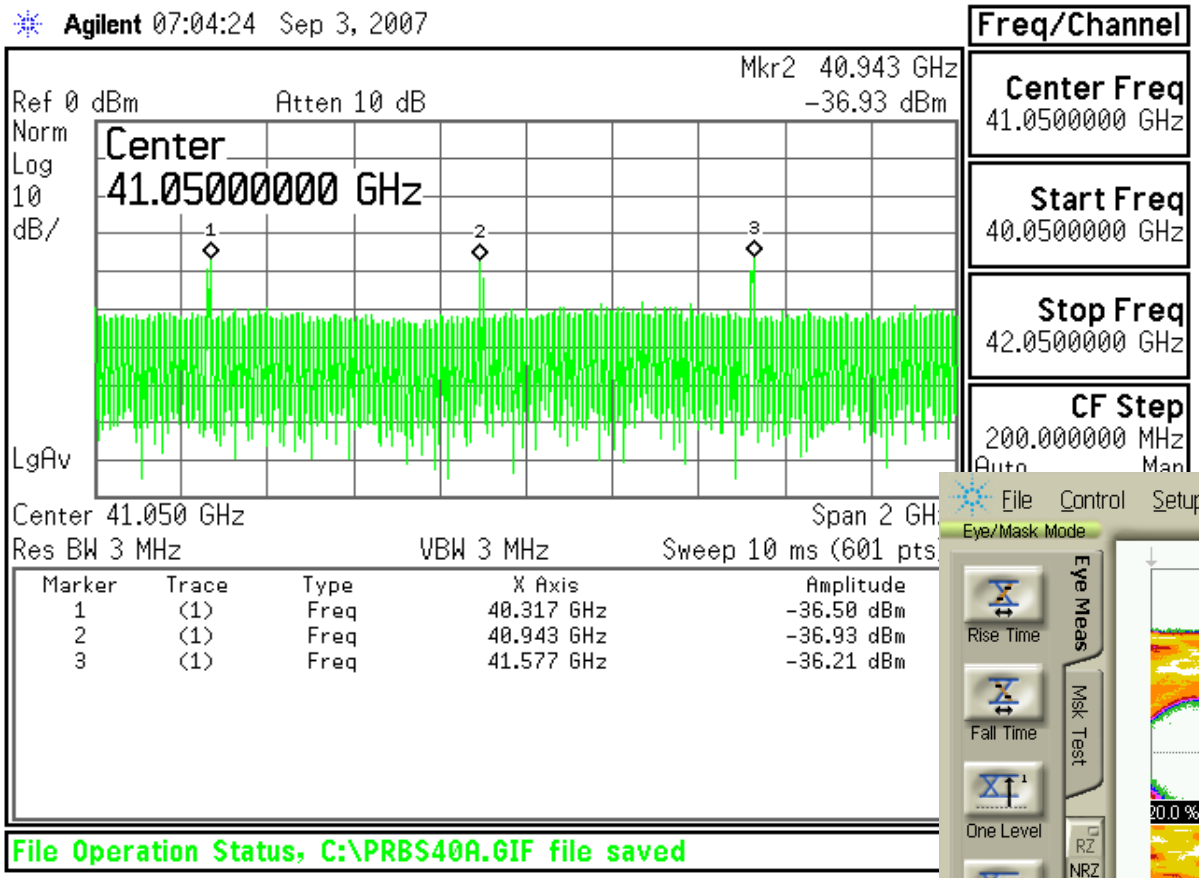
- Running for more than 1 hour continuously in the lab.
- Jitter: 560 fs (rms) , Rise/fall time: 4-5 ps, Amplitude: 300 mV_{pp} per side

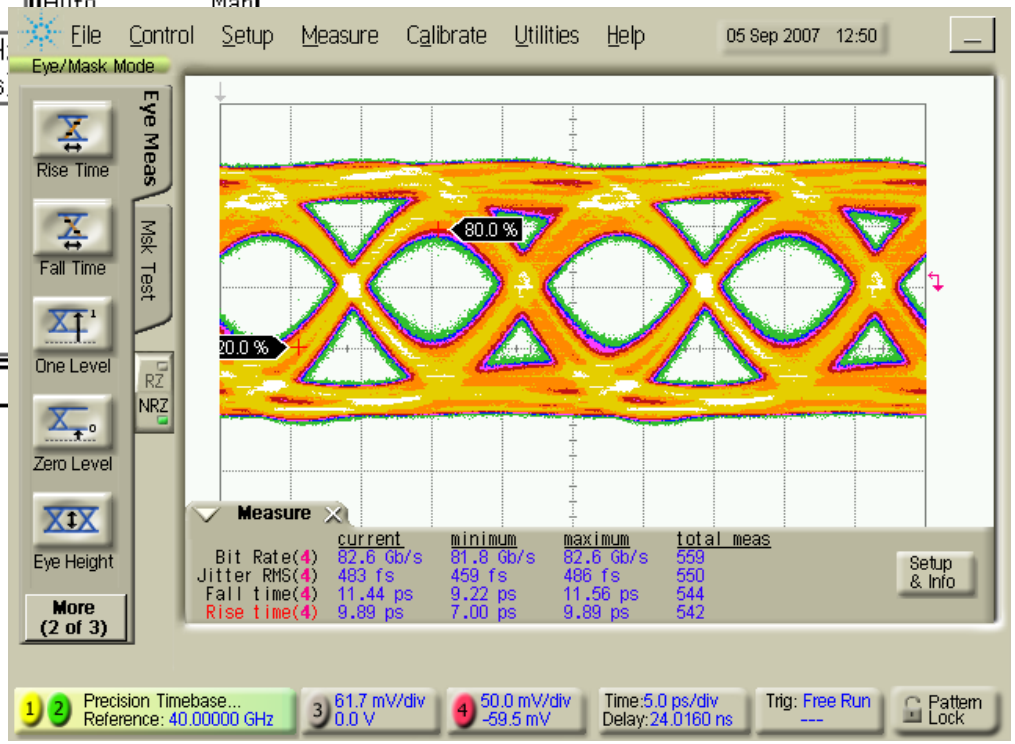
90 Gb/s: amplitude control



Little degradation in eye quality as amplitude varies from 150 mV to 300 mV per side

80 Gb/s at 100 °C





Summary

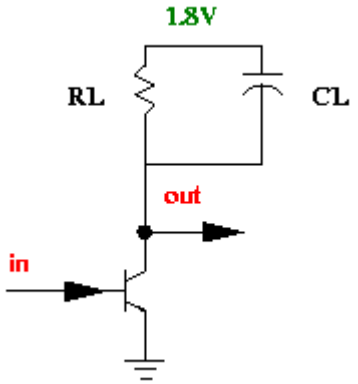
- Minimum delay of MOS/BiCMOS CML gates occurs at 0.3mA/μm
- Minimum MOS-CML voltage swing and delay decreases with every new node: $600mV_{pp}$ in 180nm, $450mV_{pp}$ in 130-nm, $350mV_{pp}$ in 90-nm and 65-nm CMOS
- In the 0.15 - 0.4mA/μm range, CML delay is robust V_T, I_{DS}, and V_{GS} variation.
- Algorithmic design methodology for MOS, HBT and BiCMOS CML gates

Back-up slides

Device model parameters

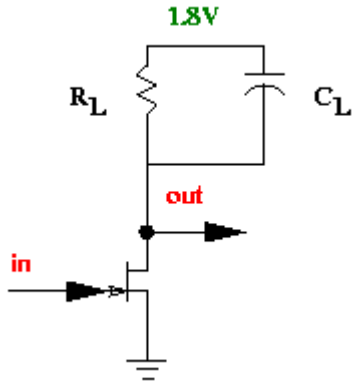
Device Parameter	90nm CMOS	130nm SiGe HBT	GaAs p-HEMT	InP HEMT
gm/μm	1.2 mS	38*IC	0.5 mS	0.65 mS
Cgd(Cbc)/μm	0.4 fF	2.5 fF	75 aF	175 aF
Cgs(Cbe)/μm	1 fF	3fF + 0.3p*gm	750 aF	584 aF
Cdb(Ccs)/μm	1.5fF	1.1 fF	170 aF	220 aF
JpfT (mA/μm)	0.3	2	0.3	0.3
SL (V/ps)	0.16	0.56	0.81	0.56
BVCEO/GDO (V)	1.5	1.6	6	2
VBE/VT (V)	0.3 (0.75)	0.9	-0.9	-0.6
Vsupply (V)	1.2	1.8-3.3	5	3

CE/CS Stage



$$A_V = \frac{-g_m R_L}{1 + s\left[R_{\pi 0}\left(C_\pi + C_\mu\left(1 + g_m R_L\right)\right) + R_L\left(C_\mu + C_{cs} + C_L\right)\right]}$$

$$\tau_1 = R_{\pi 0} C_\pi + R_{\mu 0} C_\mu + R_L\left(C_\mu + C_{cs} + C_L\right)$$



$$R_{\pi 0} = r_\pi \| R_b \qquad R_{\mu 0} = R_{\pi 0}\left(1 + g_m R_L\right) + R_L$$

$$\frac{1}{\tau_2} = \frac{1}{R_{\pi 0} C_\pi} + \frac{1}{R_L C_\pi} + \frac{1}{R_L C_\mu} + \frac{1}{R_L C_{cs}} + \frac{1}{R_L C_L} + \frac{g_m}{C_\pi}$$

CE/CS stage: input impedance

$$Z_{input} \approx R_b + \frac{1}{[C_\pi + (1 + g_m R_L) C_\mu] s}$$

$$Z_{input} = R_b + \frac{1}{sC_\pi} \| \frac{1 + R_L (C_\mu + C_{cs} + C_L) s}{sC_\mu (1 + g_m R_L + R_L s C_{cs})}$$

$$\tau_{delay} = \frac{\ln(2)}{\omega_{3dB}} = \frac{0.69}{6.28 \times 20\text{GHz}} = 5.5\text{ps}$$

CE/CS stage: numerical example

$$A_V = -g_m R_L = \frac{-I_C R_L}{V_T} \qquad R_b = 0;\ R_L \times 2I_C = \Delta V = 250\,mV;\ A_V = -5$$

$$\tau_1 = R_L(C_\mu + C_{cs} + C_L) = \Delta V \frac{(C'_\mu + C'_{cs})A_E}{I_T} + \Delta V \frac{C_L}{I_T}$$

$$\tau_1 = \Delta V \left(\frac{C'_\mu + C'_{cs}}{\frac{I_T}{I_{CpT}} \downarrow_{CpfT}} + \frac{C_L}{I_T} \right) = \Delta V \left(\frac{1}{SL_I} + \frac{C_L}{I_T} \right) \qquad \tau_1(ps) = 0.25\left(2 + \frac{C_L(fF)}{I_T(mA)}\right)$$

- It takes 1 mA of tail current for each 2 fF of load capacitance to maintain 50% of intrinsic slew rate!
- The base resistance term cannot be neglected in HBT implementations.
- The gate resistance term can be minimized in MOSFET inverters by reducing finger width W_f

130nm CMOS example (R_g=0)

$$A_V = -R_L g_m = -2 ; g_m = \frac{I_T}{V_{eff}};$$

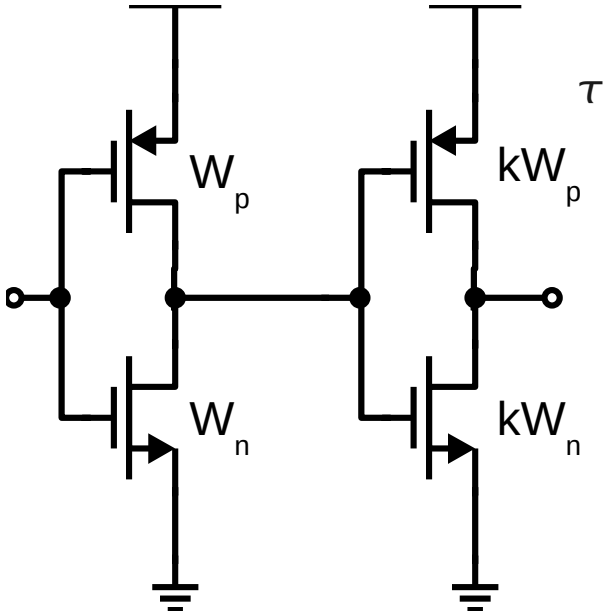
V_{eff} = 0.3V; ΔV = 0.6 V; A_V = -2; C_{int} = 0; k = 2, C'_{gd} = 0.5fF/μm, C'_{db} = 1.7 fF/μm

$$SL_I = \frac{0.3 mA/um}{0.5 fF/um + 1.7 fF/um} = 0.136 V/ps$$

$$\tau_1(ps) = \Delta V(7.35 + 9.166 \times k) + \Delta V \frac{C_{int}}{I_T} = 4.41ps + 2 \times 5.5ps = 15.4ps$$

What happens if FET is biased beyond peak f_T in the linear I_D-V_{GS} region?

CMOS inverter chain delay ($V_{An}=V_{Ap}$, $W_p = 2W_n$)



$$\tau_1 = (r_{on} \| r_{op})[C_{gd}(p) + C_{db}(p) + C_{gd}(n) + C_{db}(n)] = \frac{3}{2} r_o (C_{gd} + C_{db})$$

$$\tau_2 = \left(\frac{r_o}{2} + \frac{R_g}{2k}\right)[3k\, C_{gs} + (1 + g_m r_o) 3k\, C_{gd}]$$

$$\tau_2 = \frac{3}{2} r_o \left(k + \frac{R_g}{r_o}\right)[C_{gs} + (1 + g_m r_o) C_{gd}]$$

$$\tau = \frac{3}{2} r_o (C_{gd} + C_{db}) + \frac{3}{2} r_o \left(1 + \frac{R_g}{k r_o}\right)[C_{gs} + (1 + g_m r_o) C_{gd}]$$

- Delay expression is similar to MOS-CML delay if $R_L = r_o$ and $A_V = -g_m r_o$
- In real implementations, for the same g_m, $R_L << r_o$ and CMOS inverter $|A_V| = 6 .. 10 > 2$
- MOS-CML delay >3 times smaller than CMOS delay

Bipolar and MOS cascode stages

$$A_V \approx \frac{-g_{m1} R_L}{1 + s\left[R_b (C_{\pi 1} + 2\,C_{\mu 1}) + R_L (C_{\mu 2} + C_{cs2} + C_L)\right]} \qquad Z_{input} = R_b + \frac{1}{\left[C_\pi + 2\,C_\mu\right] s}$$

$$\tau_1 = R_b (C_{\pi 1} + 2\,C_{\mu 1}) + R_L (C_{\mu 2} + C_{cs2} + C_L) \qquad \tau_2 \approx \frac{C_{\pi 2} + C_{cs1} + 2C_{\mu 1}}{g_{m2}} \approx \frac{1}{\omega_{T2}}$$

$$A_V = \frac{-g_{m1} R_L}{1 + s\left[R_g (C_{gs} + 2\,C_{gd}) + R_L (C_{gd} + C_{db} + C_L)\right]}$$

$$\tau_2 \approx \frac{C_{gs2} + C_{bd1} + C_{sb2} + 2C_{gd1}}{g_{m2}} > \frac{2}{\omega_{T2}}$$

Cascading bipolar cascode inverters

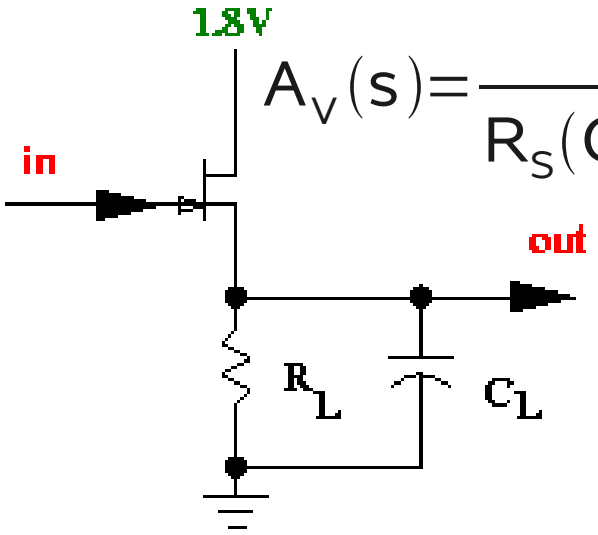
$$\tau_1 = \Delta V \frac{C_\mu + C_{cs} + C_w}{I_T} + \left(k + \frac{R_b}{R_L}\right) \Delta V \frac{C_\pi + (1 - A_V) C_\mu}{I_T} \approx \frac{\Delta V}{SL_I} + \frac{\Delta V}{2 V_T} \frac{k + \frac{tech}{\Delta V}}{\omega_T}$$

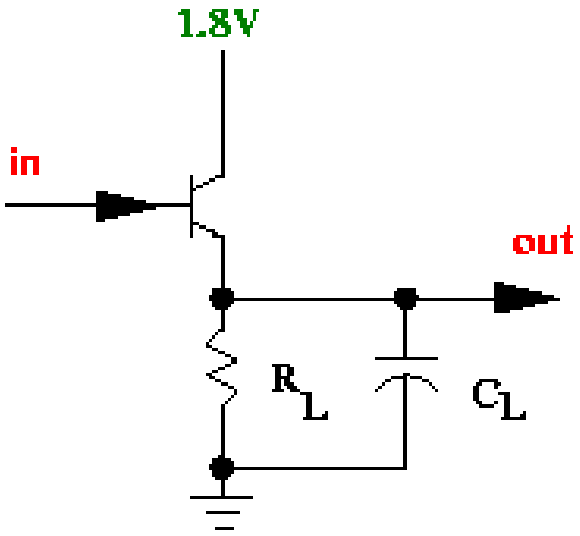
$$A_V = -1; \quad \Delta V = I_T R_L; \quad g_m = \frac{I_T}{2 V_T}$$

Cannot be reduced by optimizing layout!

$$R_b = (100..300)\,\Omega\mu m \times I_E(\mu m); \quad \frac{R_b}{R_L} = \frac{R_{bI} w_E J_{CpfT}}{\Delta V} = \frac{0.12...0.36V}{\Delta V}$$

EF/SF stage with capacitive load





$$A_V(s)=\frac{g_m+sC_\pi}{R_S(C_\pi C_L+C_\pi C_\mu+C_\mu C_L)s^2+(g_m R_S C_\mu+C_L+C_\pi)s+g_m}$$

$$\tau_1 \approx R_S C_\mu+\frac{C_\pi+C_L}{g_m}$$

- Two poles -> potentially unstable -> ringing
- R_S includes R_b
- If C_L is small, bandwidth is limited by f_T.
- Slows down with C_L (loading ...) or by reducing f_T (bias current density)

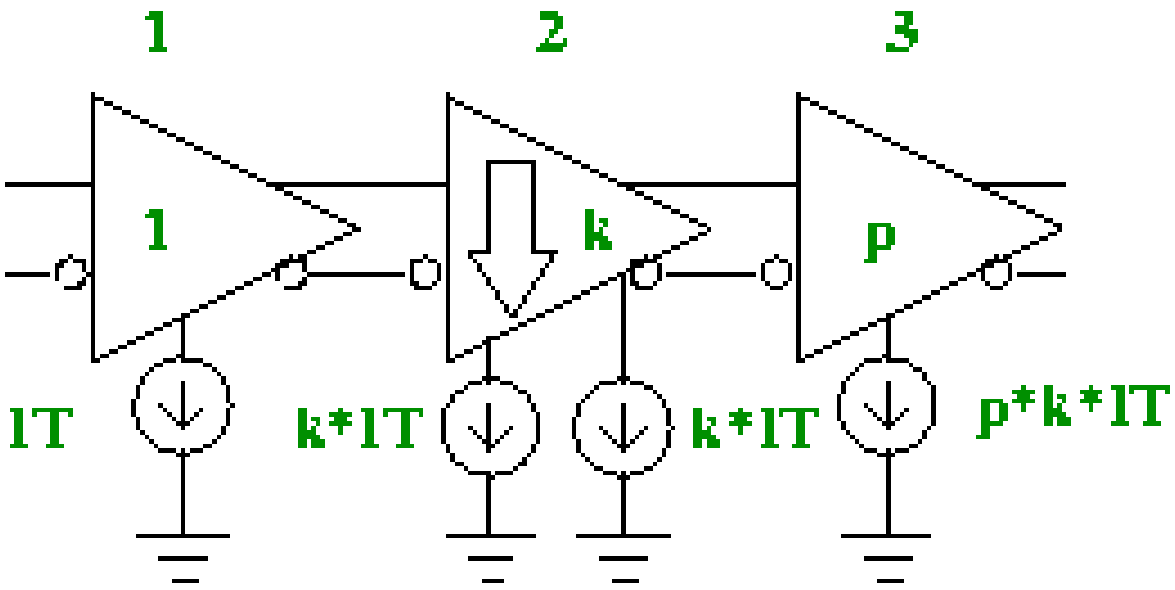
EF/SF stage: input/output impedance

$$Z_{input} = R_b + Z_\mu \,\text{II}\left[Z_\pi + (1 + g_m Z_\pi) Z_L\right]$$

$$Z_{input} = R_b + \frac{1}{j\omega C_\mu} \,\text{II}\left[\frac{1}{j\omega C_\pi} + \frac{1}{j\omega C_L} - \frac{g_m}{C_\pi C_L \omega^2}\right]$$ Negative resistance

$$Z_{out} \approx \frac{R_S C_\pi s + 1}{g_m + C_\pi s}$$ looks inductive up to f_T ...

Cascading ECL stages (R_b=0, from EF τ_p)

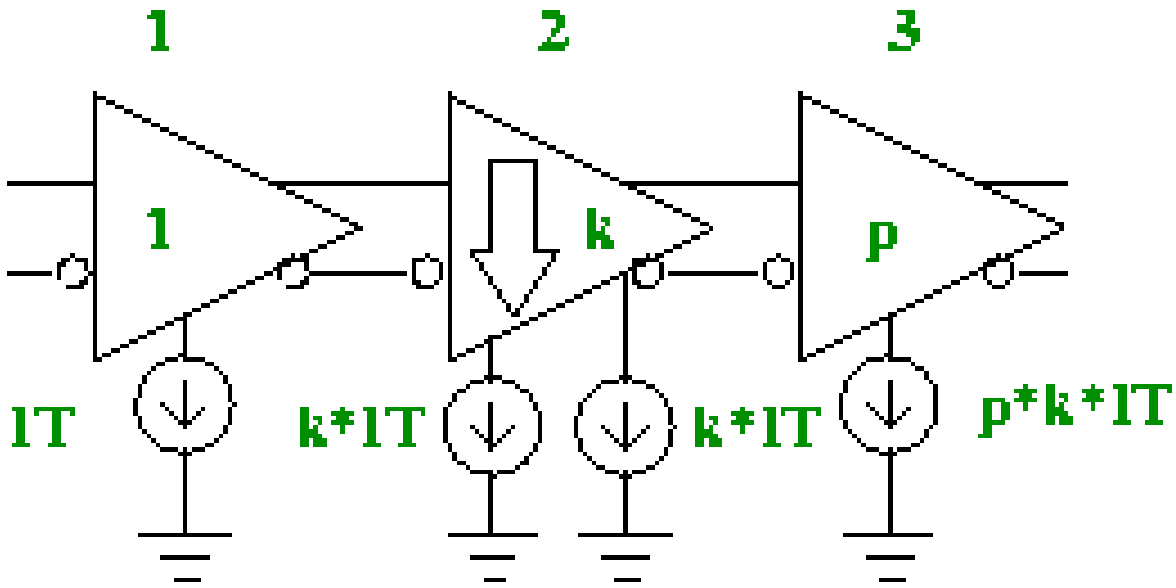


$$Z_{L1} \approx \frac{1}{skC_\mu} \Big\| \left[\frac{1}{skC_\pi} + \frac{1}{sC_{L2}} \right] \qquad Z_{L2} = \frac{1}{[pkC_\pi + pk(1+g_m R_L)C_\mu]s}$$

$$\tau_{p1} \approx R_L(C_{cs} + C_\mu + kC_\mu) + \frac{(p+1)C_\pi + p(1+g_m R_L)C_\mu}{g_m}$$

$$\tau_{p1} \approx \frac{\Delta V}{SL_I} + \frac{p+1}{\omega_T} + \Delta V \frac{(p+k-1)C_\mu}{I_T} = 1.5p + 0.5k + 1ps$$

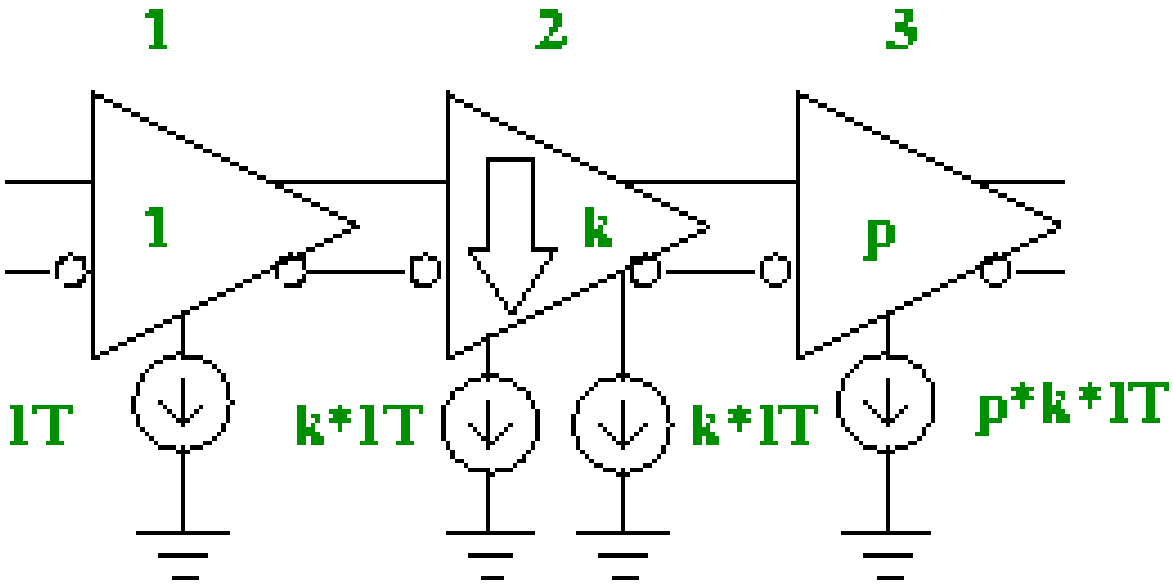
Cascading SCFL stages: from SF τ_p



$$\tau_{p1} \approx R_L\left(C_{db}+C_{gd}+k\,C_{gd}\right)+\frac{(p+1)C_{gs}+C_{sb}+p\left(1+g_m R_L\right)C_{gd}}{g_m}$$

$$\tau_{p1} \approx \frac{\Delta V}{SL_I}+\frac{p+1}{\omega_T}+\Delta V\,\frac{(p+k-1)C_{gd}+C_{sb}}{I_T} \approx 4\,ps+2p+0.375k\,(GaAs\,pHEMT)$$

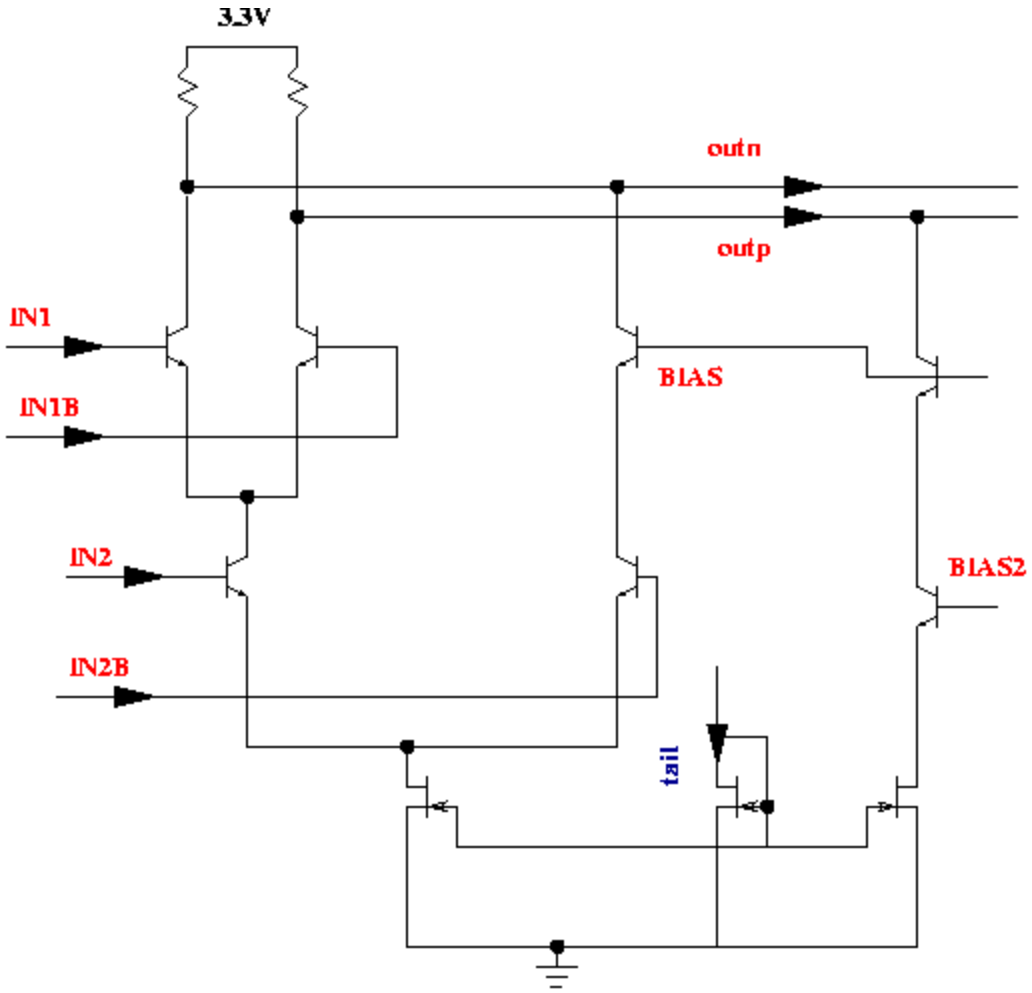
Cascading SCFL Stages



$$\tau_1 = \Delta V \frac{C_{gd} + C_{db} + C_{int}}{I_T} + k\,\Delta V \frac{C_{gd} + \frac{C_{int}}{k} + C_{gs} \,\mathrm{II}\left[C_{sb} + p\left(C_{gs} + (1 + A_V) C_{gd}\right)\right]}{I_T} + \tau_{SF}$$

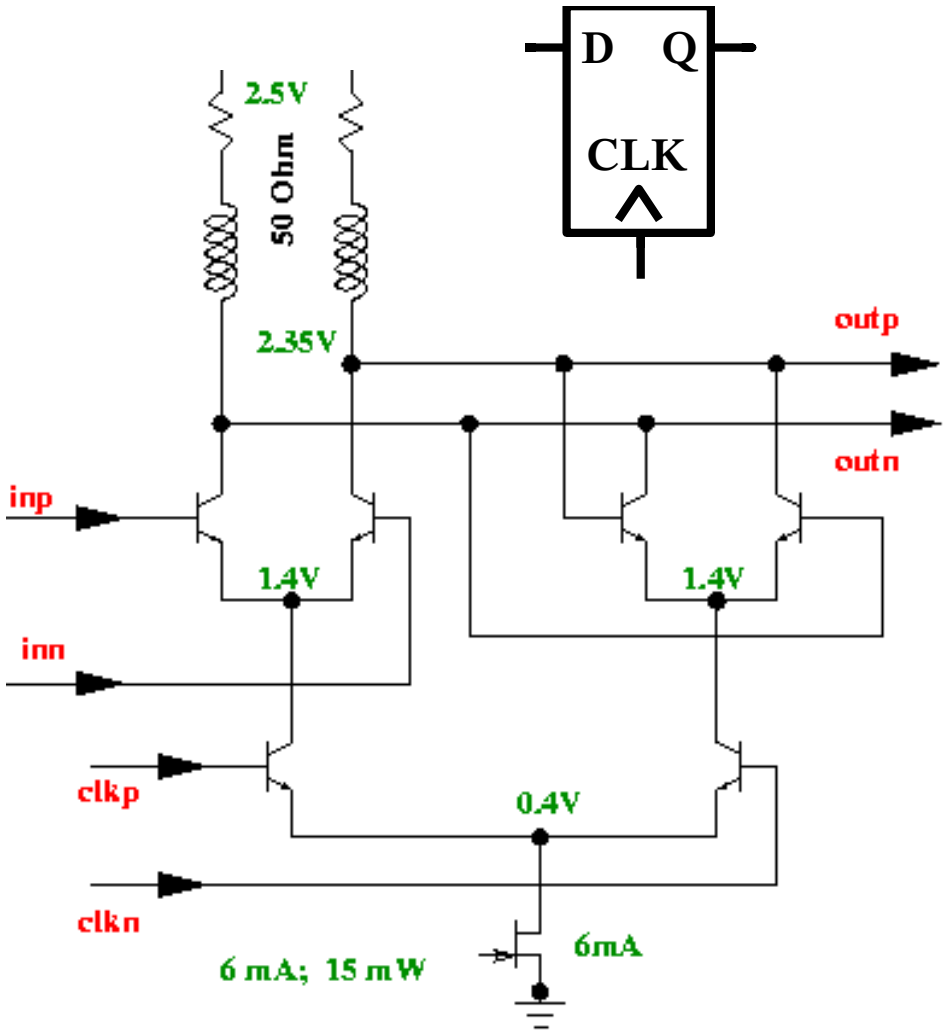
$$\frac{\Delta V}{SL_I} + \frac{\Delta V}{V_{eff}} \frac{1.1k}{\omega_T} > \tau_1 > \frac{\Delta V}{SL_I} + \frac{\Delta V}{V_{eff}} \frac{(0.66 \ldots 0.8)k}{\omega_T}$$

AND - unbalanced: BiCMOS CML



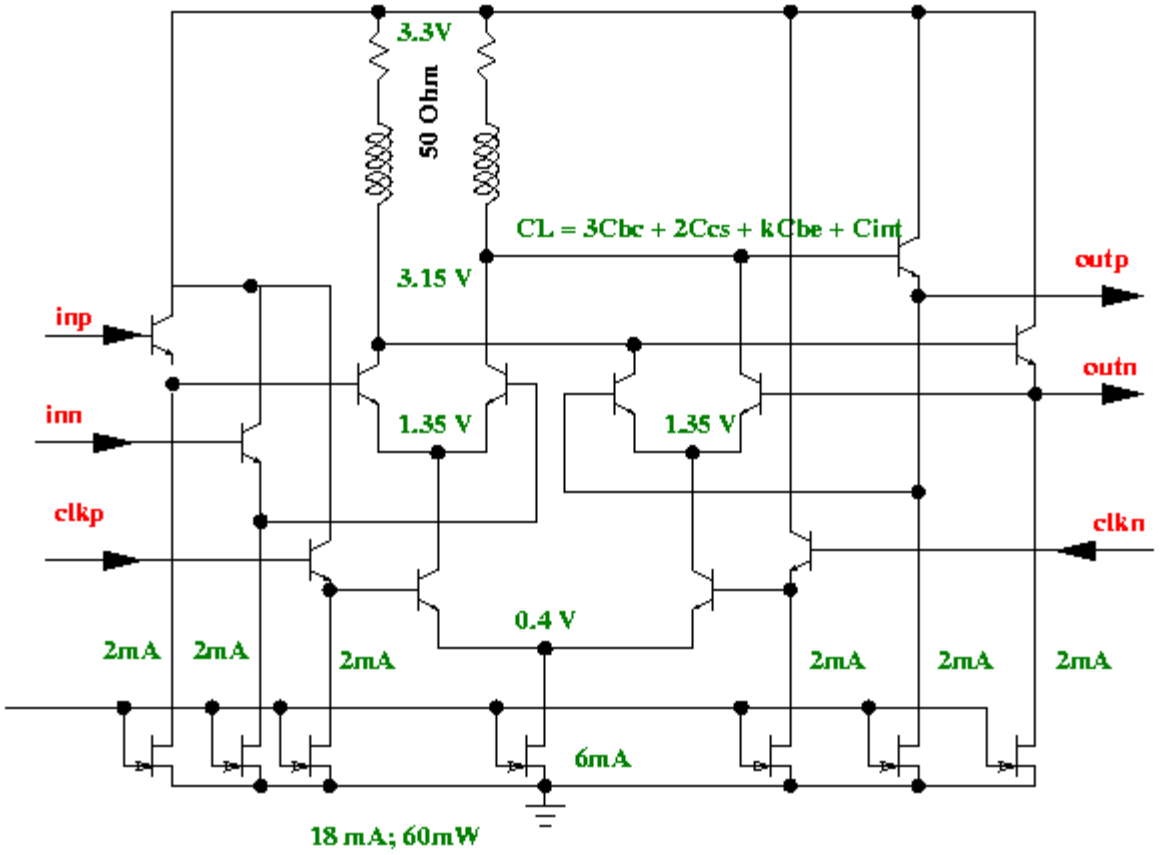
- n-MOS current tails for voltage headroom
- Cascode for good isolation and symmetry + extra tail

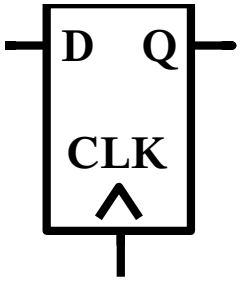
D-Latch: Bipolar CML (slow)



- n-MOS current tails for voltage headroom
- Inductive peaking
- No EF in latch

D-Latch: Bipolar ECL (fast: 60 GHz)



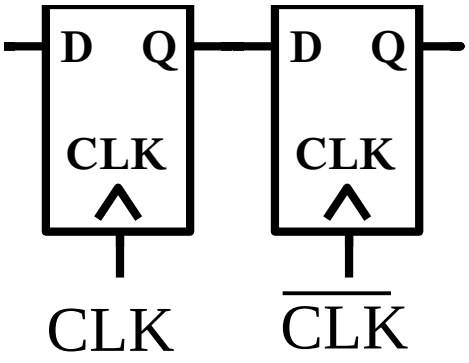


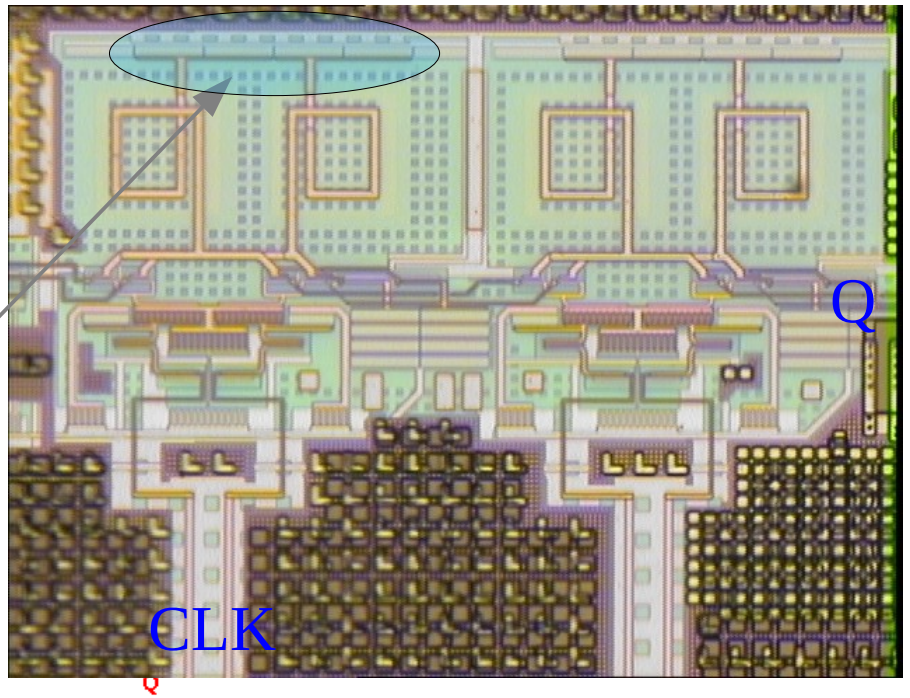
n-MOS current tails for voltage headroom

Inductive peaking

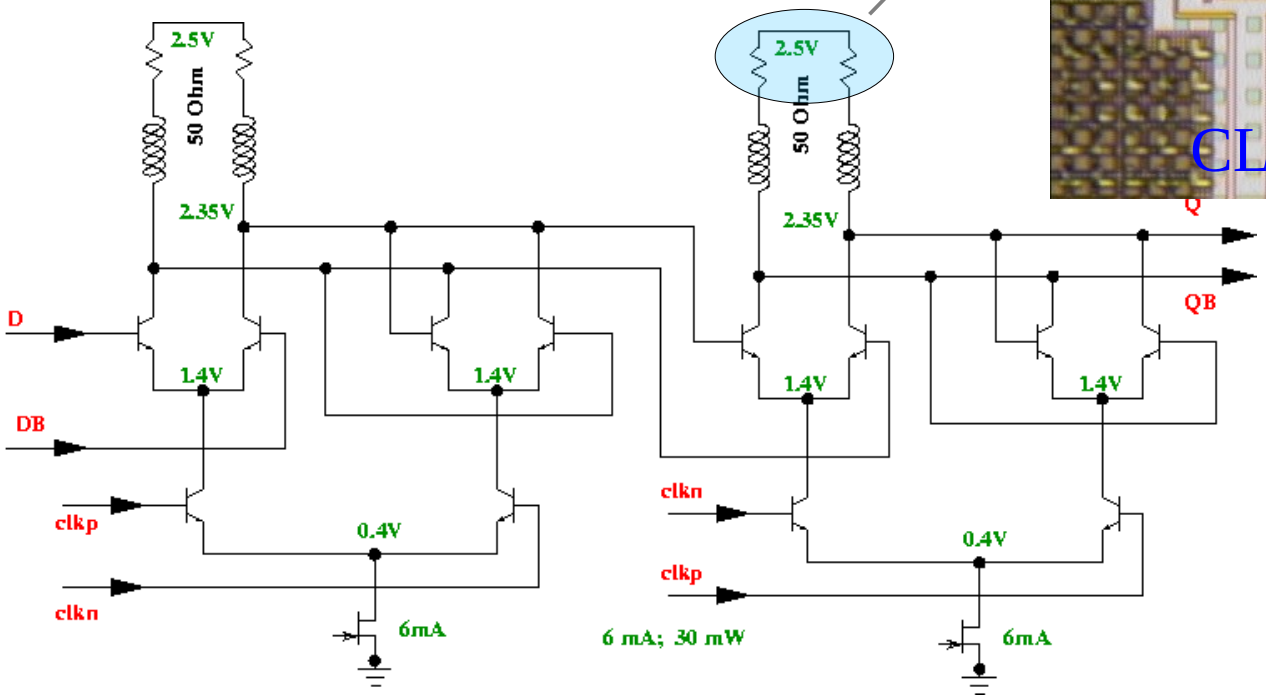
Fast - EF in latch

D-Flip-Flop: bipolar CML

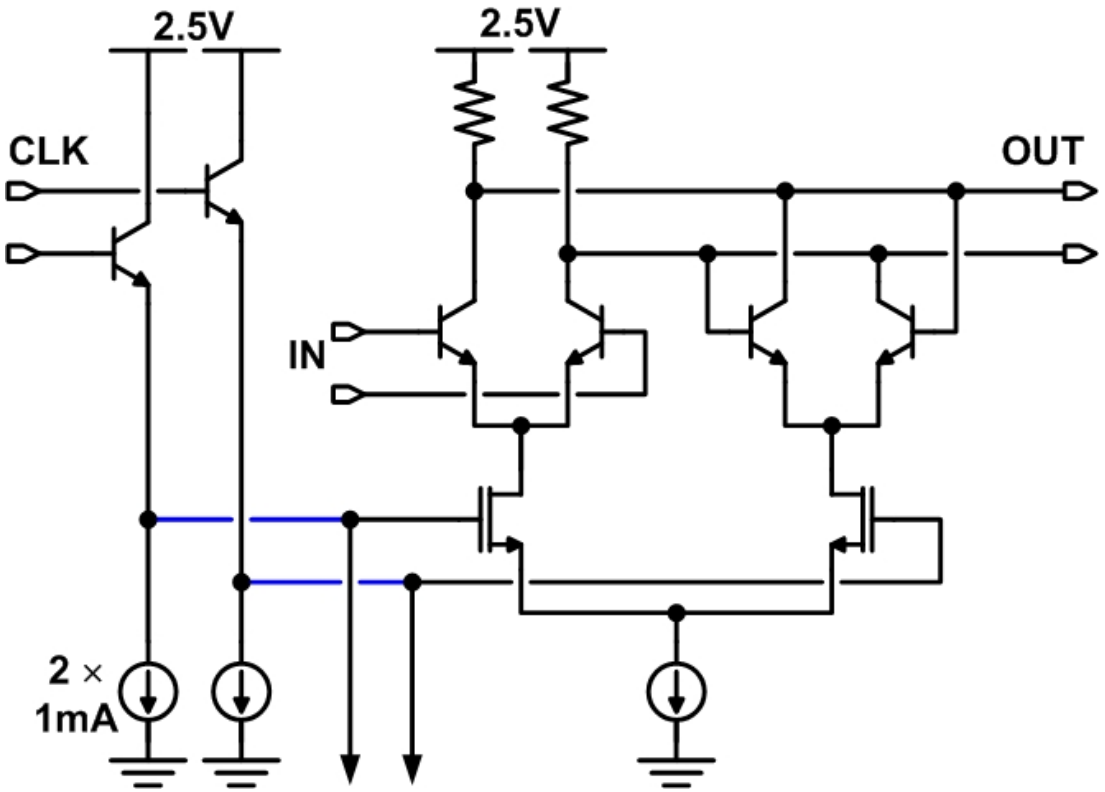


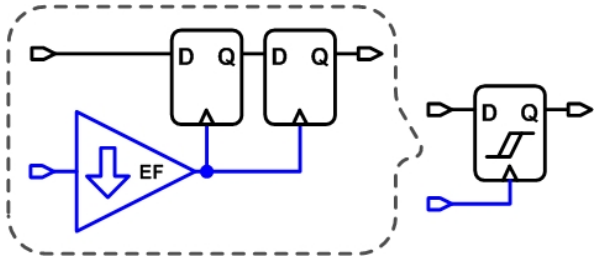


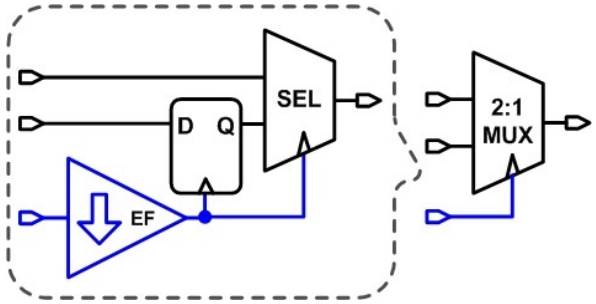
CLK



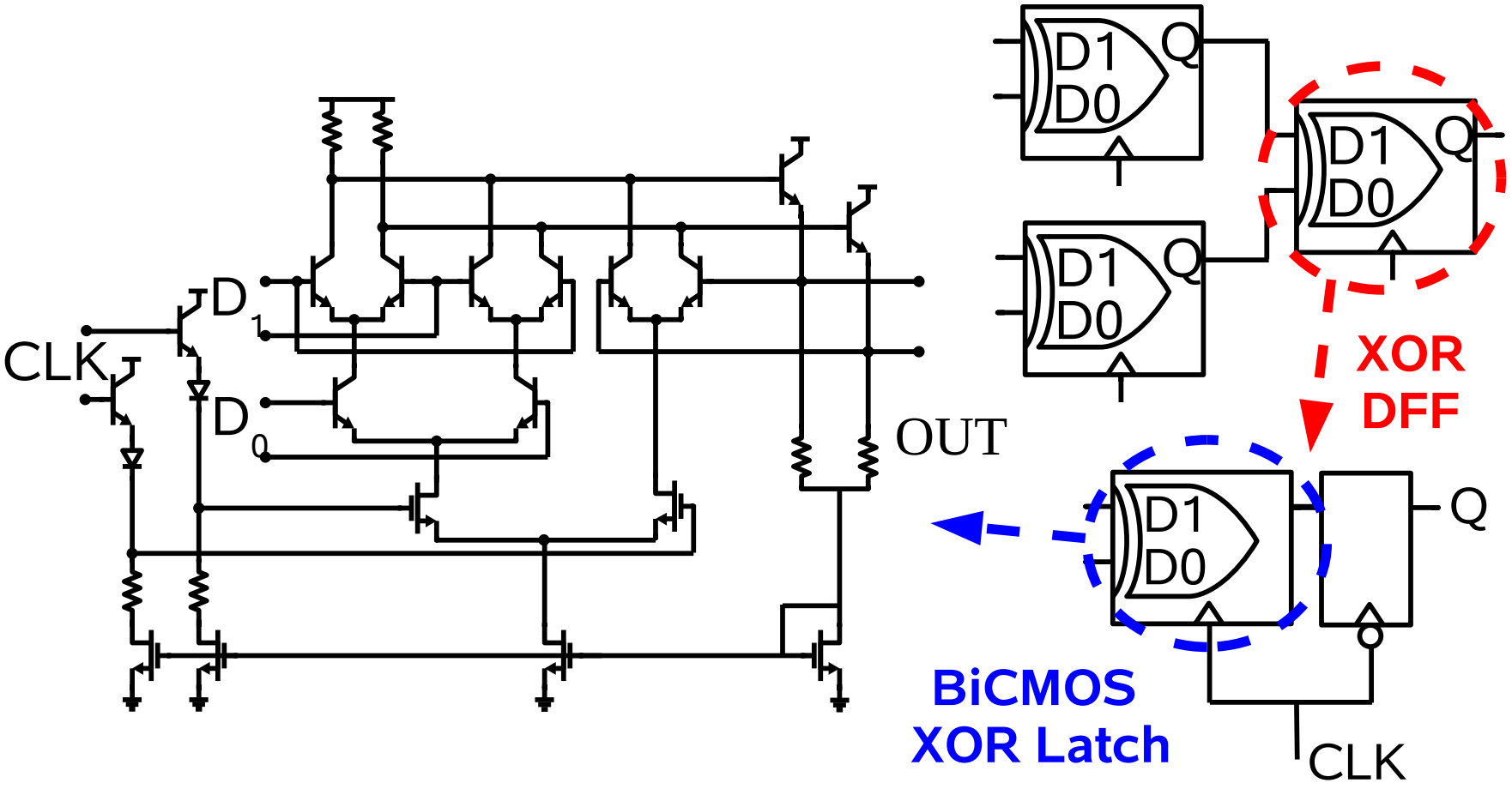
D-Latch: BiCMOS CML (12 GHz)
(E. Laskin CSICS 2005)







BiCMOS XOR Latch

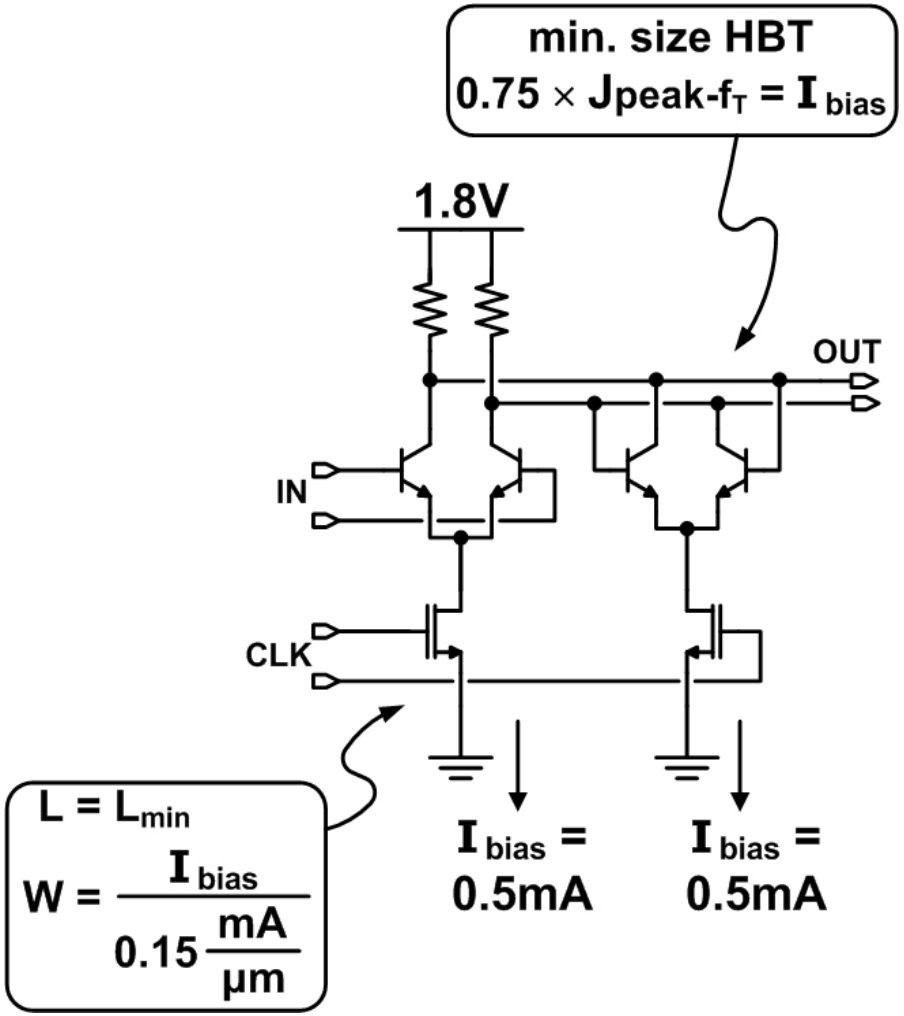


Further Power Reduction

- Same technology
- Removed current source
- V_{DD} = 1.8 V, I_{total} = 1 mA
- Power reduced:

  2.5 mW → 1.8 mW
- Same speed: 12 GHz
- Simulated with

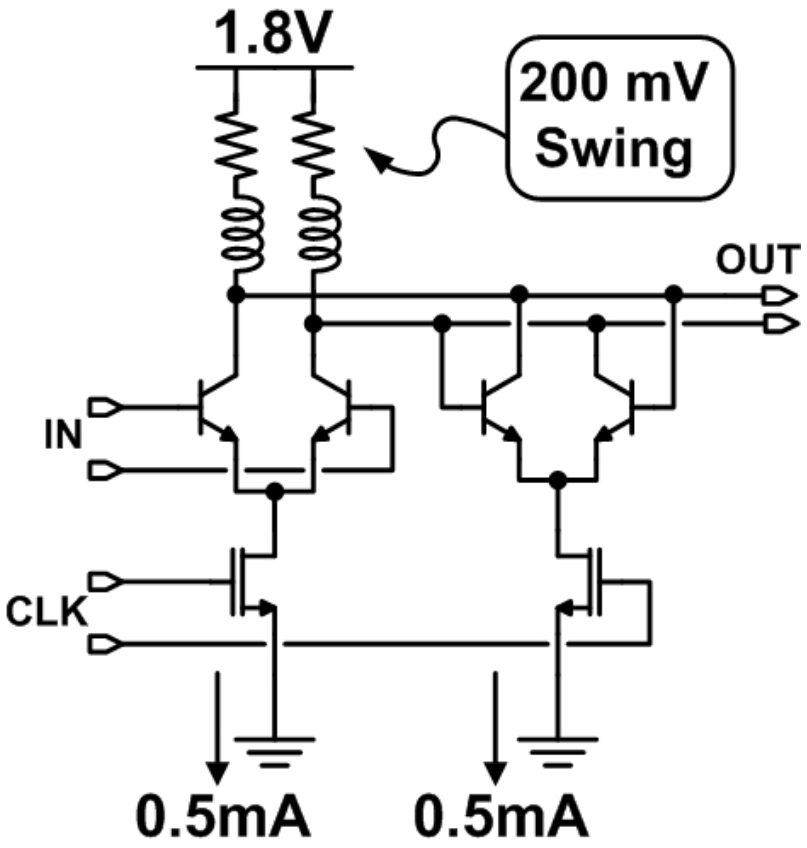
  extracted layout parasitics



V. Kozlov et al, IEEE CSICS 2012

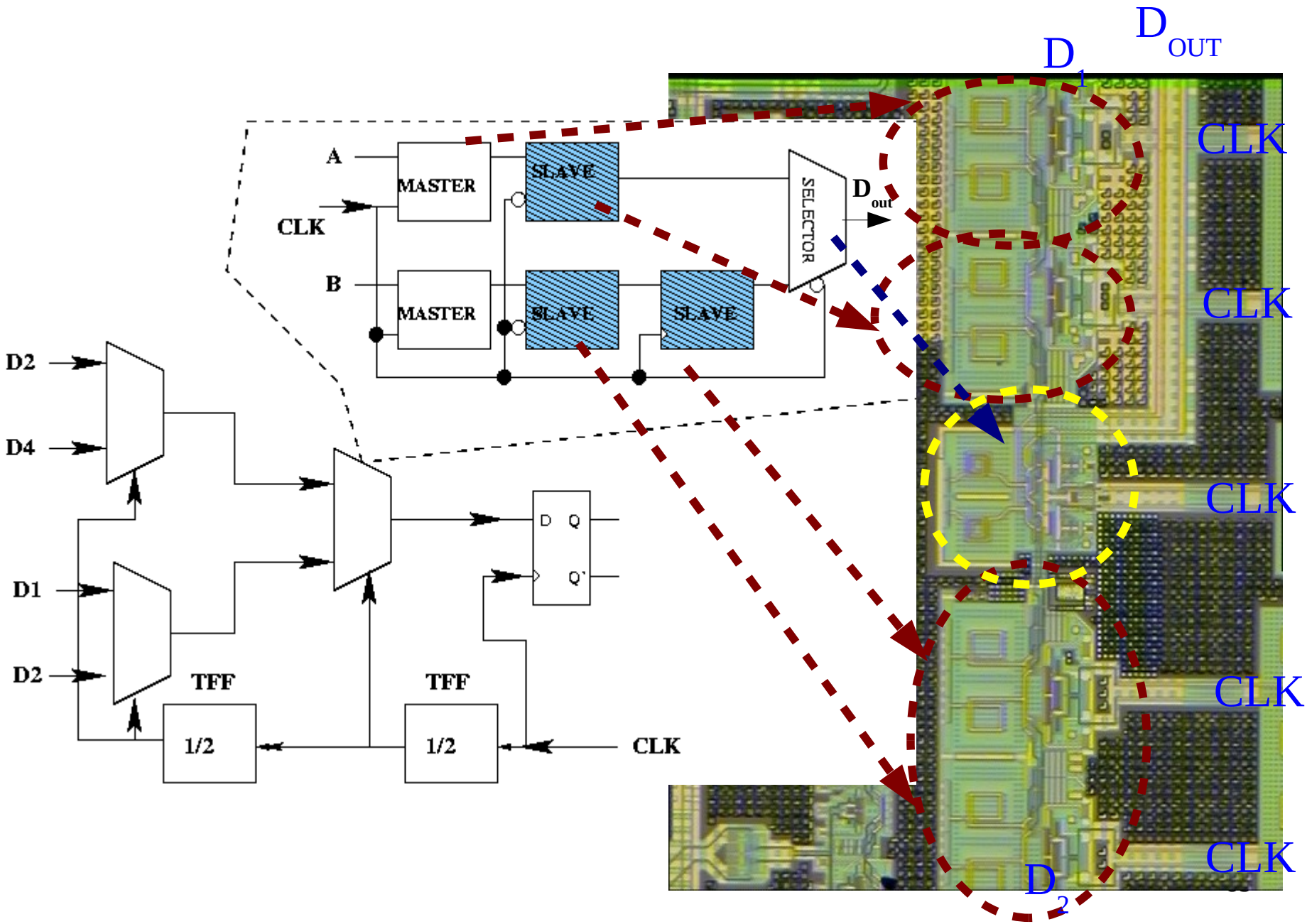
Scaling to Next Tech. Node

- 90 nm SiGe BiCMOS [3]
- HBT f_T: 160 → 230 GHz
- MOS f_T: 80 → 120 GHz
- Same power: 1.8 mW
- f_T improvement: x1.42
- Inductive peaking: x1.5
- Δ V reduced: x1.3



- Speed increased : 12 GHz → 30 GHz
- Simulated with extracted layout parasitics

4:1 MUX


A
CLK
B
MASTER
MASTER
SLAVE
SLAVE
SLAVE
SELECTOR
D out
D2
D4
D1
D2
TFF
TFF
1/2
1/2
D Q
Q'
CLK
D OUT
D 1
D 2
CLK
CLK
CLK
CLK
CLK