Problems for Chapter 15 of 'Ultra Low Power Bioelectronics'

Problem 15.1

From the ideal ADC's transfer curve of Figure 15.1 and the assumption that the input statistic that the error between $[-\Delta/2, +\Delta/2]$ is equally likely, show that the rms error of the quantized representation of a real number is $\Delta/\sqrt{12}$. Repeat the exercise with a non-ideal ADC's transfer characteristic in which the transition point doesn't occur halfway between consecutive codes, but is skewed to be 1/3 of the distance between two consecutive codes (the transition points occur at $\Delta/3$, $\Delta+\Delta/3$, $2\Delta+\Delta/3$, …).

Problem 15.2

Consider an ideal 8-bit ADC. Find the signal-to-noise ratio (SNR) in dB of the digitized output signal for the two input signals below:

a) A rail-to-rail sawtooth waveform.
b) A rail-to-rail sinusoidal waveform.

Problem 15.3

An idealized algorithmic ADC shown in Figure 15.2 (b). For this problem, assume that it only has 4 bits of resolution. For simplicity, assume that V_{REF} = 1 V.

a) Find the sequence of voltage values at v_{RES}, and the sequence of the digital output bits for v_{IN} = -0.3 V. What voltage does the output code correspond to?
b) Repeat part a) for v_{IN} = 0.14 V.
c) Construct the ADC's transfer characteristic similar to the one shown in Figure 15.1.

Problem 15.4

Figure P15.4 shows a simplified schematic of the ADC of Figure 15.4 in a 5-bit instantiation. During the sampling phase, the top plates of all the capacitors in the array (V_{comp} node) are connected to V_{ref} through the reference switch, while the bottom plates are connected to v_{IN}. During the hold mode, the bottom plates of all capacitors are grounded, making $V_{comp} = V_{ref} - v_{IN}$. The successive-approximation iterations then proceed as described in Section 15.1 (for 16C, 8C, 4C, 2C, and C in that order). Note that the right-most capacitor, C, is connected to v_{IN} during sampling phase, but will never be connected to V_{ref}. The bit-cycling phase ends after the evaluation of the second-rightmost C. Plot the time sequence of the node voltage, V_{comp}, and the output codes for the following input voltages:

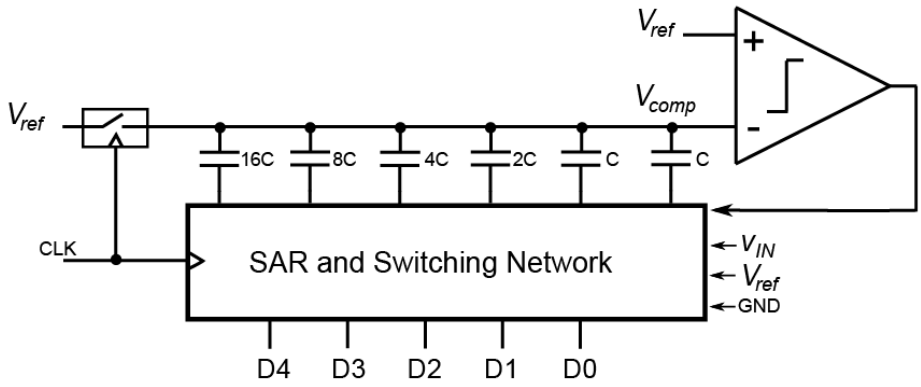

Figure P15.4: A successive-approximation register ADC.

a) $v_{IN} = 0.8V_{ref}$
b) $v_{IN} = 0.1V_{ref}$
c) Repeat the calculation in part a) and b), but assume that there is a parasitic capacitance with a value of 4C from the V_{comp} node to ground. Does this parasitic affect the output codes of the ADC if the comparator is ideal?
d) Comment on how such parasitic capacitance might affect the accuracy of the ADC in a real implementation in which the comparator has non-zero input-referred noise.

Problem 15.5

In this problem, we shall investigate how a ΣΔ ADC utilizes the techniques of oversampling and noise shaping to suppress quantization noise. We will investigate each of the two techniques sequentially.

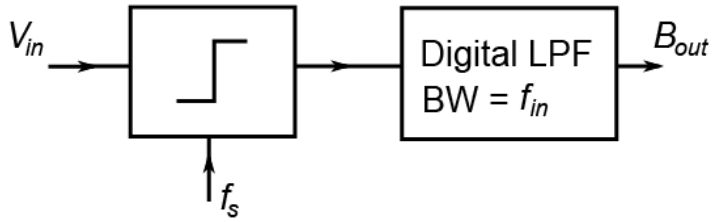

Figure P15.5: A block diagram that illustrates the oversampling technique for quantization-noise reduction.

a) To understand the effect of oversampling alone, consider the simplified oversampling ADC shown in Figure P15.5. The comparator is clocked at a frequency of f_s that is much higher than the input signal's bandwidth f_{in}. Assume that the digital lowpass filter (LPF) has a brick-wall filter (ideal filter with infinitely steep roll-off) with a cutoff frequency of f_{in} and that the input signal is a rail-to-rail sinusoidal waveform. Calculate the SNR at the output of this converter in dB in terms of N, the ADC's resolution, and the the oversampling ratio of the converter, $OSR = f_s / 2 f_{in}$.
b) With the ΣΔ scheme shown in Figure 15.5, derive an expression for the SNR of the converter in terms of N and OSR. Assume that the integrator time

constant is $\tau = 1/\pi f_s$ and that the digital low-pass filter is ideal with an infinitely steep roll-off. How does your answer compare to that obtained in part a)?

Problem 15.6

Suppose you design a 5-bit ADC, using the neuron-inspired ADC's algorithm as described in section 15.2. Sketch a timing diagram similar to the one in Figure 15.6 (b) for an input current of $I_{in} = 1.9I_{ref}$. Clearly label the residue during each stage of the conversion. What is the total conversion time in terms of the clock period T_{clk}?

Problem 15.7

Assume that the error-correction mechanism shown in Figures 15.8 (a) and (b) is perfect and that the clock period is T_{clk}.

a) Estimate the attenuation of the comparator's input-referred noise power spectral density at a frequency $f << 1/T_{clk}$ due to the error-correction mechanism.
b) If f_{crnr}, the *1/f*-vs.-thermal-noise corner (see Section 7.8), is $<< 1/T_{clk}$, explain why input-referred *1/f*-noise and offset in the comparator are attenuated via the error-correction mechanism.

Problem 15.8

SAR ADCs with capacitive DACs are a popular architecture due to their good energy efficiency. The capacitive DAC in a SAR does not consume static power and can thus can be very energy efficient. Figure P15.8 of this problem presents a 'split-capacitor' switching technique designed to further lower the power of this DAC by reducing its average capacitive switching energy. To motivate the operation of this technique, we shall first examine the traditional SAR shown in Figure 15.4 (b). Suppose that the ADC shown in Figure P15.4 (b) samples an input voltage $v_{IN} = 0$ V onto the capacitive DAC array. Traditionally, the bottom plate of all the DAC capacitors, starting from the MSB capacitor, are sequentially connected to V_{ref}. If a conversion bit is evaluated to zero, the capacitor corresponding to that bit is then reset to GND. For the example of Figure P15.4 (b) with a zero input, at the beginning of the bit-cycling period, the bottom plate of the MSB capacitor (128C) is first connected to V_{ref}, then it is reset to GND after the MSB is evaluated to zero. On the next iteration, the bottom plate of the (MSB-1) capacitor (64C) is connected to V_{ref}, and then reset to ground after the bit is evaluated to zero, and so on. We can see that sequentially charging each capacitor to V_{ref} and then throwing away all the charge is wasteful of power for output codes where most of the bits are zeros.

The split-capacitor array in Figure P15.8 attempts to minimize wasted energy by splitting the capacitor corresponding to each bit into two half capacitors. During the sampling period, all the capacitors in this 5-bit example are connected to v_{IN}. Before the bit-cycling period, one half-capacitor corresponding to each bit (bit4 through the dummy) is connected to V_{ref} while the other half capacitor corresponding to that bit is connected to ground. This strategy is equivalent to connecting the MSB capacitor to V_{ref} as in the traditional case. During bit cycling, starting from bit 4 until bit 0, if the bit is evaluated to zero, the already charged half capacitor is reset to ground.

However, if the bit is evaluated to 1, the other non-charged half capacitor is connected to V_{ref}.

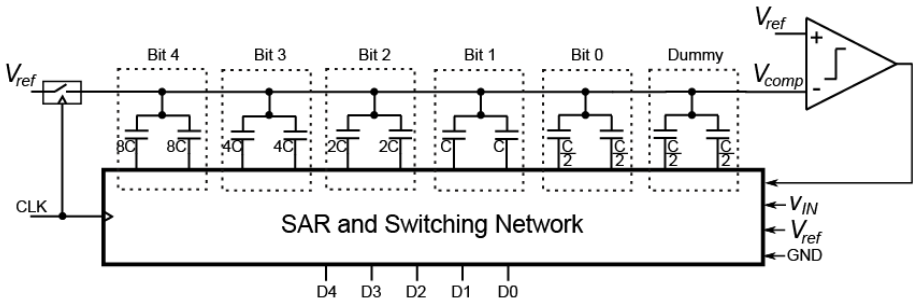

Figure P15.8: A successive-approximation register with split-capacitor array.

a) Verify that the two capacitive switching strategies (traditional and split-capacitor) produce the same sequence of voltages at V_{comp}.
b) For the 5-bit version of Figure P15.4, calculate the energy drawn from V_{ref}, in terms of V_{ref} and C during the bit-cycling period for an input voltage of v_{IN} = 0 V.
c) For the split capacitor scheme of Figure P15.8, calculate the energy drawn from V_{ref} during the bit-cycling period for v_{IN} = 0 V in terms of V_{ref} and C. How much energy does the split-capacitor scheme achieve compared to the traditional scheme for this particular input voltage? Which output code achieves the maximal energy saving?
d) For a 5-bit instantiation, write a computer program to calculate the energy drawn from V_{ref} (in terms of $CV_{ref}^2 / 2$) for all output codes for a conventional scheme and for a split-capacitor scheme. Plot your results on the same graph.

Problem 15.9

In this problem, we will investigate the idea of adiabatic switching as described in section 15.6 to understand how it can minimize switching energy in a capacitive DAC.

a) In Figure 15.15 (b), if the MSB capacitor is switched directly from ground to V instead of via multiple steps, calculate the energy drawn from V, and energy stored in the capacitor array, in terms of C_{eq} and V. What is the energy dissipated in the switch?
b) If the MSB capacitor is charged from ground to V in three steps as explained in section 15.6, calculate the total energy dissipated in the switches after the capacitor has been charged to V.
c) If instead of having three steps, the charging is done in N steps with equal voltage increments on each step, show that, in the limit of very large N, the energy dissipated in the switches converges to zero.
d) In practice, what would limit the savings with N, and would there, therefore be an optimal N?

Problem 15.10

In section 15.5, we discussed how op-amp-based switched-capacitor gain circuits in a pipelined ADC can be replaced by comparator-based gain circuits. In this problem, we will investigate the operation of the comparator-based gain circuit in more detail. Assume that $0 < v_{IN} < V_{ref}$.

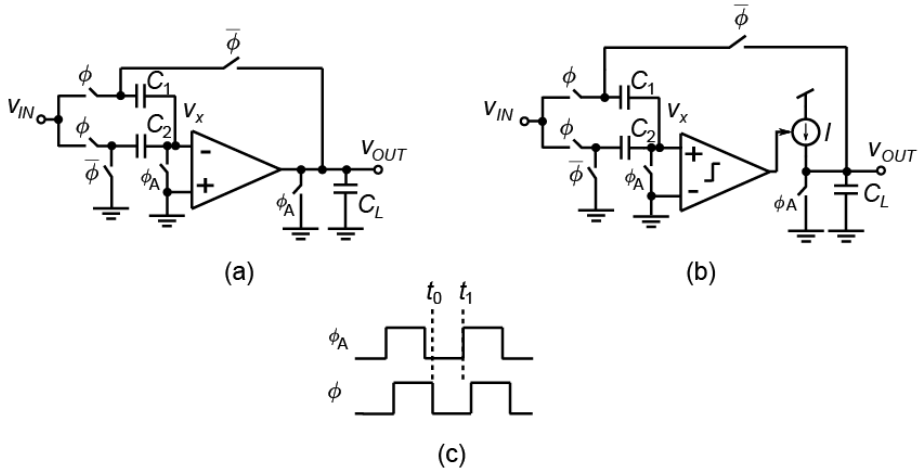

Figure P15.10: Circuits for a comparator-based gain circuit.

a) Consider the operational-amplifier-based gain circuit in Figure P15.10 (a). It operates on two clock phases, ϕ_A and ϕ where ϕ_A is a slightly advanced version of ϕ to make the circuit insensitive to parasitic capacitance at the node v_x. During a sampling phase, ϕ_A goes high resetting the node v_x to ground. The input voltage v_{IN} is sampled onto C_1 and C_2 once ϕ goes high. During a charge-transfer phase, the switches controlled by $\overline{\phi}$ are closed, connecting the left plate of $C_1$to v_{OUT} while connecting the left plate of C_2 to ground. Determine $v_{OUT}(t_1)$, the output voltage at the time of the rising-edge of ϕ_A as shown in Figure P15.10 (c), as a function of $v_{IN}(t_0)$. Assume that the periods of ϕ_A and ϕ are long enough such that v_{OUT} has stabilized.

b) The role of the op-amp is to force the virtual ground condition at v_x. In Figure P15.10 (b), the op-amp is replaced with a comparator and a current source I. The sampling phase is the same as described in a). During the charge-transfer phase, the left plate of C_2 is connected to ground while the left plate of C_1 is connected to v_{OUT}. The current source is turned on when the output of the comparator is low. Once the output of the comparator goes high, it shuts off the current source I. Sketch the voltage at node v_x as a function of time during the charge transfer phase (from t_0 to t_1). Also sketch the voltage at v_{OUT} as a function of time during the charge-transfer phase. Assume that the current I is large enough such that both node voltages have stabilized before t_1. What is the final value of v_{OUT}?