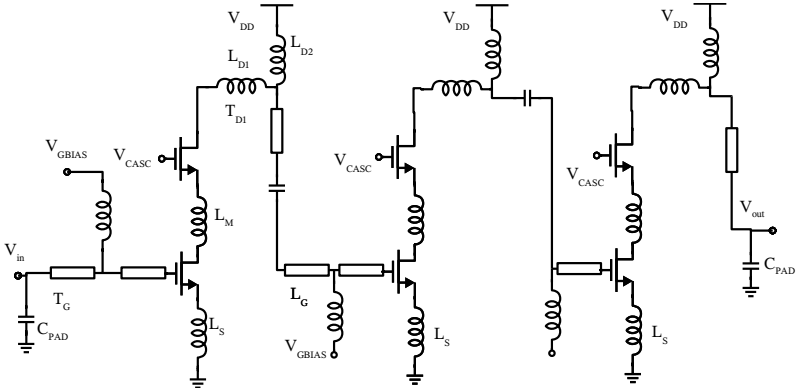
Circuit Topologies & Analysis Techniques in HF ICs

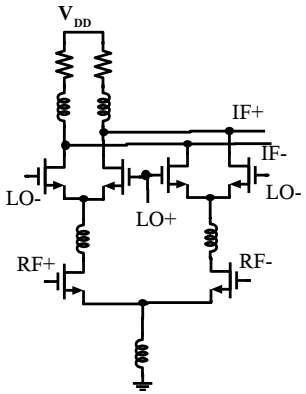
Outline

- Analog vs. Microwave Circuit Design
- Impedance matching
- Tuned circuit topologies
- Techniques to maximize bandwidth
- Challenges in differential HF circuits
- Nonlinear Techniques

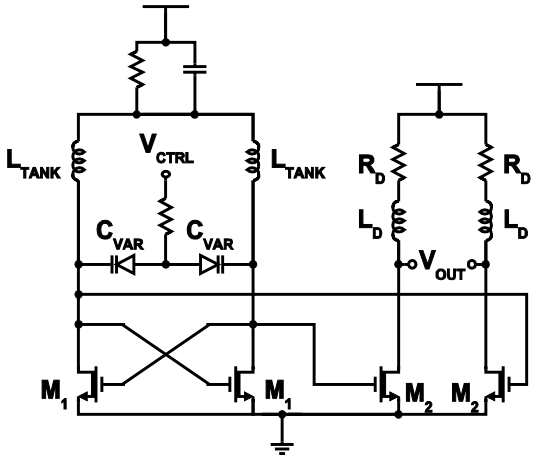
Typical HF IC Topologies: inductors



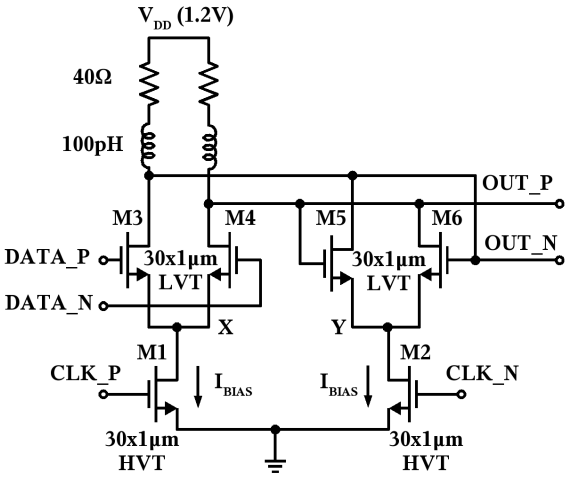
LNA



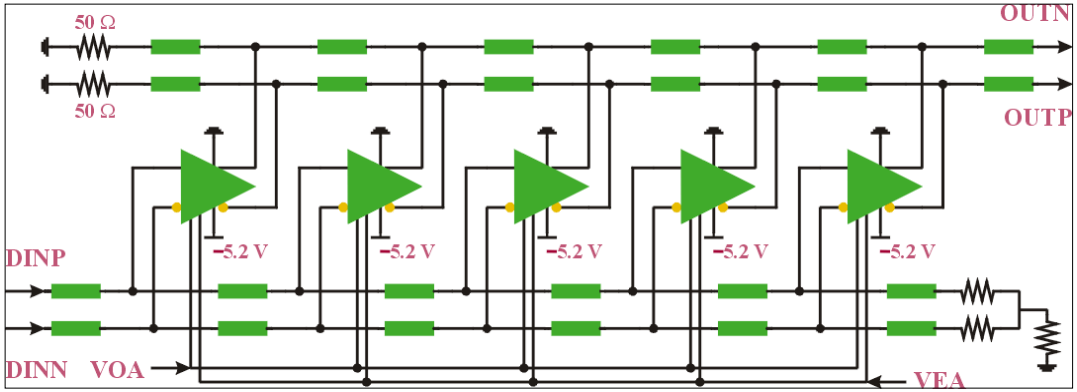
Mixer



VCO

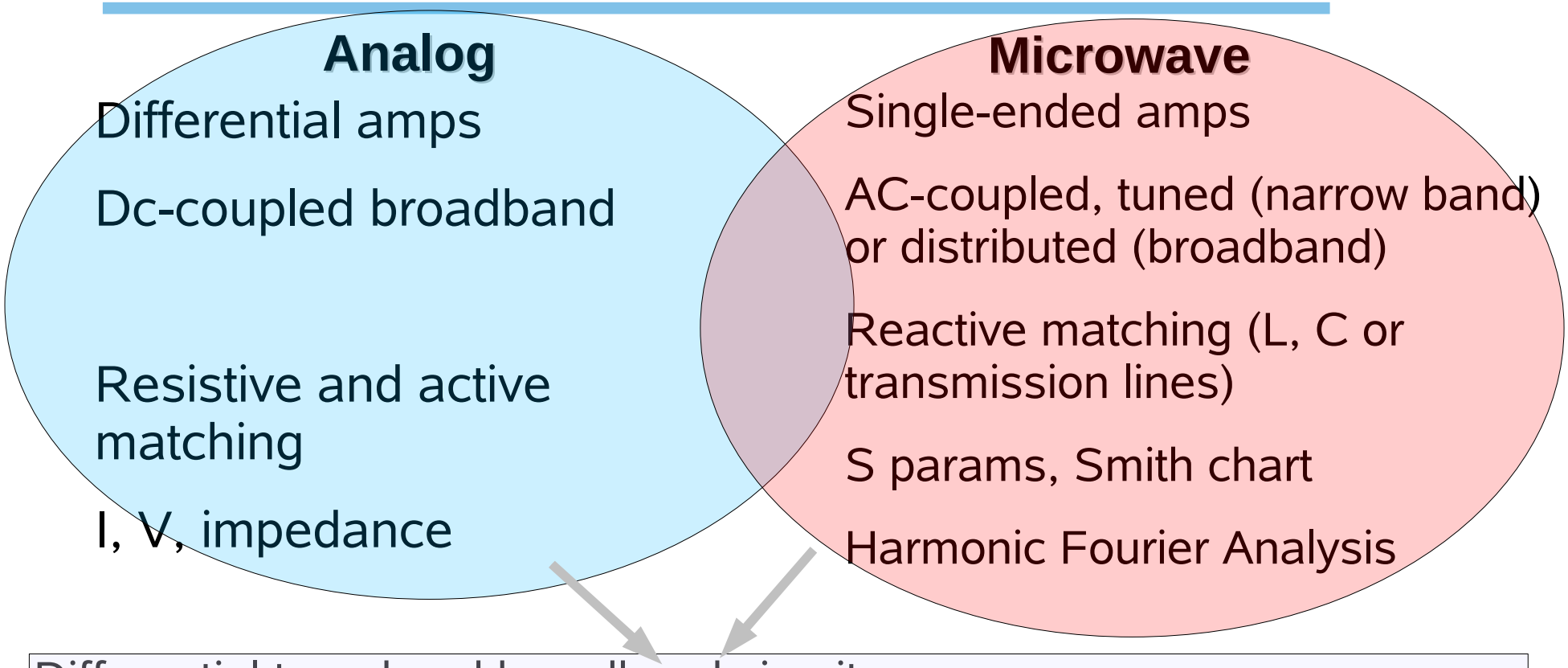


CML-LATCH



Broadband High-speed Driver

Analog vs. Microwave Circuit Design



Differential tuned and broadband circuits

Resistive, active, and reactive matching

Common mode, differential mode, and single-ended mode gain, impedance, matching and stability

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Why do we need impedance matching at HF?

•Distance between circuit pads and external terminations ~ λ.

Impedance mismatches at either end cause reflections

•Need maximum power transfer from source to load

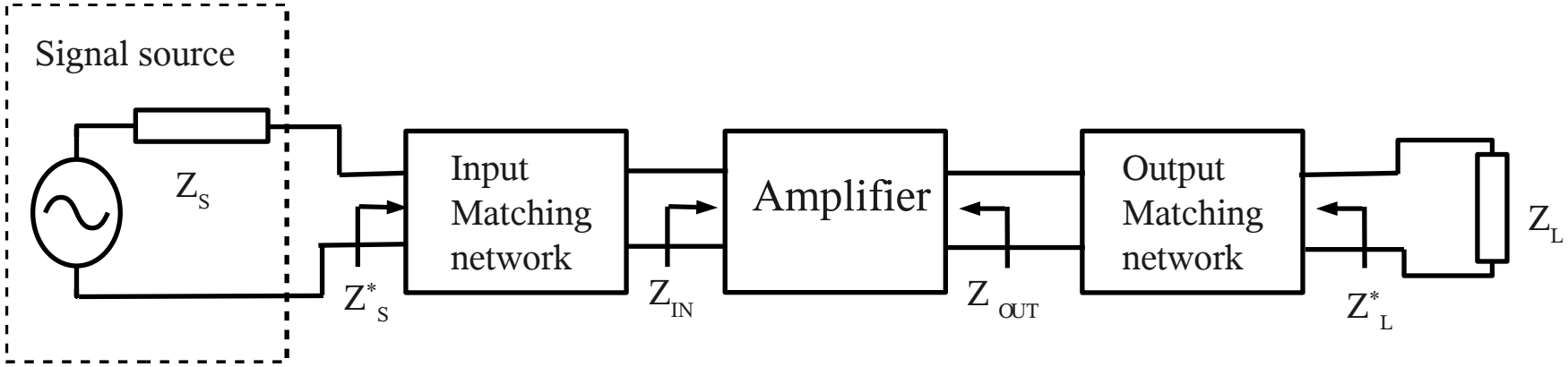
•Typical matching impedance

- 50 Ω per side (SE),
- 100 Ω diff-mode, and
- 25 Ω in CM.

Why not at LF?

- Circuits small compared to wavelength
- Can afford to lose power since transistors have lots of gain
- Resistive matching is used to avoid large area caps and inductors

Concept of Impedance Matching



Narrow-band tuned matching networks

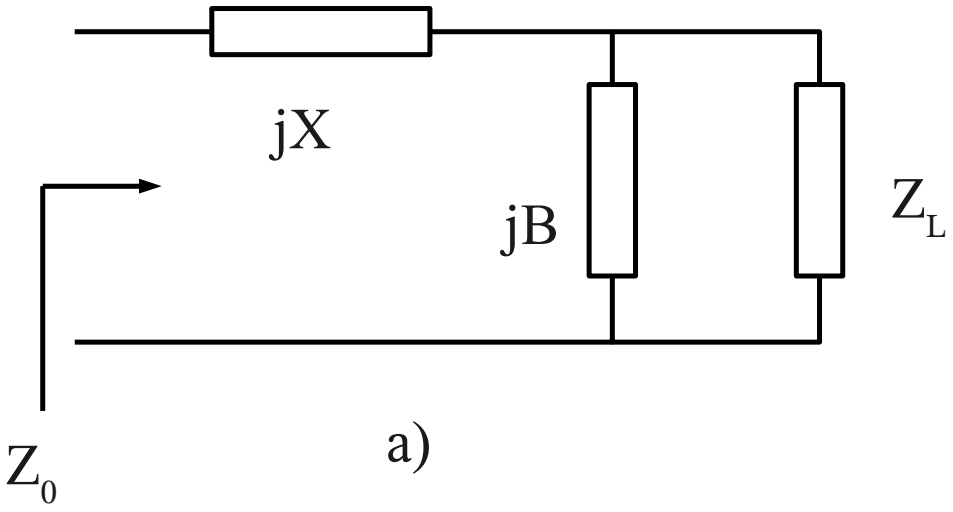
Input/output of transistors look like parallel or series R-C circuits.

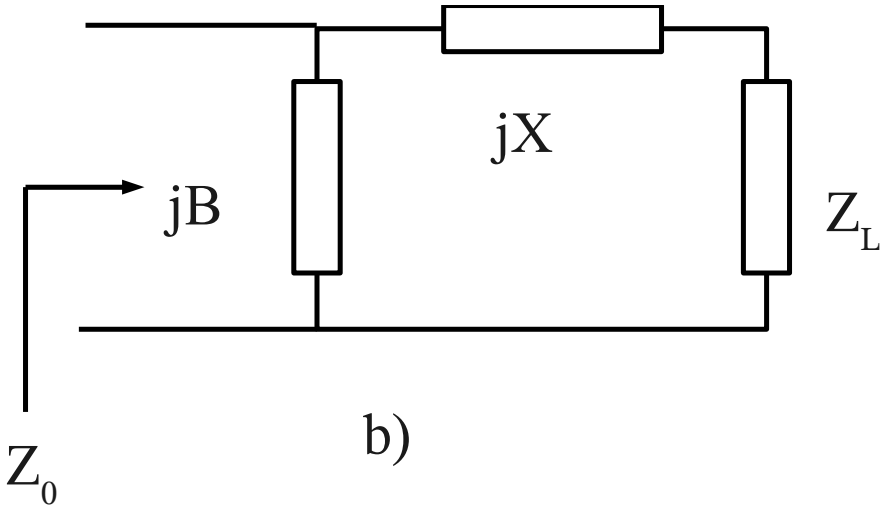
- L-network matching:
  - With lumped components
  - With transmission lines
- Multi-section matching
- Transformer matching

L-Section matching

Two lumped or t-line components can match any impedance with non-zero real part to Z_o

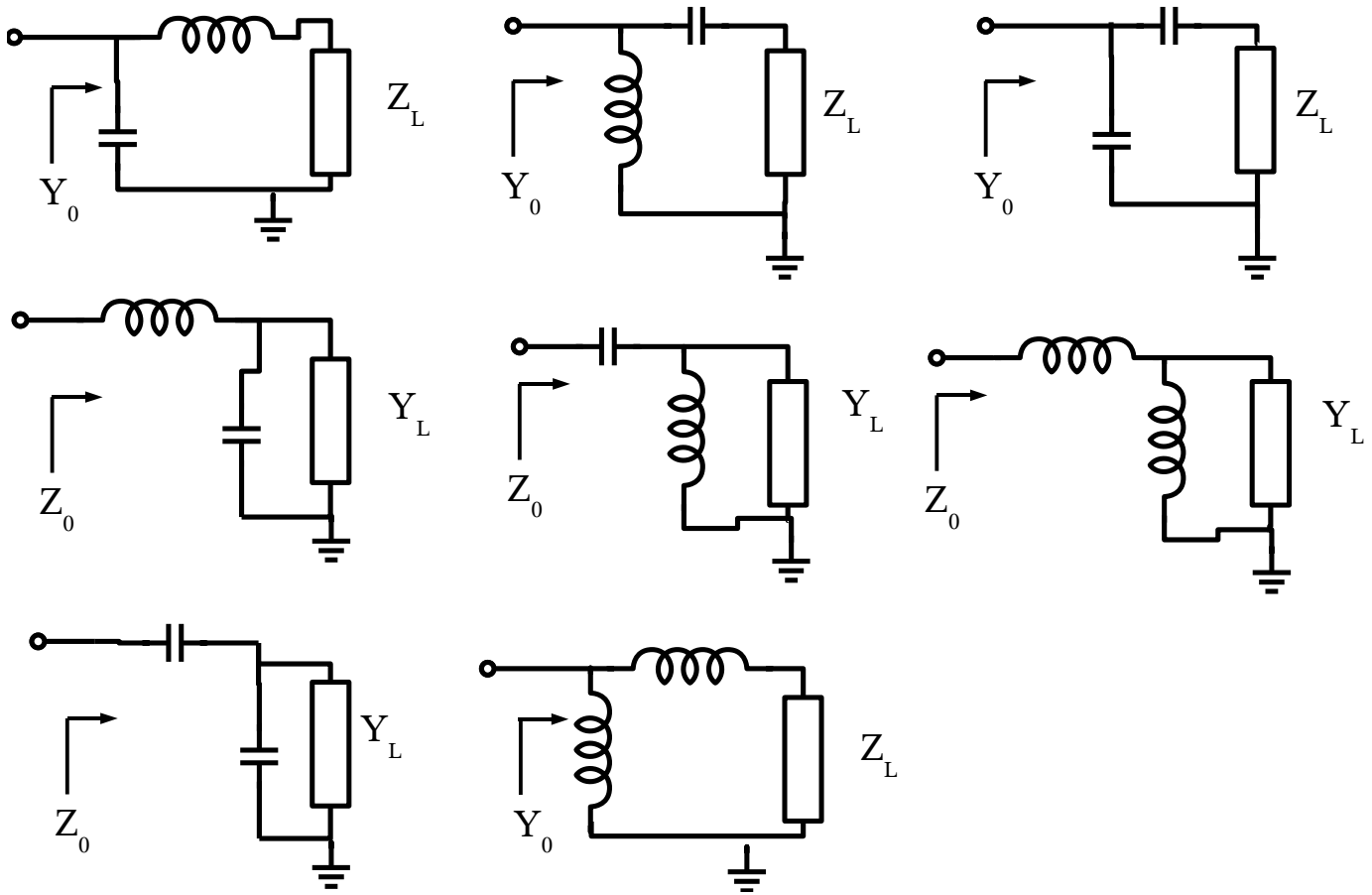
- Series jX, shunt jB used when z_L is inside 1+jx circle
- Shunt jB, series jX used when z_L is outside 1+jx circle



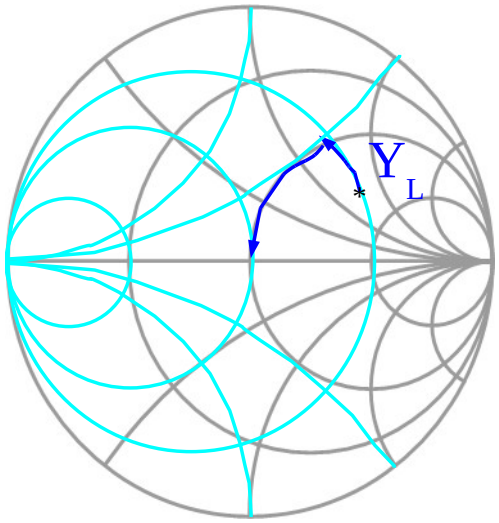


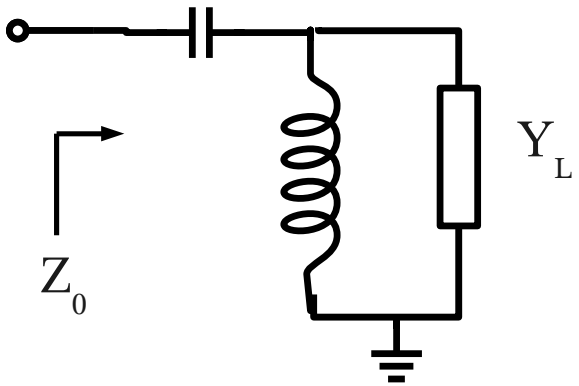
L-section matching (ii)

- 8 possible matching circuits exist
- Exact analytical and graphical solutions



Example YZ-Smith Chart: z_L :inside 1+jx circle

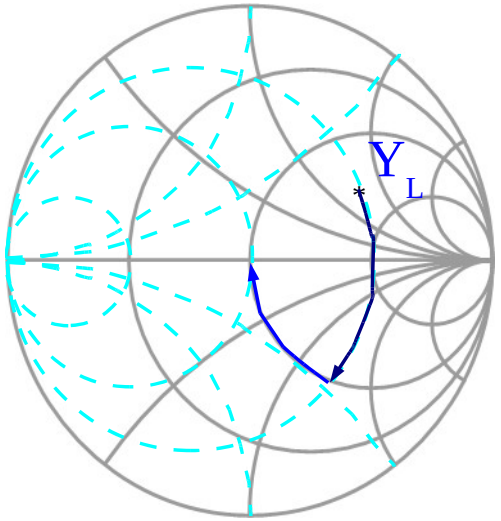


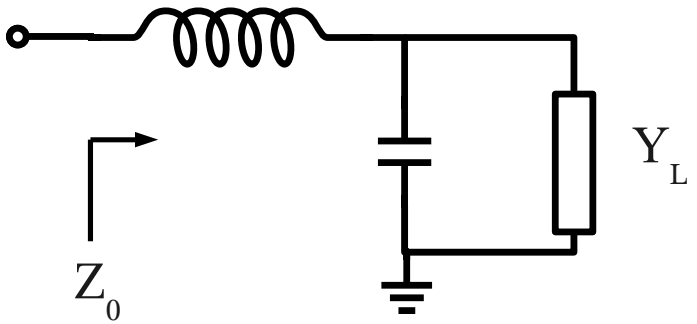


$Y_L = 0.3 - j0.3$

$b_1 = -j0.16$

$x_2 = -j1.53$



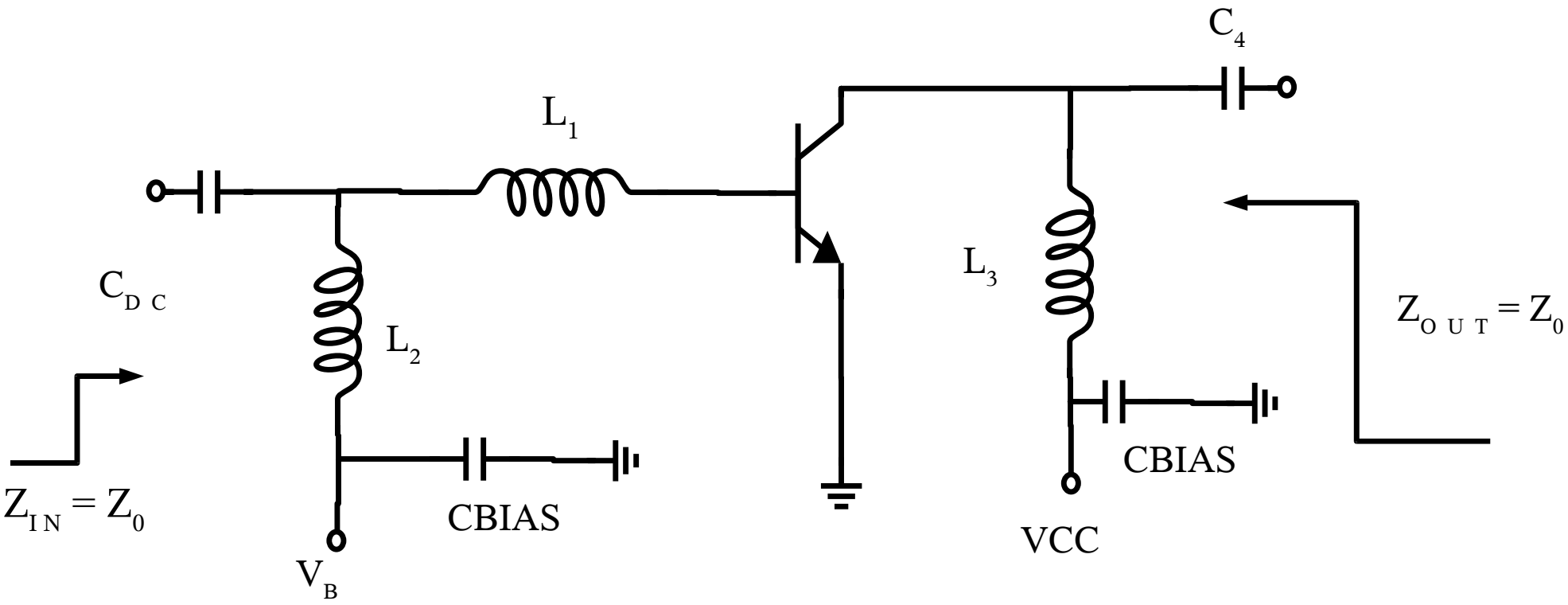


$b_1 = j0.757$

$x_2 = j1.53$

How do we select between multiple solutions?

Example: 120-GHz HBT amplifier



Q and BW_{3dB} of L-section matching network

L-sections are 2nd order (two-pole) LPF or HPF networks

- Node Q: $Q_n = \frac{|B_P|}{G_P}$ $Q_n = \frac{|X_S|}{R_S}$
- Loaded Q
- Bandwidth $Q_L = \frac{f_0}{BW_{3dB}} = \frac{Q_n}{2}$

Two typical scenarios encountered in practice:

- High Q matching in PAs
- High bandwidth matching

In either case you need more matching elements, not just 2 as in L-section: 2-step L-section, π, and T-networks

Lossless broadband input/output matching

Higher-order lossless filter networks can be employed to maximize the matching bandwidth.

Ultimate limitation for broadband matching with “lumped” elements is given by the *Bode-Fano limit* .

Example: For parallel R-C load:

$$\int_0^\infty \ln \frac{1}{\left|S_{11}(\omega)\right|} d\omega \leq \frac{\pi}{RC}$$

Using t-coils and distributed amplifier topology one can overcome this limit

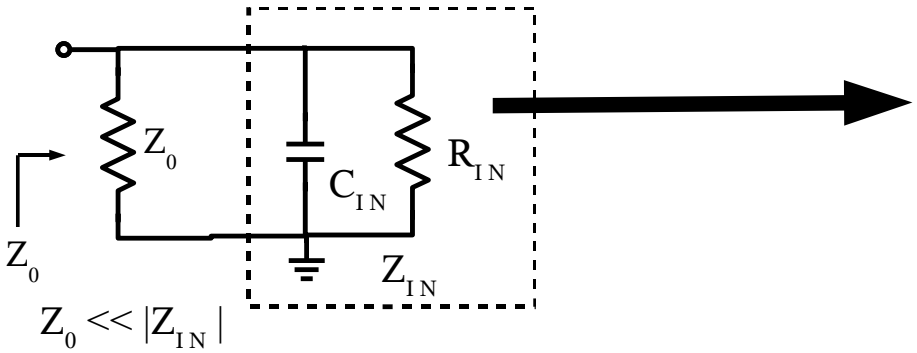
Lossy broadband input matching techniques

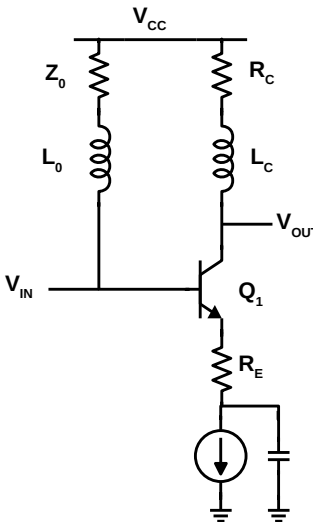
- Brute force
- Negative feedback

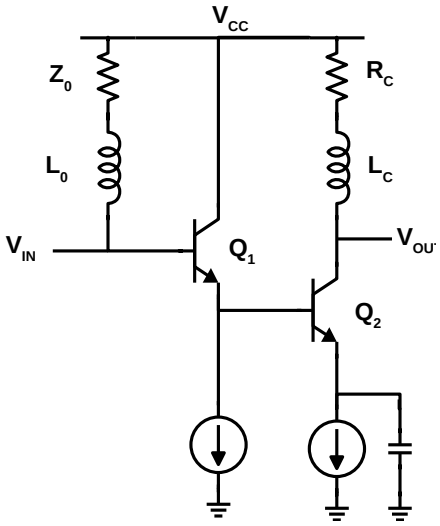
Lossy matching: Brute force

Add Z_o resistor in parallel with high impedance input/output.

Use series inductor to tune out input capacitance



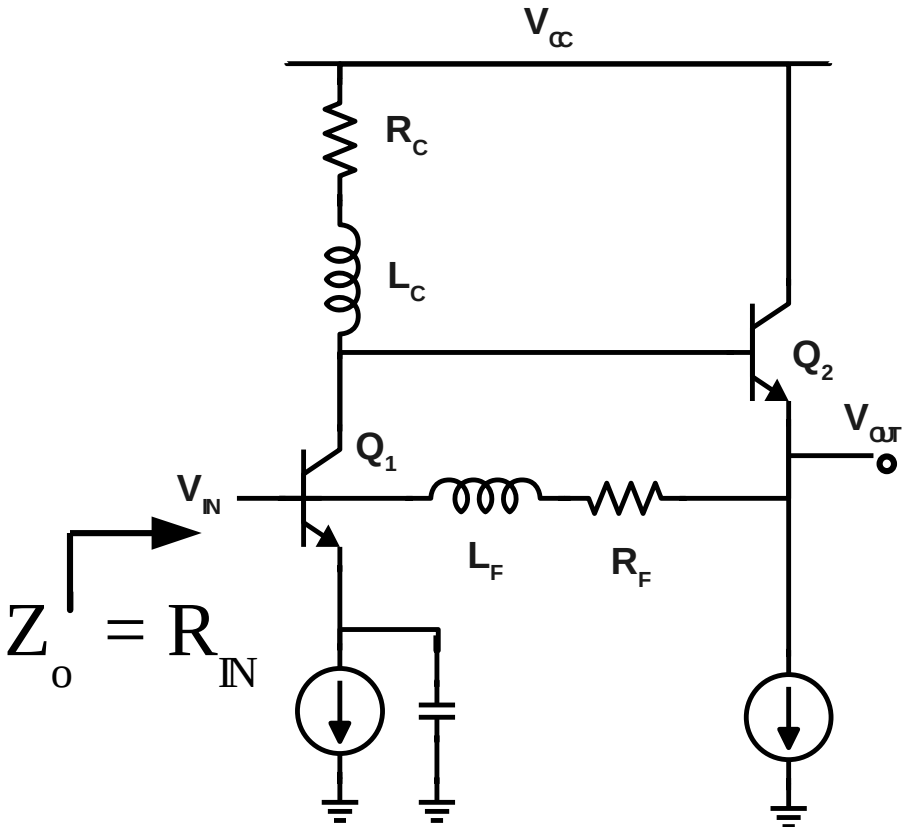


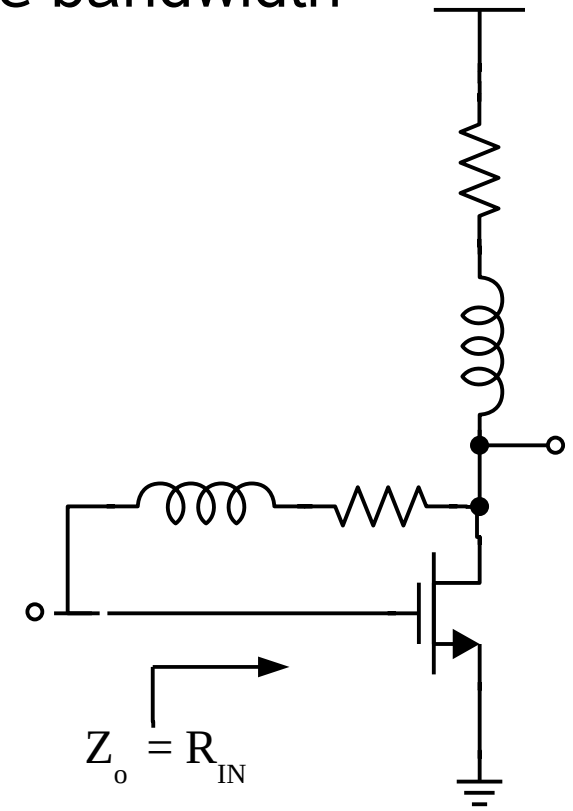


$$Z_{IN}(\omega) \approx \frac{Z_0\left(1 + j\omega\frac{L_0}{Z_0}\right)}{1 - \omega^2 C_{IN} L_0 + j\omega Z_0 C_{IN}}$$

Lossy matching: negative feedback

TIA input: low-noise, low-current, large bandwidth





$$Z_{IN}(\omega) = \frac{Z_F}{A+1} \frac{1}{1 + j\omega \frac{Z_F C_{IN}}{A+1}}$$

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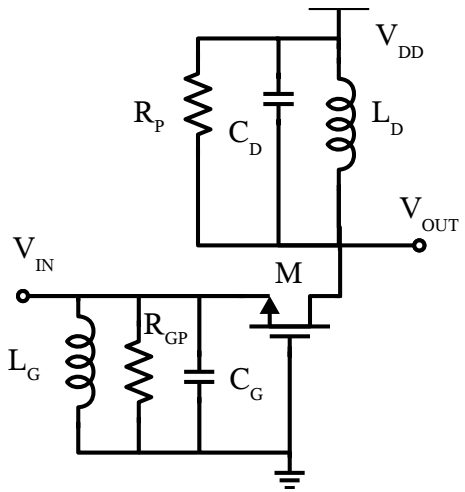
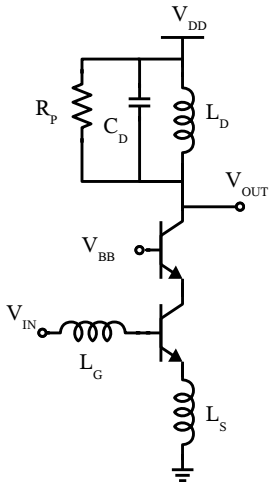
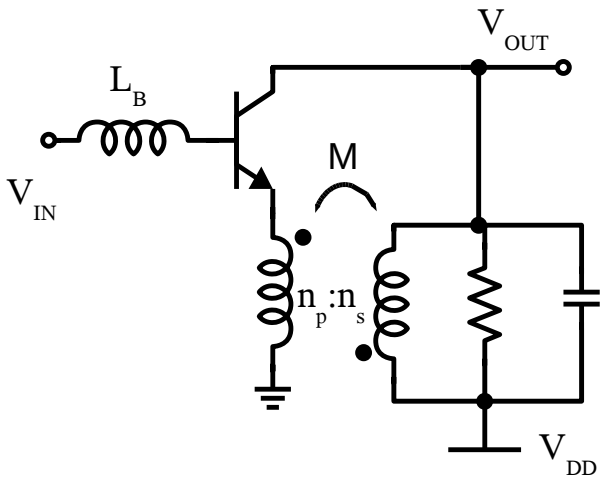
Tuned circuit topologies

Topologies:

- Tuned amplifier with parallel resonant tanks at input and output (CE/CS, CB/CG) (PAs, LNAs)
- Tuned amplifier with series resonance at input and parallel resonance at output (LNA with inductive degeneration)
- Tuned amplifiers with selective negative feedback







Analysis techniques for tuned circuits

Two-step analysis technique

- Match input/output circuit at "resonant" frequency f_o
- Analyze circuits at resonant frequency f_o by shifting entire frequency response to DC.

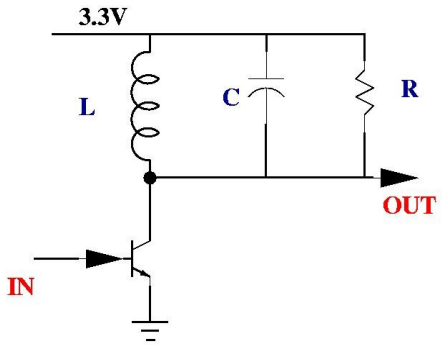
Apply the same methodology as in DC amplifiers to calculate midband gain, input and output impedance

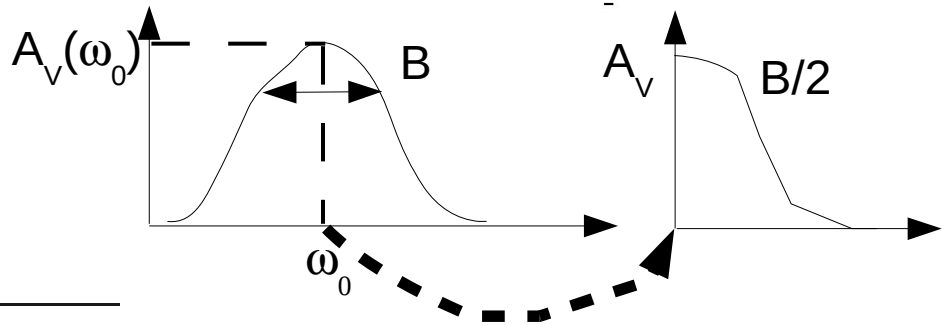
Q of resonant circuits and f_o dictate gain bandwidth

Example of single-tuned amplifier analysis

Basic topology

- CE or CS stage with resonant parallel RLC load (single-tuned circuit)

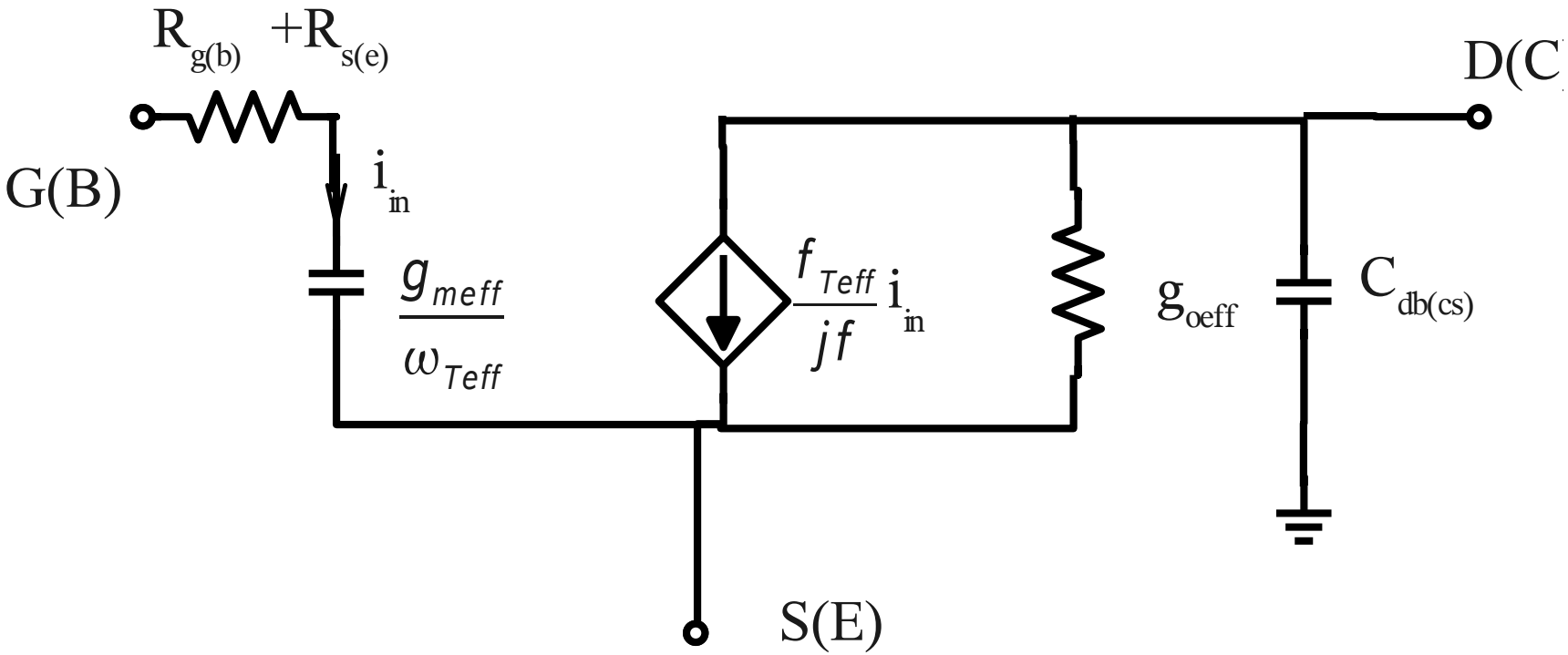




$$A_v(s) = -g_m Z_L(s) = \frac{-g_m}{C} \frac{s}{s^2 + \left(\frac{1}{CR}\right)s + \frac{1}{LC}}$$

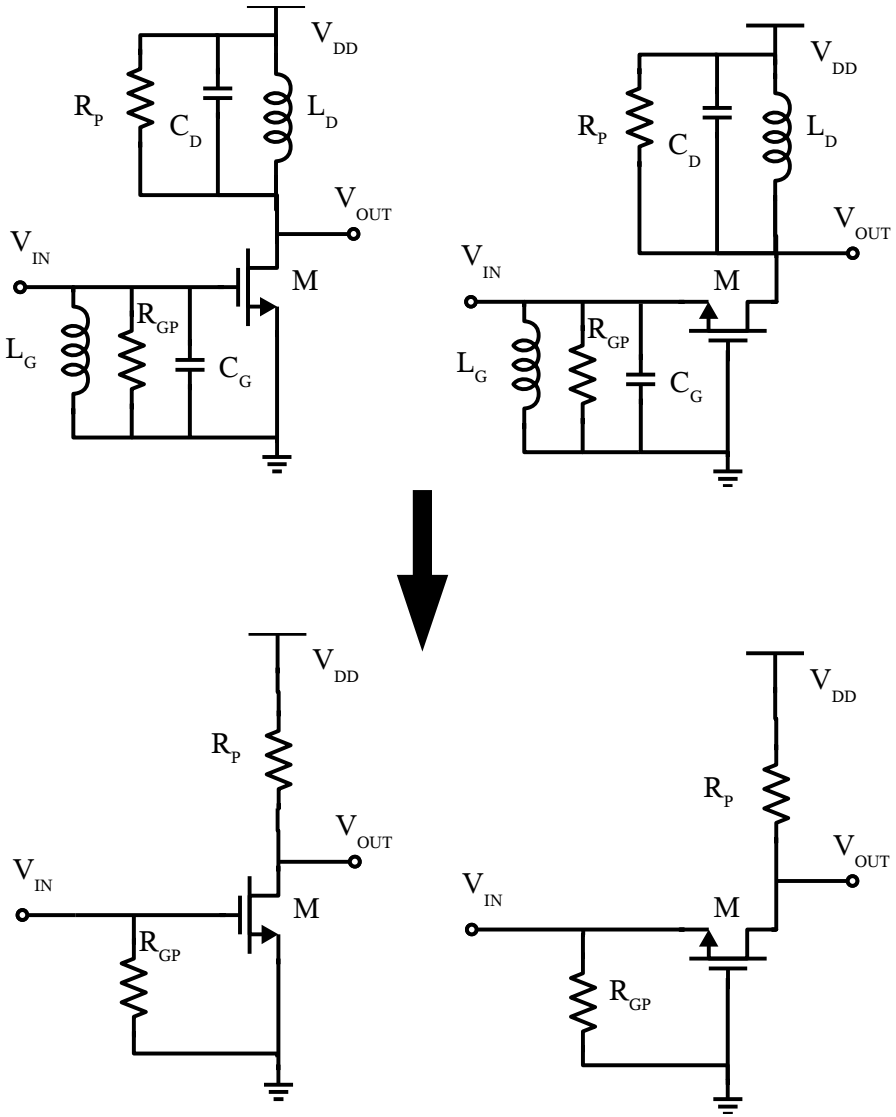
$$A_v(\omega_0) = -g_m R \text{ where } \omega_0 = \frac{1}{\sqrt{LC}};\ Q = \omega_0 C R \text{ and } B = \frac{1}{CR}$$

Simplified FET/HBT circuit for analysis



- Useful in CE/CS configuration
- No Miller capacitance

Ex. 1: at f_o they simplify to…



- $i_{sc}(f_o) = (+/-)g_m v_{in}$
- $Z_{OUT}(f_o) = R_P$ (includes r_o, loss resistance of L_D)
- $R_{IN}(f_o) = R_{GP}$ (includes R_g, loss resistance of L_G)
- $A_v(f_o) = i_{sc} \times R_{out} = (+/-)g_m R_P$

Ex. 1: Power gain calculation (ii)

Input and output- matched CS or ac-coupled cascode stage: $R_{in} = R_{GP} = Z^*_s$, $Z^*_L = Z_{OUT} = R_P$

$$v_{out} = \frac{i_{sc} \times R_P}{2} = \frac{-g_m \times R_P}{2} v_{in} \qquad i_{load} = \frac{i_{sc}}{2} = \frac{-g_m \times v_{in}}{2}$$

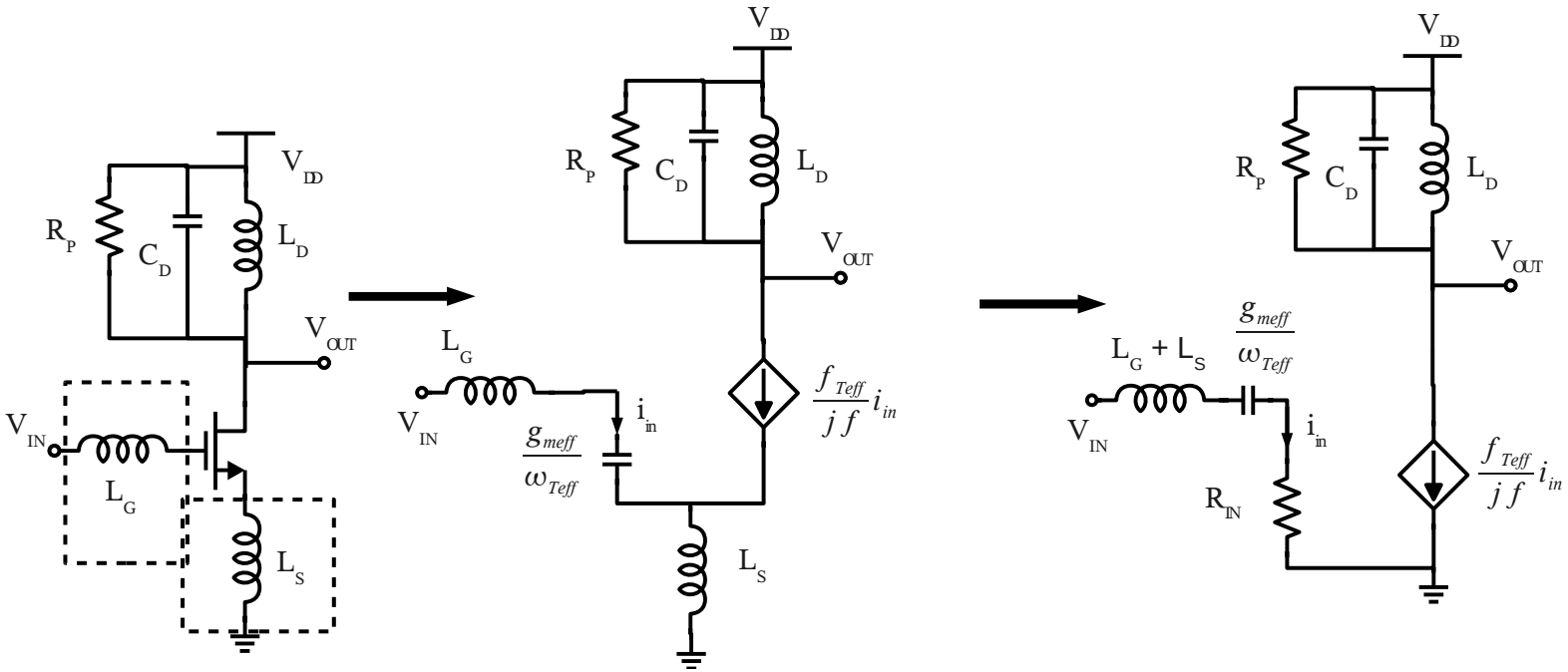
$$P_{load} = v_{out} \times i^*_{load} = \frac{g_m^2 \times R_P}{4} |v_{in}|^2 \qquad P_{in} = v_{in} \times i^*_{in} = \frac{v_{in} \times v^*_{in}}{R_{GP}} = \frac{|v_{in}|^2}{R_{GP}}$$

$$G = \frac{P_{load}}{P_{in}} = \frac{g_m^2 \times R_P \times R_{GP}}{4}$$

Prove that, for an input and output matched CG stage the power gain is the same as above!

What does it mean?

Ex. 2: Tuned CE/CS or cascode stage with inductive degeneration



- Series resonance at input
- Parallel resonance at output
- Used in LNAs, mixers

Example 2: Continued

- Account for R_S in C_{gs}, g_m, g_o, f_T
- Transfer C_{gd} in parallel with C_{gs}
- Replace $C_{gseff} + C_{gd}$ with g_{meff}/ω_{Teff}

Step 1: Calculate input impedance

$$Z_{in} = R_g + R_s + \omega_{Teff} L_S + j\left[\omega(L_G + L_S) - \frac{\omega_{Teff}}{\omega\, g_{meff}}\right]$$

Step 2: Calculate output short-circuit current i_{sc}

$$i_{sc} = \frac{-f_{Teff}}{jf} i_{in} = j\frac{f_{Teff}}{f} i_{in}$$

Example 2: (iii)

Step 3: Match the input impedance to Z_0 and terminate (match) the output on R_P

$$Z_0 = R_{IN} = R_s + R_g + \omega_{Teff} \times L_S \quad and \quad Z_L = R_P$$

Step 4: Calculate the current in load (R_P) and output power

$$i_{load} = \frac{i_{sc}}{2} = \frac{-f_{Teff}}{2jf} i_{in} \qquad v_{out} = \frac{i_{sc} \times R_P}{2} = \frac{-f_{Teff} \times R_P}{2\mathrm{j}f} i_{in}$$

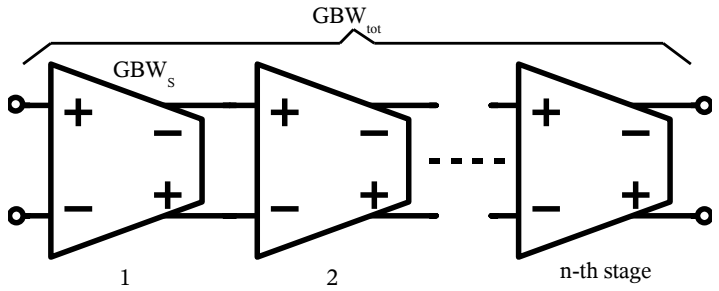
$$P_{in} = v_{in} \times i_{in}^* = i_{in} \times R_{IN} \times i_{in}^* = R_{IN} |i_{in}|^2$$

$$G = \frac{P_{load}}{P_{in}} = \frac{f_{Teff}^2}{4f^2} \times \frac{R_P}{R_{IN}}$$

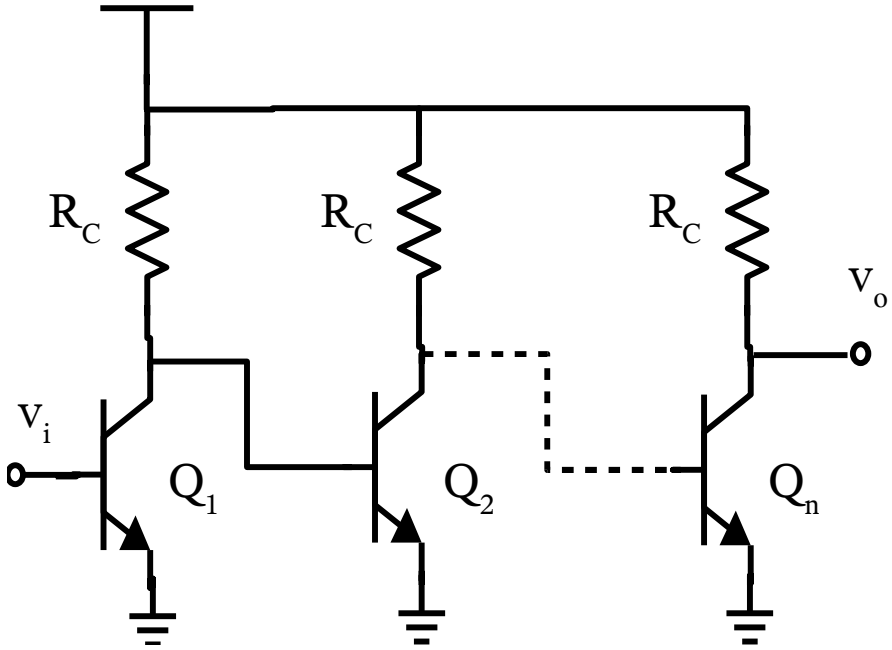
$$P_{load} = v_{out} \times i_{load}^* = \frac{f_{Teff}^2 \times R_P}{4f^2} |i_{in}|^2$$

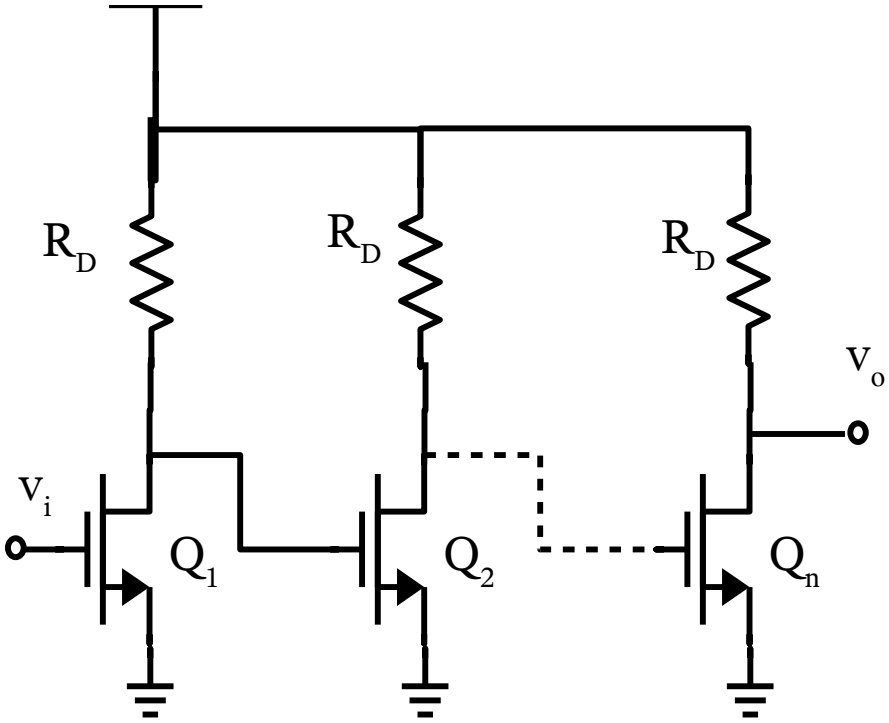
Topologies and techniques to maximize circuit bandwidth

BW decreases as number of cascaded stages increases



$$\frac{GBW_{tot}}{GBW_S} = A_{tot}^{1-1/n} \times \sqrt{2^{1/n}-1} \quad \textit{for 1st. order stages}$$





Technique to analyze bandwidth

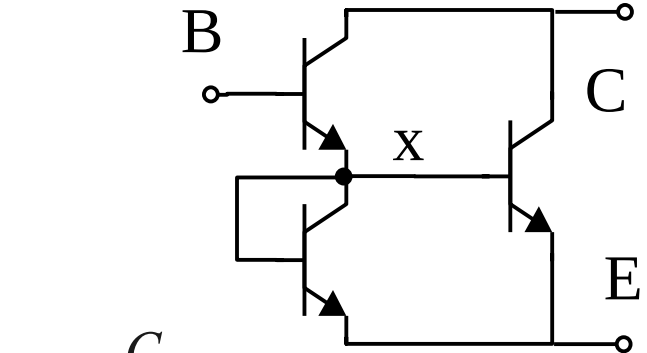
Open time constant technique (Elmore delay)

Allows to calculate dominate pole with reasonable approximation

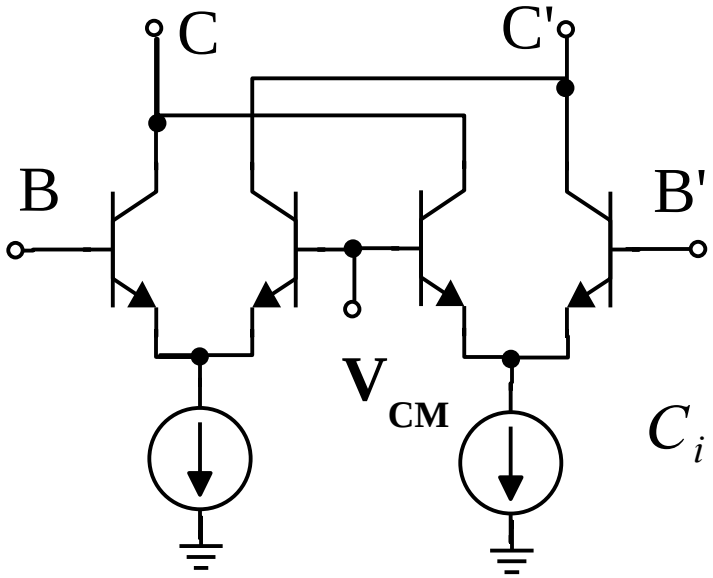
How to improve circuit bandwidth?

- Use faster transistors
- Use broadband circuit topologies and techniques
  - Reduce the input capacitance of the amplifier stage
  - Cherry-Hooper stage
  - Buffering and scaling of stages
  - Use inductive peaking and distributed amp. topologies

Reducing input capacitance: f_T doubler



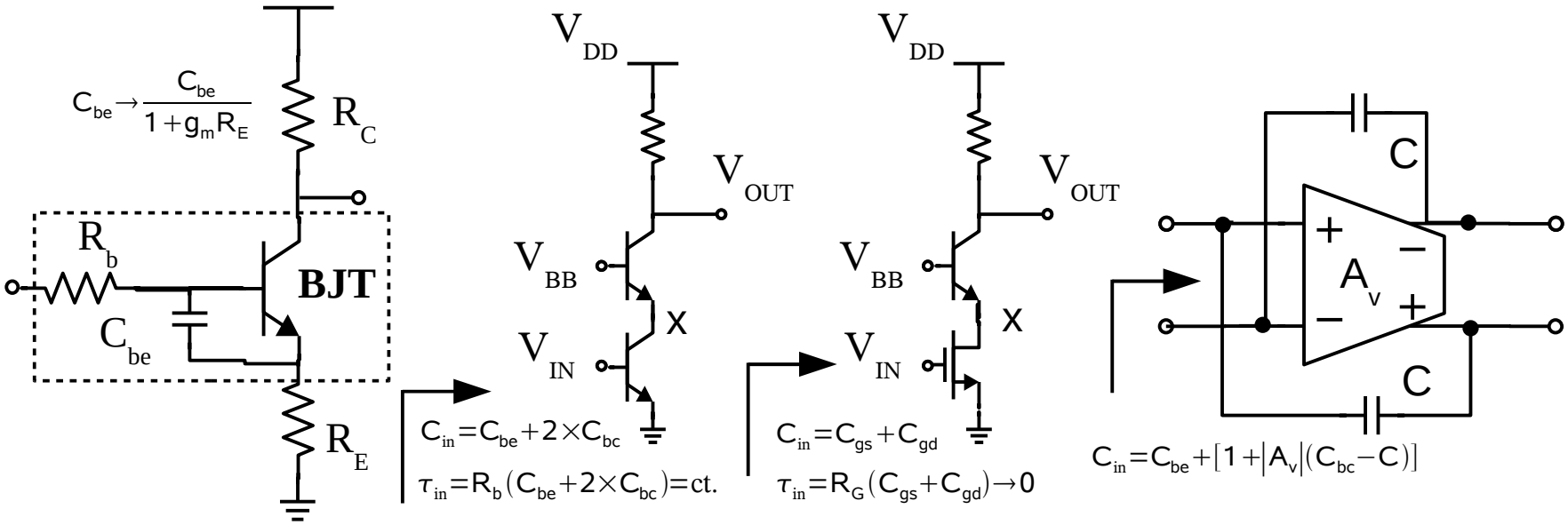
$$C_{in} \approx \frac{C_{be}}{2}$$



$$C_i = \frac{C_{be}}{2}$$

- Useful if current gain rather than power gain is important
- Works well if C_{be} (C_{gs}) >> C_{bc}, C_{cs} (C_{gd}, C_{db})
- Efficient in HBT implementation but consumes more power
- MOSFET implementation suffers from additional C_{db}, C_{sb}

Reducing input capacitance (ii)



a) Series resistive feedback (emitter degeneration)

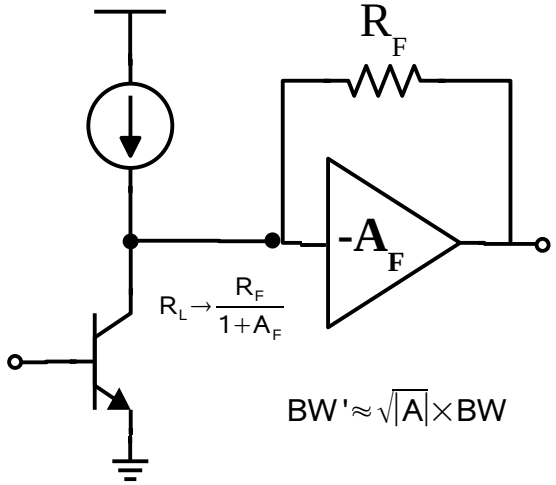
b) Reduce Miller capacitance with cascode (HBT > MOS)

c) Reduce Miller and $R_g \times C_{in}$ with BiCMOS cascode

d) Cancel out Miller cap with positive feedback (dangerous)

e) Combinations of all of the above

Speed-up input & output poles: Cherry-Hooper



$$\tau_{pCE} = R_b[C_{be} + C_{bc}(1+|A|)] + R_C(C_{be} + C_{cs})$$

$$\tau_{pCH} = R_b\left[C_{be} + \left(1 + \left|\frac{A}{A_F}\right|\right)C_{bc}\right] + \frac{R_F}{|A_F|}(C_{bc} + C_{cs}) \approx \frac{\tau_{pCE}}{|A_F|}$$

$$A(s) \approx \frac{-g_{meff}R_F}{\left[1 + \frac{s}{1+A_{F0}}\left(\frac{1}{\omega_p} + \frac{1}{\omega_F}\right) + \frac{s^2}{(1+A_{F0})\omega_p\omega_F}\right]} = \frac{A}{1 + \frac{s}{Q\omega_0} + \frac{s^2}{\omega_0^2}}$$

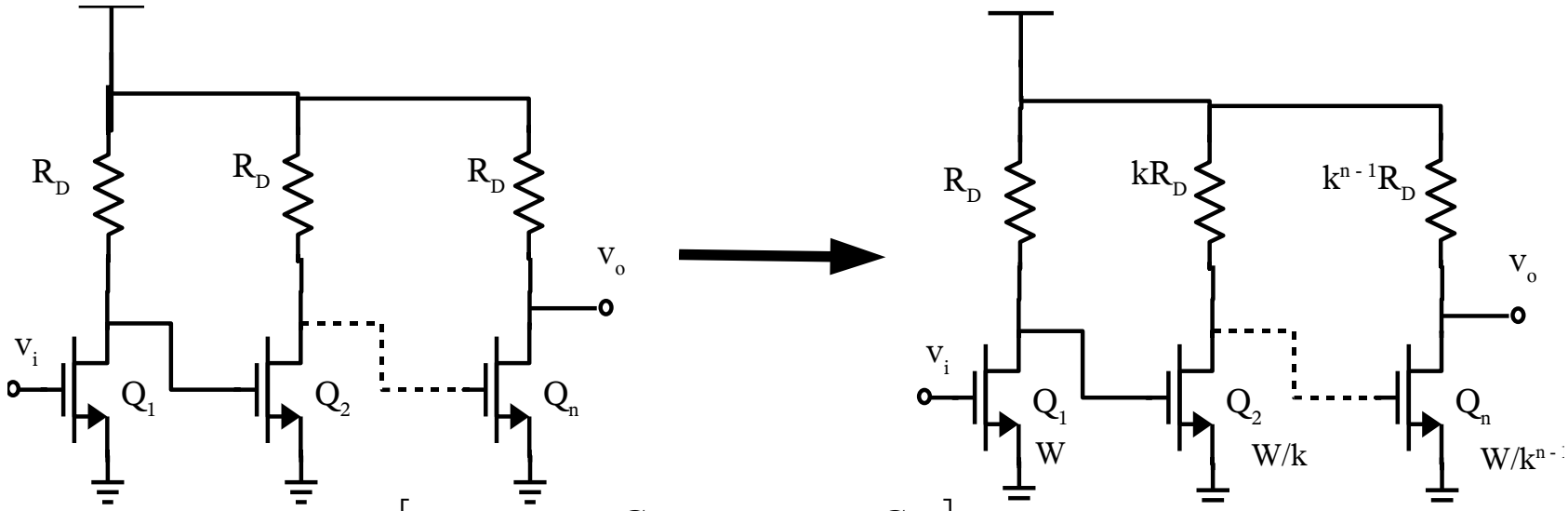
A=overall gain

$R_F = R_C$

$$\omega_0 = \sqrt{(1+A_{F0})\omega_p\omega_F} \qquad Q = \frac{\omega_0}{\omega_p + \omega_F} = \frac{\sqrt{(1+A_{F0})\omega_p\omega_F}}{\omega_p + \omega_F}$$

- Bipolar implementation is common but requires high (3.3V and up) power supply (1.8-V possible in SiGe BiCMOS)
- 1.2 V CMOS implementations possible (3-stacked LVT FETS)

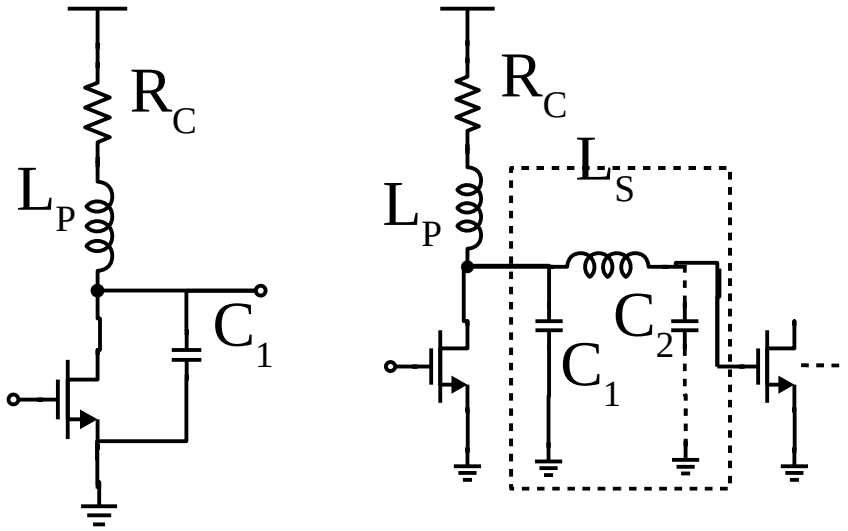
(Buffering) and Scaling



$$\tau_p = (R_D \| r_o)\left[C_{gd} + C_{db} + \frac{C_{gs}}{k} + (1+|A_0|)\frac{C_{gd}}{k}\right] + R_g\left[C_{gs} + (1+|A_0|)C_{gd}\right]$$

- Reduce output node capacitance by decreasing the bias current and size of each following stage
- Works in input amplifier of broadband receivers but limited by minimum size transistor
- Buffering works in BJT circuits by using EF+ INV

Tune out node cap: inductive peaking (1930's)



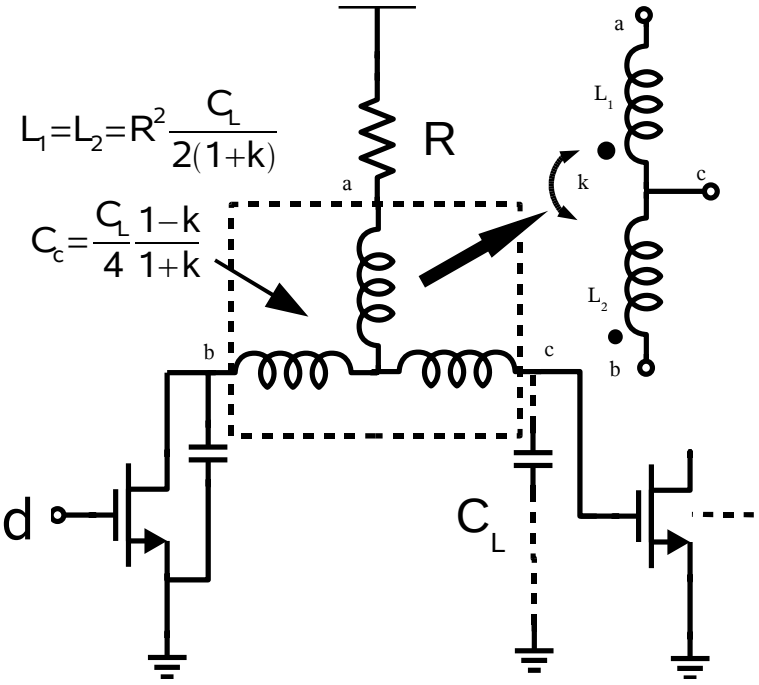
$$A_v(s) = A_o \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{Q\omega_0} + \frac{s^2}{\omega_0^2}} \qquad Q = \frac{1}{R_C}\sqrt{\frac{L_P}{C_1}}$$

$$A_0 = -g_{meff} R_C;\ \omega_0 = \frac{1}{\sqrt{L_P C_1}};\ \omega_z = \frac{R_C}{L_P} = \frac{\omega_0}{Q}$$

a) Shunt peaking: about 1.6xBW

b) Shunt-series peaking: about 2xBW

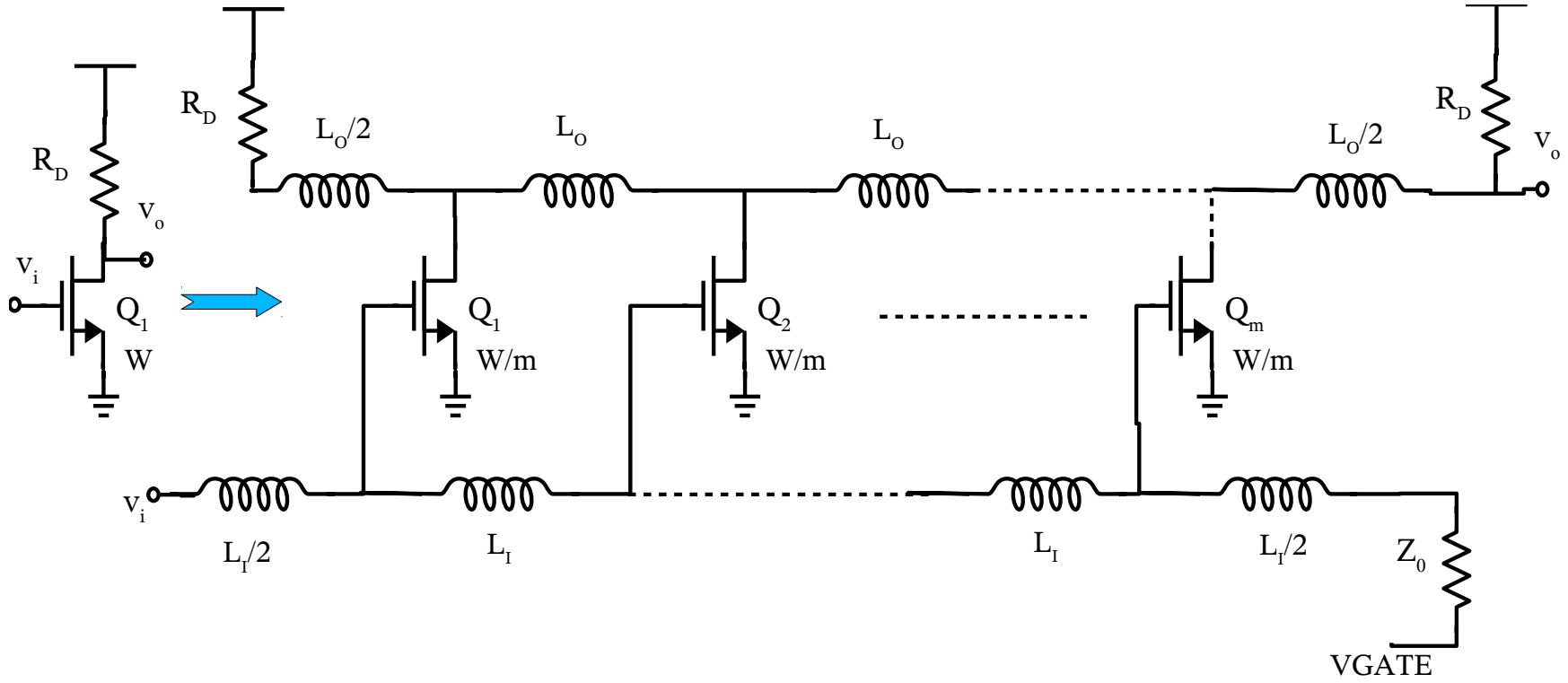
c) Shunt and double-series, t-coil > 2.8xBW (T. Lee, 1998). C_c is connected between nodes a and b.



Distributed amplifier

Absorb input and output capacitance in artificial t-line

Parcival 1936



Distributed amplifier

$$Z_0 = \sqrt{\frac{L}{C}} \text{ and } BW_{3dB} = \frac{1}{\pi\sqrt{LC}}$$

$$L_I = Z_0^2 \frac{C_I}{m} \text{ and } L_O = R_D^2 \frac{C_O}{m}$$

$$GBW_S = \frac{g_{meff}}{2\pi(C_I + C_O)}$$

$$GBW'_S = min\left(m\frac{g_{meff}}{2\pi C_I}, m\frac{g_{meff}}{2\pi C_O}\right)$$

$$A = -m\frac{g_{meff}}{m}\frac{R_D}{2} = -g_{meff}\frac{R_D}{2}$$

$$BW_{3dB} = min\left(\frac{1}{\pi\sqrt{L_I\frac{C_I}{m}}}, \frac{1}{\pi\sqrt{L_O\frac{C_O}{m}}}\right)$$

Challenges in diff. circuits at HF

•No common mode rejection (current sources are capacitive, especially the “advanced” ones)

•The differential pair transistors are capacitively degenerated in common-mode leading to additional stability problems.

•Coupling between differential inputs due to capacitive input impedance.

•Differential impedance is no longer 2×single-ended impedance.

How to verify stability

In single-ended, differential, and common mode check for:

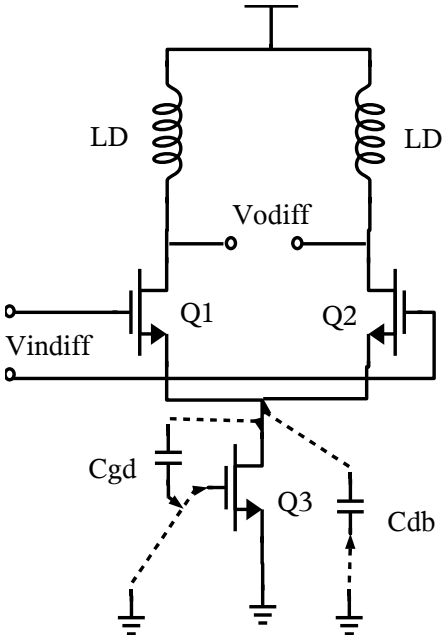
- $k < 1$ at any port
- $S_{ii} > 1$ at any port i
- negative resistance at any port
- peaking > 1dB in gain vs. frequency characteristics
- check for any of the above between stages if suspicious...
- In amplifiers with feedback, check for the closed loop phase margin (>60°) in DM, CM, and SE mode.

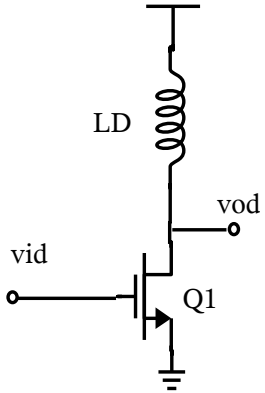
Common reasons for instability

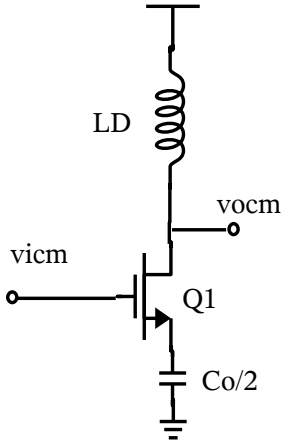
Diff/Common mode negative resistance problem

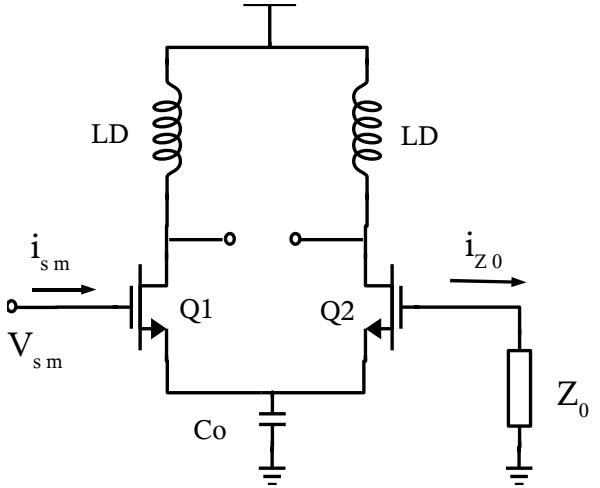
- Capacitively loaded emitter/source -> negative resistance
- Monolithic inductors turn into capacitors beyond SRF
- Current tails are capacitive: negative resistance in common mode
- Cascode bipolar and CMOS circuits are unstable
- Resistive degeneration helps.
- Inductive supply lines

SE, DM, CM input impedance in diff. pair









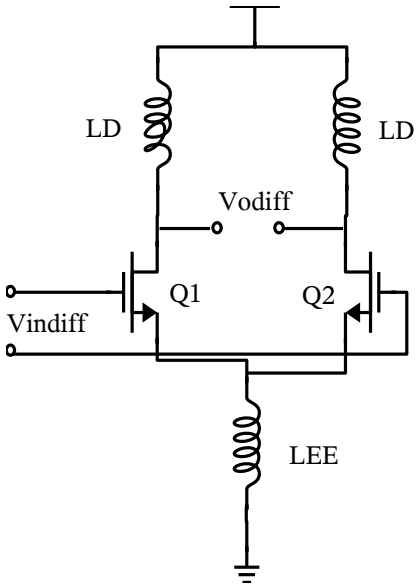
$$Z_{indiff} = 2(R_g + R_s) + \frac{2\omega_{Teff}}{j\omega g_{meff}}$$

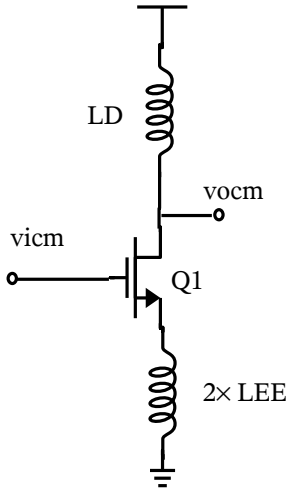
$$z_{ocs} = \frac{r_o}{1 + j\omega r_o C_o}$$

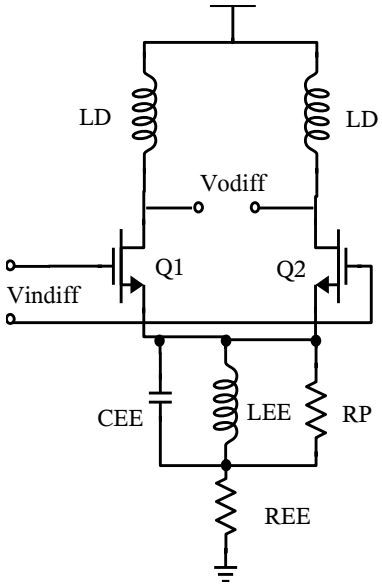
$$Z_{incm} = \frac{v_{icm}}{2 i_{icm}} = \frac{R_g + R_s}{2} - \frac{\omega_{Teff}}{\omega^2 C_o} + \frac{1}{j\omega C_o} + \frac{\omega_{Teff}}{2 j\omega g_{meff}}$$

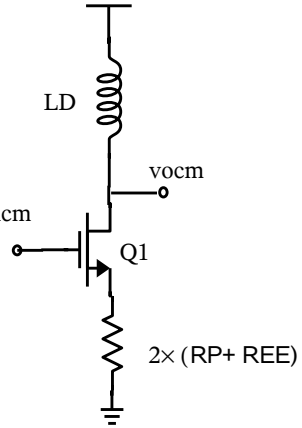
$$Z_{ism} = \frac{V_{ism}}{i_{ism}} = \left(R_g + R_s + \frac{\omega_{Teff}}{j\omega g_{meff}}\right) + \frac{\left(R_s + R_g + Z_0 + \frac{\omega_{Teff}}{j\omega g_{meff}}\right)\left(1 + \frac{\omega_{Teff}}{j\omega}\right)}{1 + \frac{R_s + R_g + Z_0}{z_{ocs}} + \frac{\omega_{Teff}}{j\omega}\left(1 + \frac{1}{g_{meff} z_{ocs}}\right)} \rightarrow Z_{ism} = \left(R_g + R_s + \frac{\omega_{Teff}}{j\omega g_{meff}}\right)$$

Techniques to improve CMR at HF

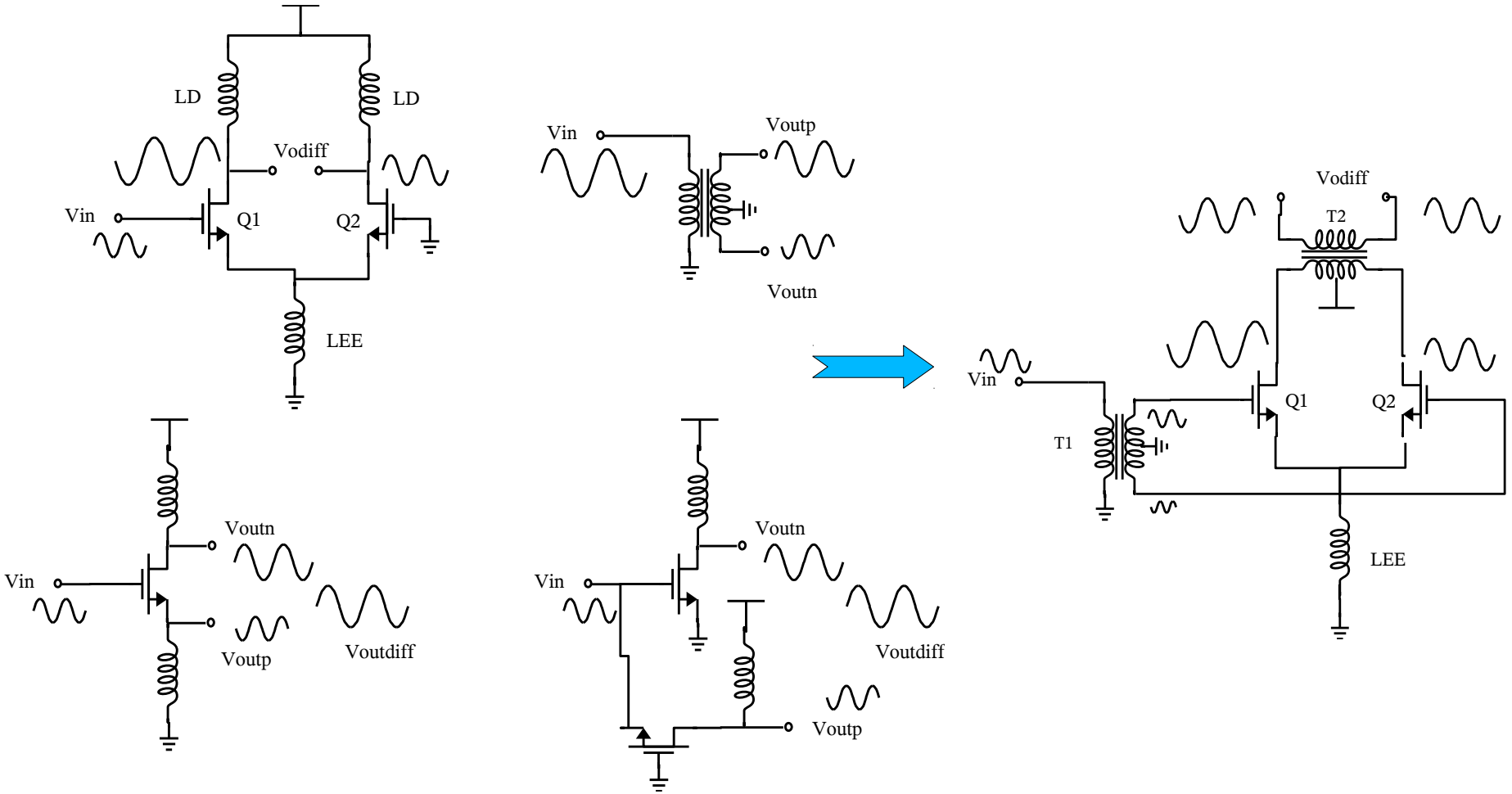








CM leakage at HF and solutions



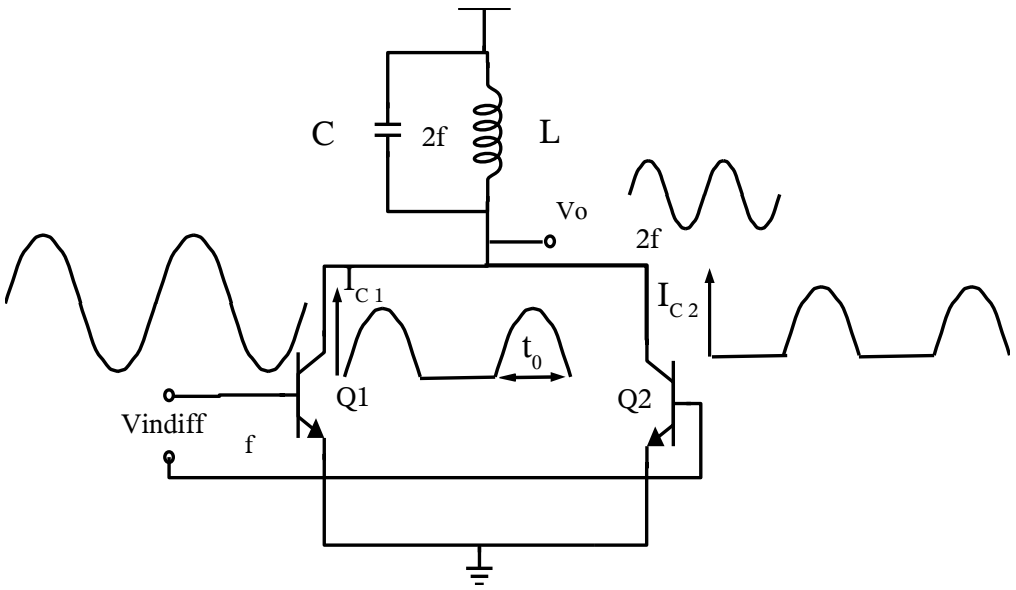
Non-linear techniques

- Most important HF circuits operate at large signal:
  - PA,
  - multiplier,
  - Mixer,
  - Oscillator
- Harmonic Fourier series analysis is employed to analyze such circuits.

$$I_C(t) = I_0 + I_1\cos(\omega t) + I_2\cos(2\omega t) + \ldots + I_n\cos(n\omega t)$$

Multipliers

- Important in synthesizers and signal sources >100 GHz
- I_{MAX} = maximum collector/drain current of transistor
- T = period of fundamental signal at input
- t_o<T/2 is duration of current pulse => class AB to B
- Optimal t_0 depends on harmonic order



$$I_n = I_{MAX}\frac{4t_0}{\pi T}\left|\frac{\cos\left(n\pi\frac{t_0}{T}\right)}{1-\left(2n\frac{t_0}{T}\right)^2}\right|$$

$$P_{out} = I_n\frac{V_{MAX}-V_{MIN}}{2} \le I_n\frac{V_B}{2}$$

Design equations

$$R_{LOPT} = \frac{V_{MAX} - V_{MIN}}{2I_n} \approx \frac{V_{DD}}{I_n}$$

$$P_{out} = I_n \frac{V_{MAX} - V_{MIN}}{2} \leq I_n \frac{V_B}{2}$$

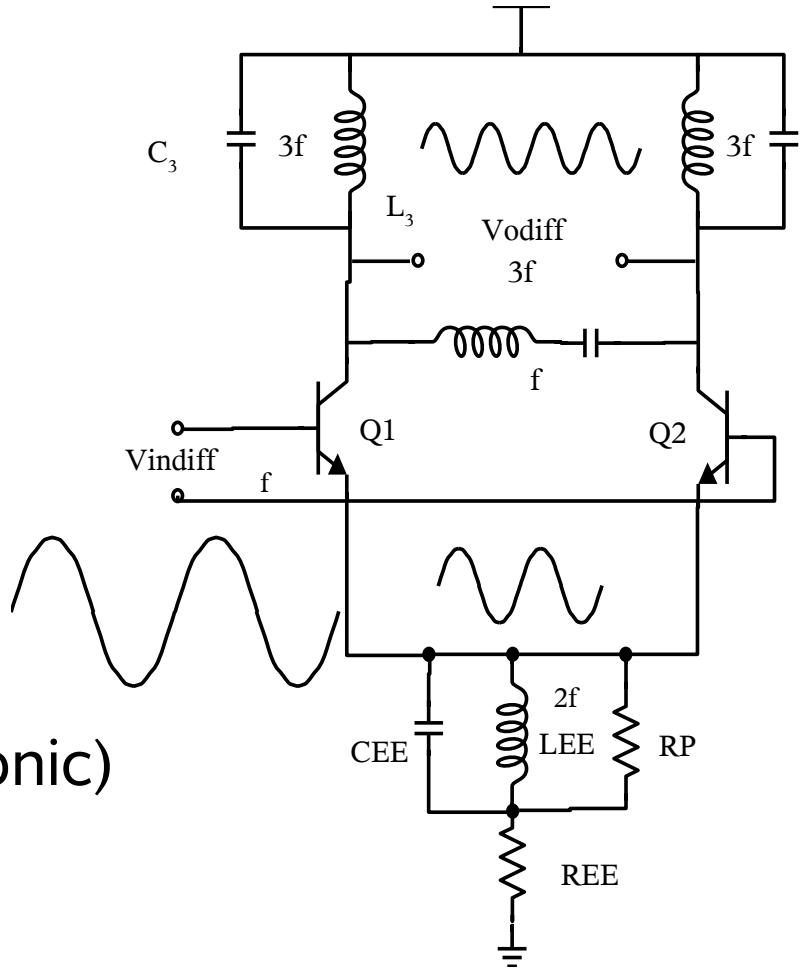
$$I_0 = I_{MAX} \frac{2t_0}{\pi T}$$

$$P_{DC} = 2 I_0 V_{DD} = \frac{4 t_0}{\pi T} I_{MAX} V_{DD}$$

$$\eta_{DC} = \frac{P_L}{P_{DC}} \leq \frac{I_n}{2I_0} = \left| \frac{\cos\left(n\pi \frac{t_0}{T}\right)}{1 - \left(2n \frac{t_0}{T}\right)^2} \right|$$

Tripler

$$V_{odiff}(3\omega) = -2R_{P3} I_{MAX} \frac{4t_0}{\pi T} \left| \frac{\cos\left(3\pi \frac{t_0}{T}\right)}{1-\left(6\frac{t_0}{T}\right)^2} \right|$$



R_{P3} (output impedance at 3rd harmonic) should be equal to R_{LOPT}

Summary

- HF circuit topologies feature L, xfmr, t-lines
- Impedance matching critical at HF
- Tuned HF circuits can be analyzed using “downconversion” and applying traditional LF amplifier analysis
- Broadbanding techniques involve special topologies, feedback, scaling, inductive peaking
- Differential and common-mode stability analysis critical in successful HF ICs
- Nonlinear circuits are analyzed using Fourier series