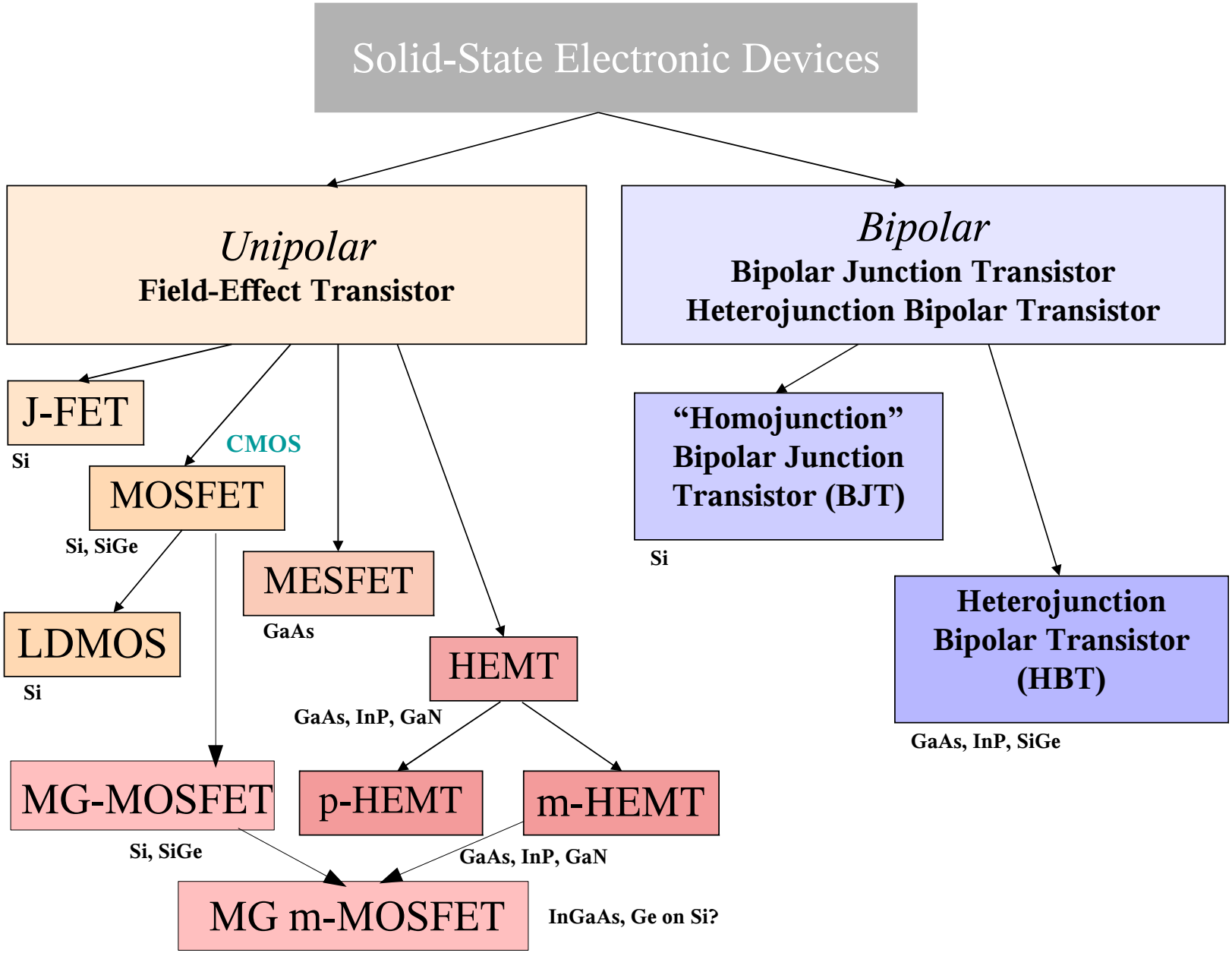
4. HF transistors

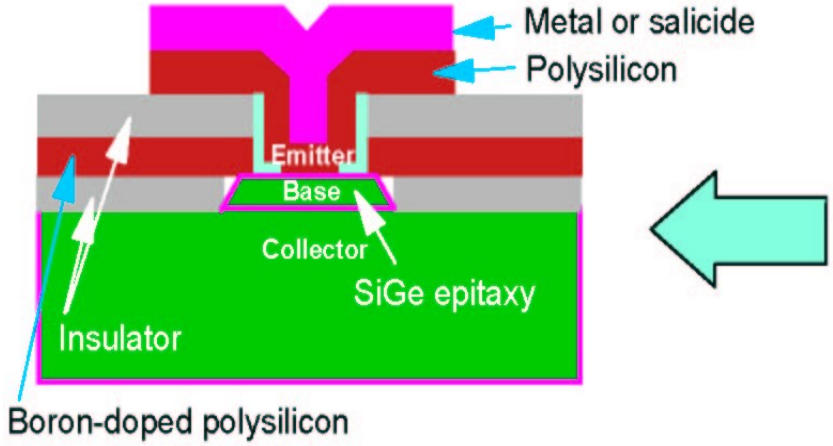
Outline

- Microwave and mm-wave transistors
- High-frequency figures of merit
- MOSFET structure & HF equivalent ckt.
- SiGe HBT structure & HF equivalent ckt.
- FETs vs. Bipolars

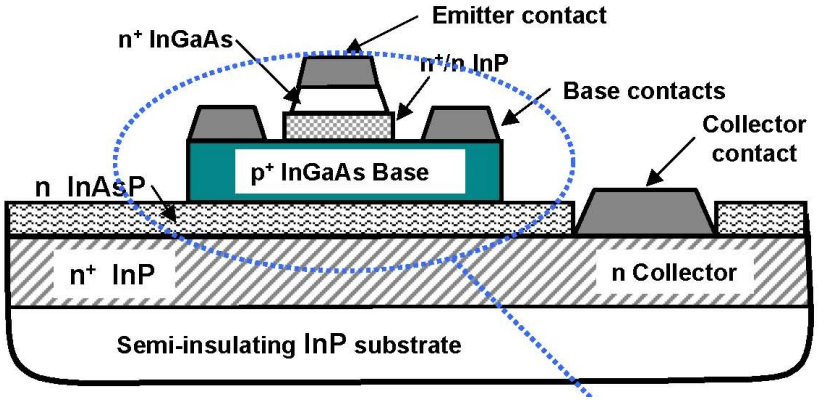

Solid-State Electronic Devices
Unipolar
Field-Effect Transistor
Bipolar
Bipolar Junction Transistor
Heterojunction Bipolar Transistor
J-FET
Si
CMOS
MOSFET
Si, SiGe
MESFET
GaAs
LDMOS
Si
HEMT
GaAs, InP, GaN
MG-MOSFET
Si, SiGe
p-HEMT
m-HEMT
GaAs, InP, GaN
MG m-MOSFET
InGaAs, Ge on Si?
"Homojunction" Bipolar Junction Transistor (BJT)
Si
Heterojunction Bipolar Transistor (HBT)
GaAs, InP, SiGe

μ-wave & mm-wave transistors

- SiGe HBT

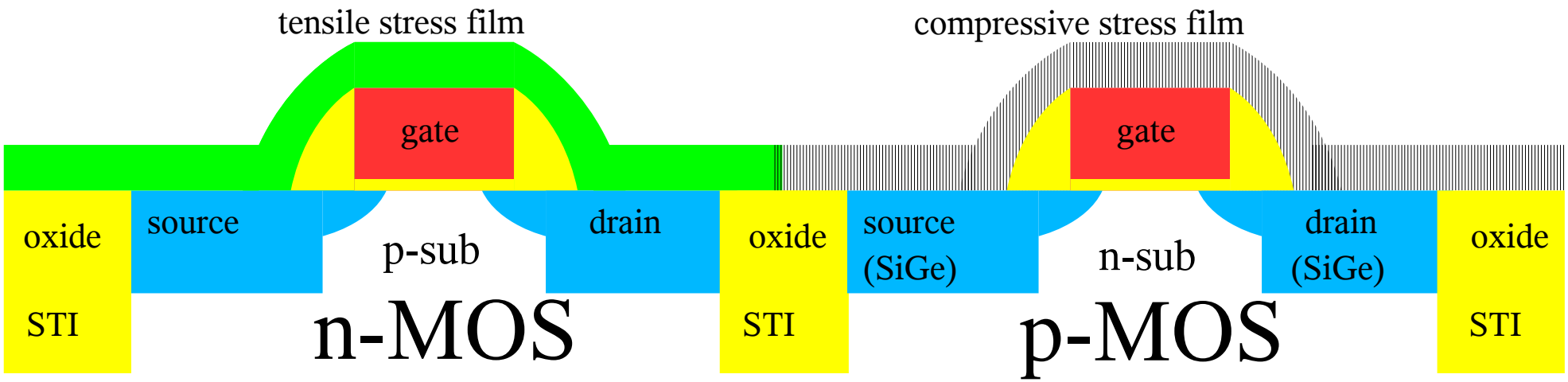


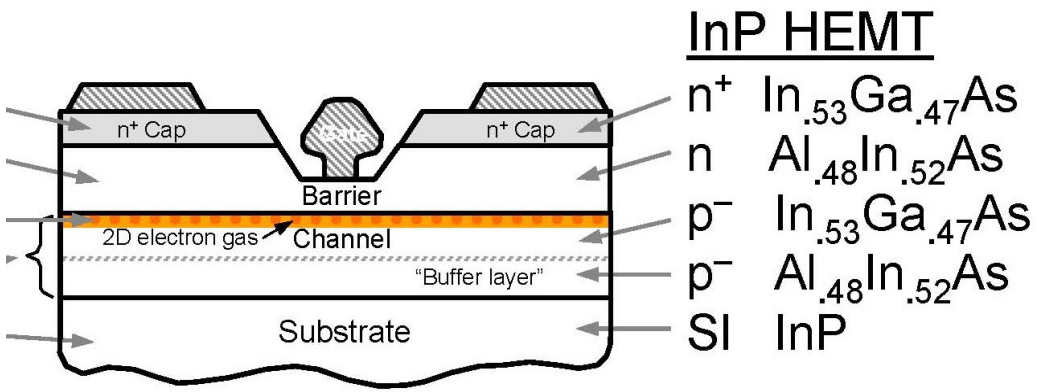
- InP (GaAs) HBT



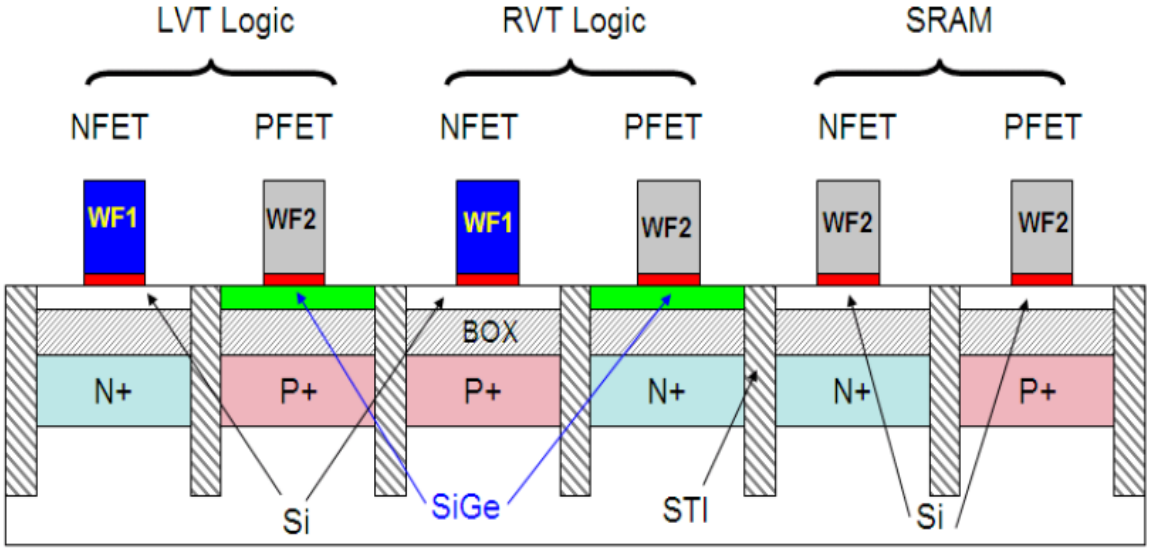
μ-wave & mm-wave transistors

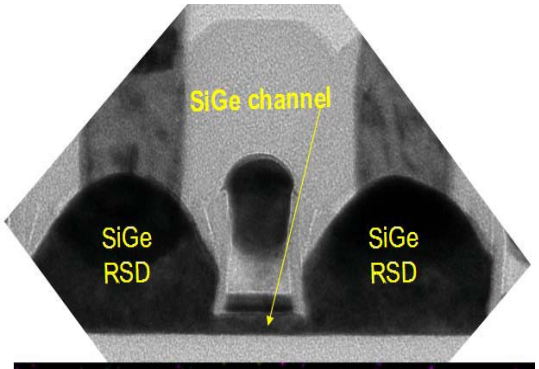
- Si MOSFET





22-nm ETSOI IBM/ST/LETI/GF/SOITEC





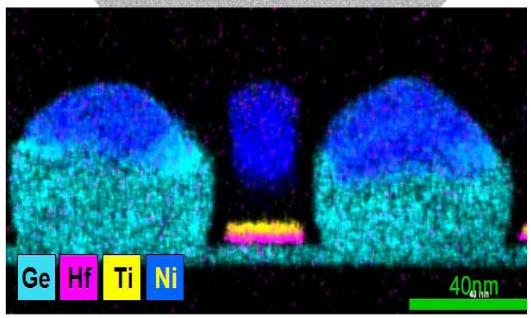


Fig. 18 Schematic showing integration of SiGe channel in conjunction with back gating and HK/MG to achieve multi-V_t in ETSOI. SiGe PFET is used in high performance logic to boost device performance while Si PFET is used in SRAM to achieve low leakage. All devices have undoped channels to eliminate random doping fluctuation and to reduce device va

K. Cheng et al. Paper 18.1, IEDM 2012

S. Narasimha et al. Paper 3.3, IEDM 2012

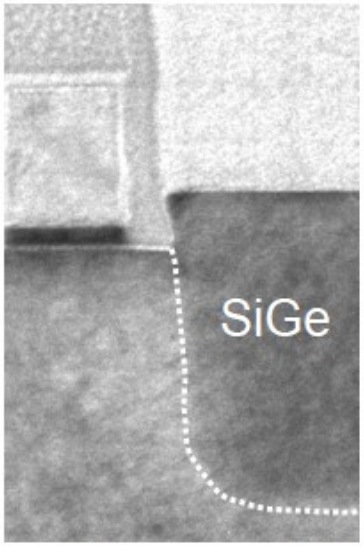


Fig 10. Cross-section of PFET showing embedded SiGe Source/Drain Stressor.

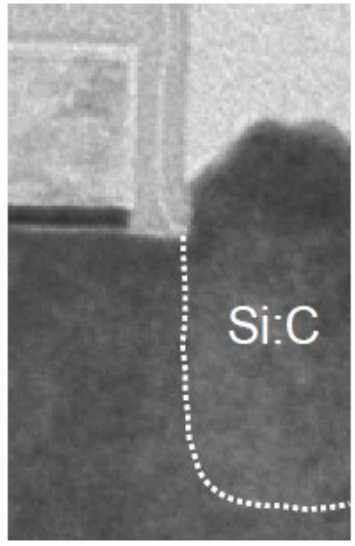


Fig 11. Cross-section of NFET showing embedded Si:C Source/Drain Stressor.

Intel 22-nm FinFET

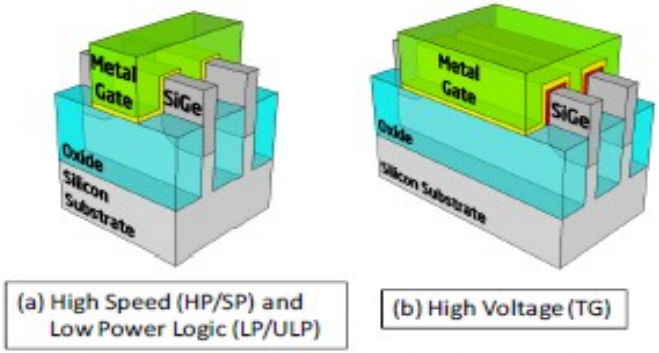


Fig. 1. 22 nm SoC Tri-Gate transistor families, including high speed logic (HP/SP), low power logic (LP/ULP) and high voltage (TG)

Fin not thin enough for fully depleted
Fin had to be doped=> bad for speed

C.-H. Jan et al.
Paper 3.1, IEDM 2012

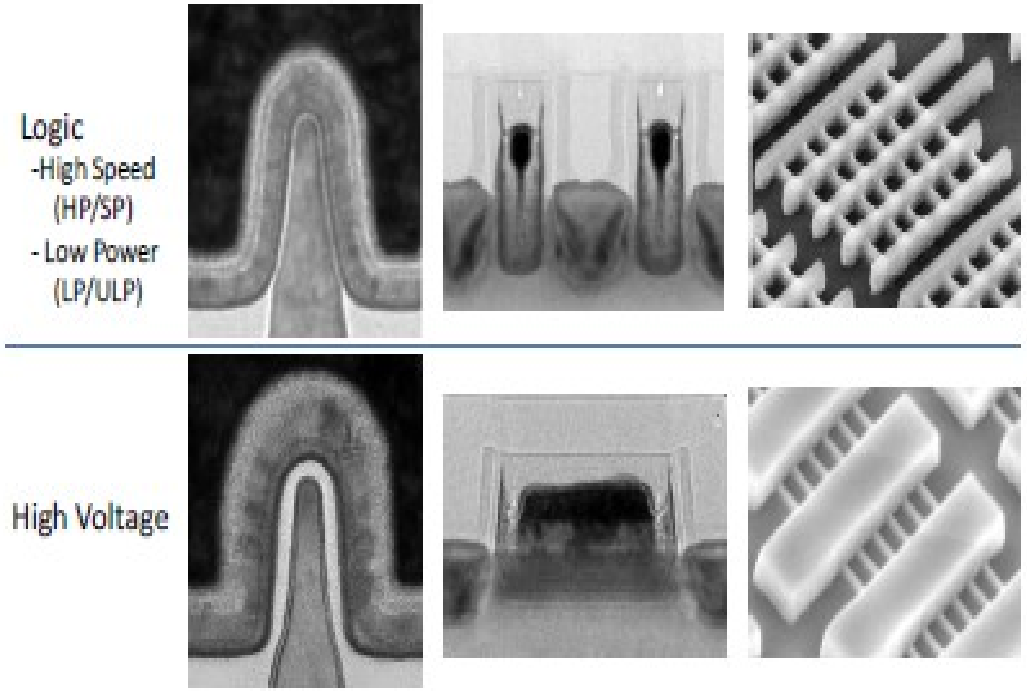


Fig. 2. Fin cut TEM, gate cut TEM, and tilted SEM of logic thin gate (top) and high-voltage thick-gate (bottom) transistors

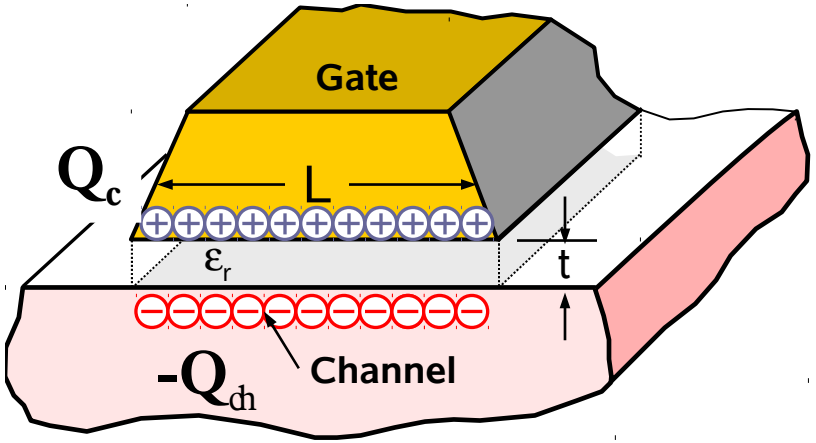
What drives device performance?

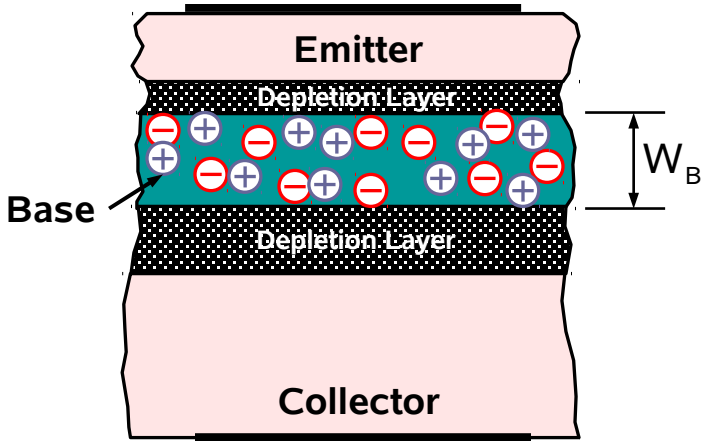
- Material properties
  - electron mobility (InP > SiGe > Si)
  - hole mobility (SiGe > Si > InP)
  - saturation velocity (InP > Si/SiGe)
  - breakdown field (InP > Si)
  - thermal conductivity (Si > SiGe > InP)
- Lithography (Si > InP)
- Yield & reliability (MOS > SiGe HBT > InP HBT)

FET vs. HBT

- Unipolar: electrons or holes
- Intrinsic device speed is laterally defined by L
- lithography driven.

- Bipolar: electrons & holes
- intrinsic device speed is vertically defined by W_B
- atomic layer growth driven





- In both cases, real device speed is affected by 3-D parasitics.
- Scaling in 2D and 3D is important.

MOSFET vs. HEMT

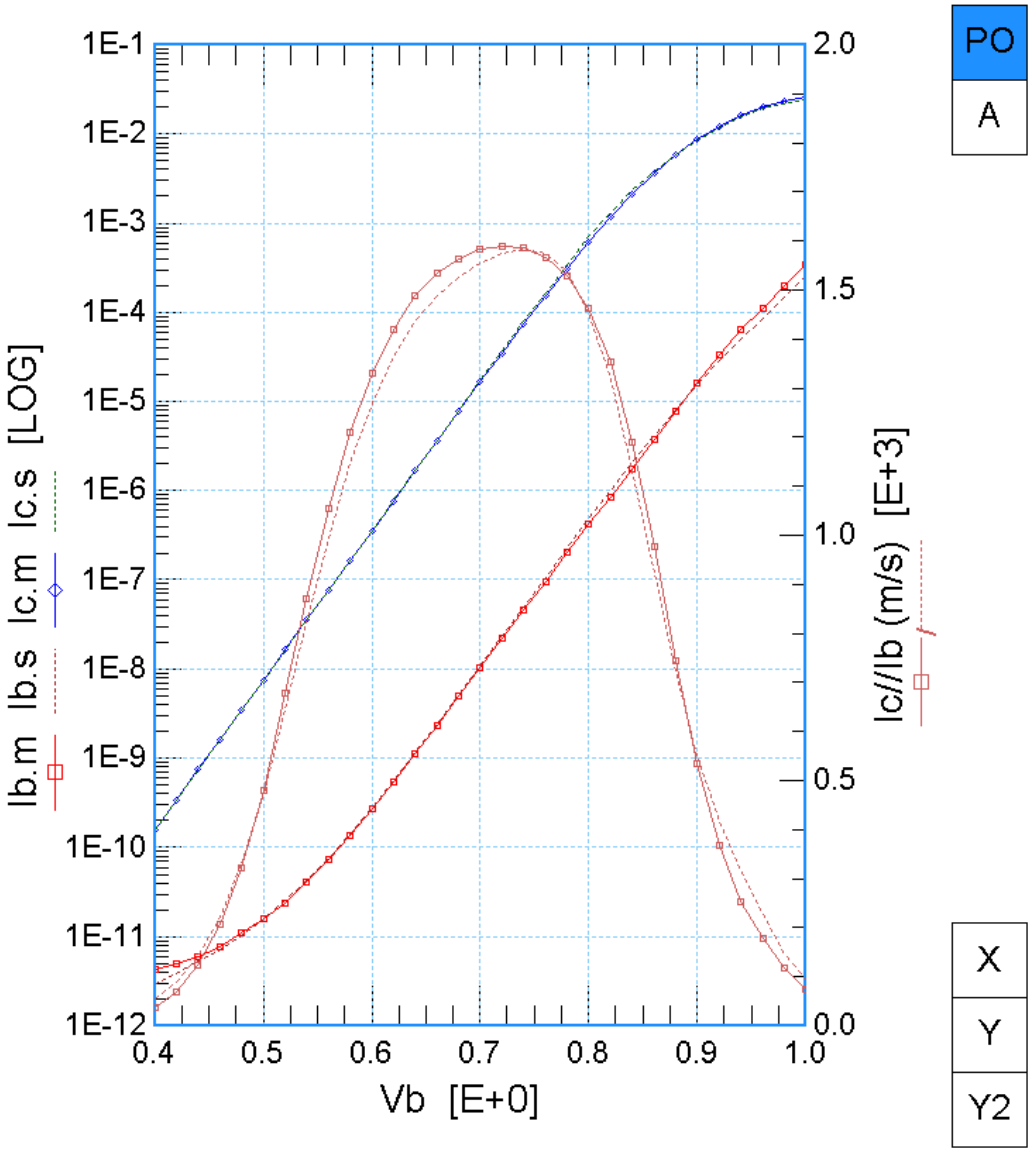
- Mostly on silicon
- MOS insulator gate
- No gate current *
- Inversion channel
- Both p-type and n-type
- Substrate node must be biased

- III-V and Si, SiGe
- Schottky gate
- Gate current (small)
- Accumulation channel
- Mostly n-type
- Substrate node not biased, connected to ground (as in SOI MOSFETs)

- The same DC I-V characteristics and small-signal equivalent circuit

$$Q_n = C_{gate} W \left(V_{GS} - V_T \right); \quad I_{DS} = Q_n v_n(E)$$

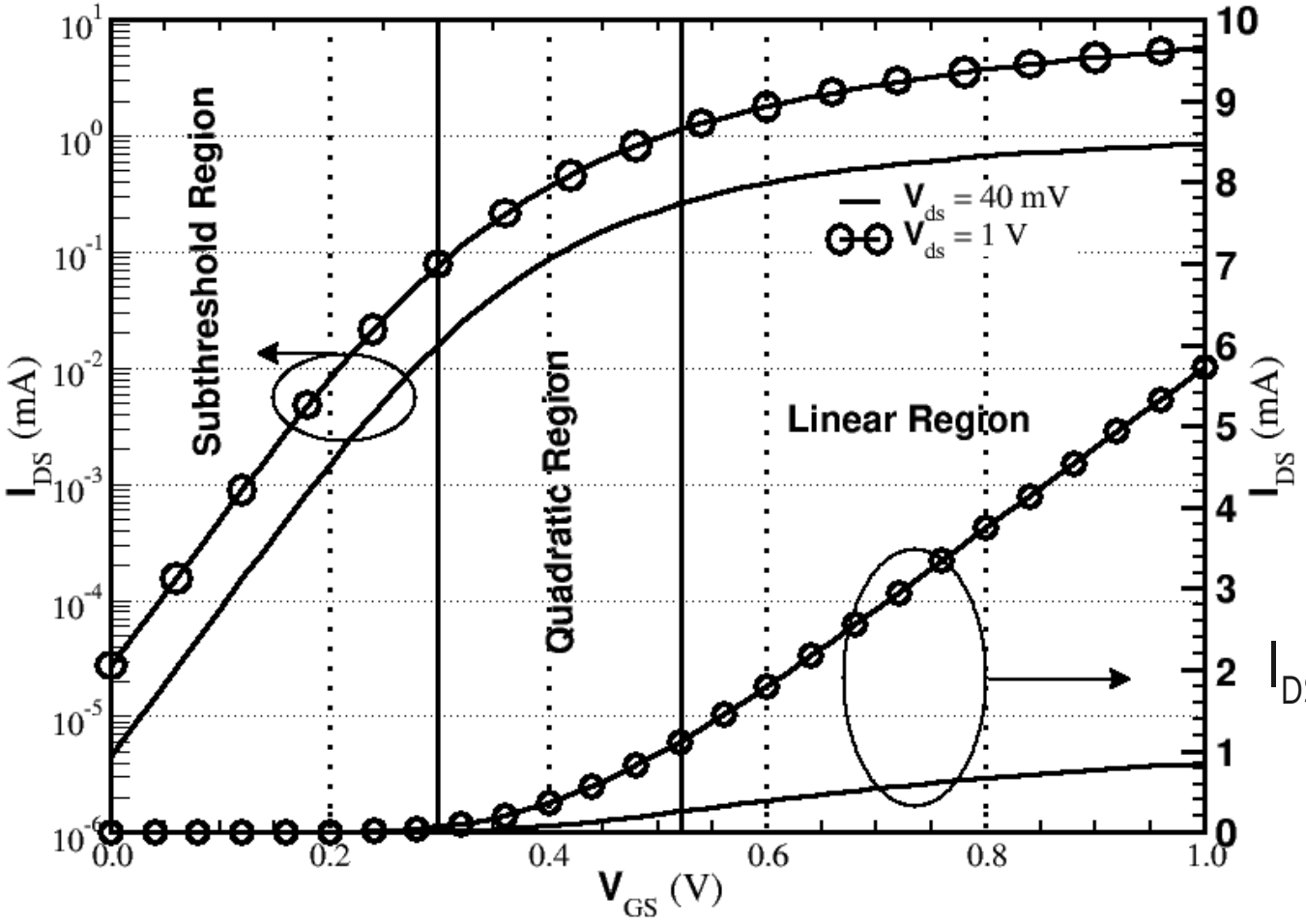
Typical Forward HBT Gummel Plot



$$I_C = J_S A_E \exp\left(\frac{V_{BE}}{VT}\right)\left(1 + \frac{V_{CE}}{V_A}\right)$$

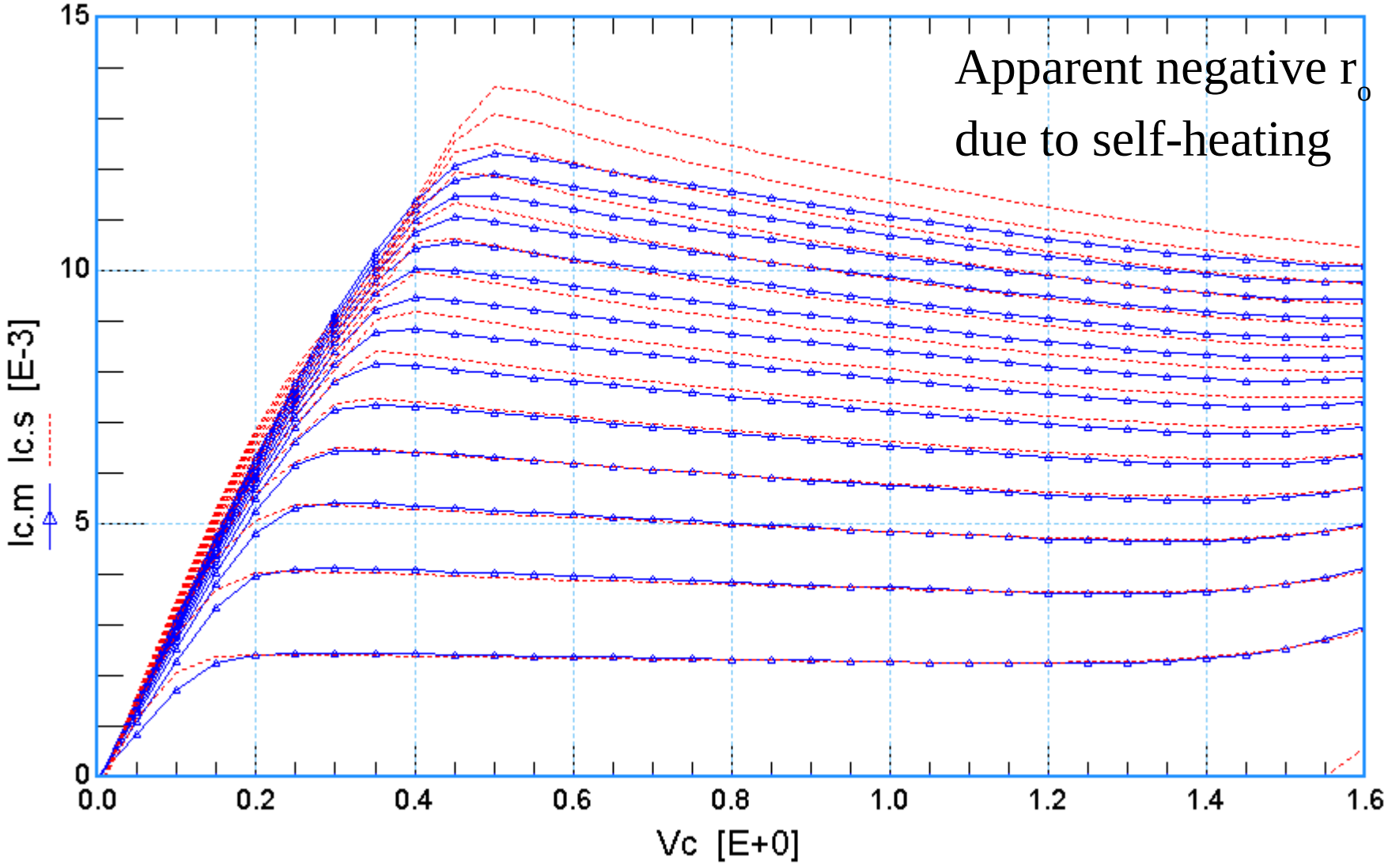
Transfer characteristics in 90-nm n-MOS

- Square-law in sub 130-nm MOSFETs invalid for most bias range



$$I_{DS} = k'_n (L) W \left(V_{GS} - V_T \right)$$

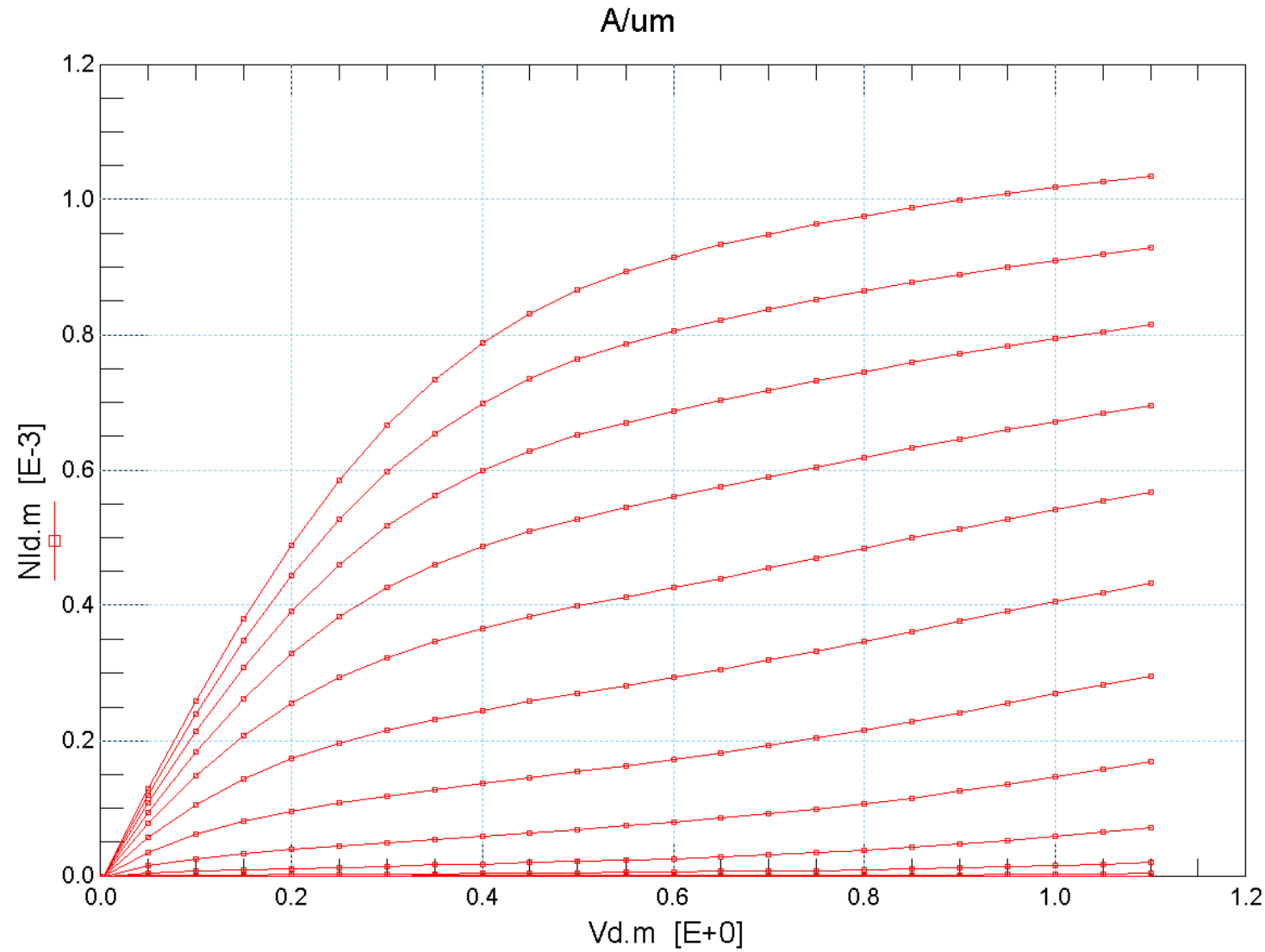
Typical HBT output characteristics



PO
A
E

X
Y

45-nm SOI MOSFET output characteristics



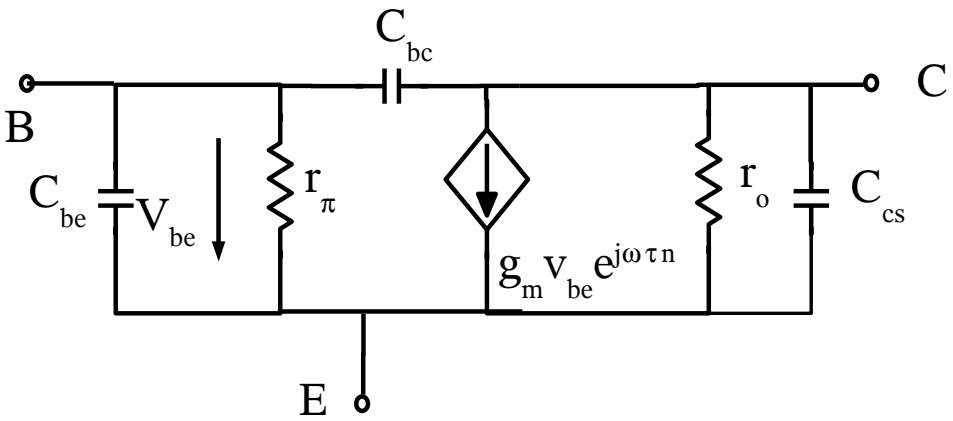
Plot IBM_45nm_SOI_40x0p77_SS_nmos/dc/output/output

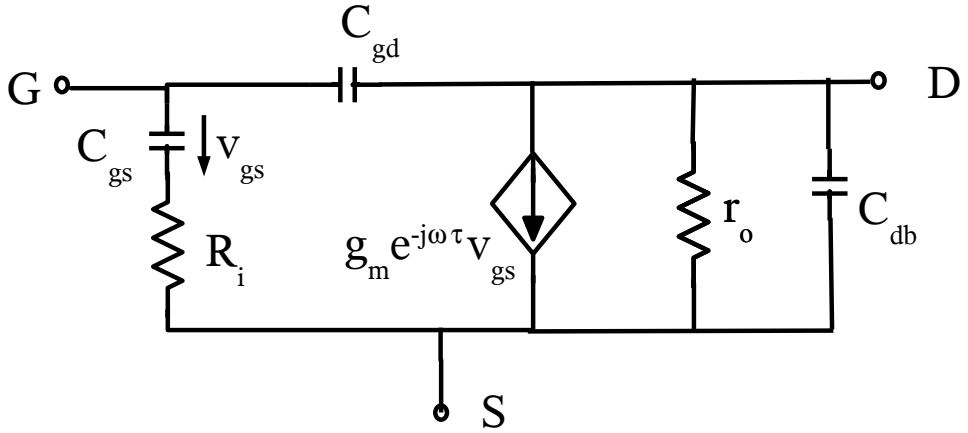
DC Characteristics
FET vs. HBT

- Transfer Characteristics:
  - Exponential in subth.
  - Square-law or linear in saturation region
  - Low turn-on voltage: 0.5 to 0.2 V
- Output Characteristics
  - Small V_A (r_o)
  - Low breakdown

- Transfer Characteristics:
  - Exponential
  - High turn-on voltage: 0.7 to 0.9 V
- Output Characteristics
  - Large V_A (r_o)
  - Moderate breakdown

HF equiv. circuit and y-matrix of intrinsic CE/CS transistor





$$\left[\frac{y}{W}\right]=\begin{bmatrix} j\omega(C'_{gs}+C'_{gd}) & -j\omega C'_{gd} \\ g'_m-j\omega C'_{gd} & g'_o+j\omega(C'_{db}+C'_{gd}) \end{bmatrix};\ [y]=\begin{bmatrix} g_\pi+j\omega(C_{be}+C_{bc}) & -j\omega C_{bc} \\ g_m-j\omega C_{bc} & g_o+j\omega(C_{cs}+C_{bc}) \end{bmatrix}$$

- Input admittance and voltage gain for 2-port loaded by admittance Y_L

$$Y_{IN}=Y_{11}-\frac{Y_{12}Y_{21}}{Y_L+Y_{22}} \text{ and } G_v=\frac{-Y_{21}}{Y_L+Y_{22}}$$

Common base/gate and cascode

- FET/HBT in CG/CB

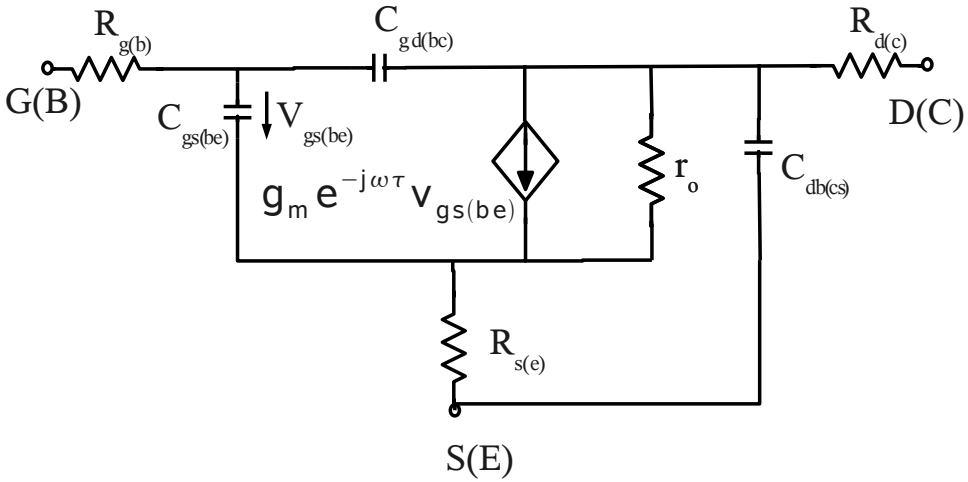
$$\left[\frac{y}{W}\right]=\begin{bmatrix} g'_m+g'_o+j\omega(C'_{gs}+C'_{sb}) & -g'_o \\ -g'_m-g'_o & g'_o+j\omega(C'_{db}+C'_{gd}) \end{bmatrix};$$

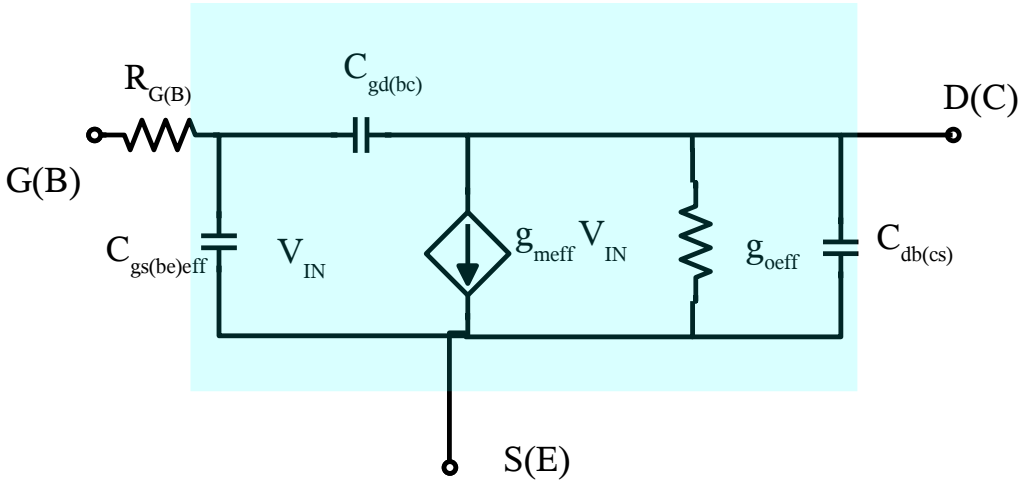
$$[y]=\begin{bmatrix} g_m+g_o+g_\pi+j\omega C_{be} & -g_o \\ -g_m-g_o & g_o+j\omega(C_{cs}+C_{bc}) \end{bmatrix}$$

- FET/HBT in cascode topology

$$Y_{IN}=Y_{11,CS}-\frac{Y_{12,CS}Y_{21,CS}}{Y_{22,CS}+Y_{11,CG}-\frac{Y_{12,CG}Y_{21,CG}}{Y_L+Y_{22,CG}}} \qquad G_v(casc)=\frac{-Y_{21,CS}}{Y_{12,CG}-\left[\frac{Y_{11,CG}+Y_{22,CS}}{Y_{21,CG}}\right][Y_L+Y_{22,CG}]}$$

CE/CS HF circuit useful for hand analysis



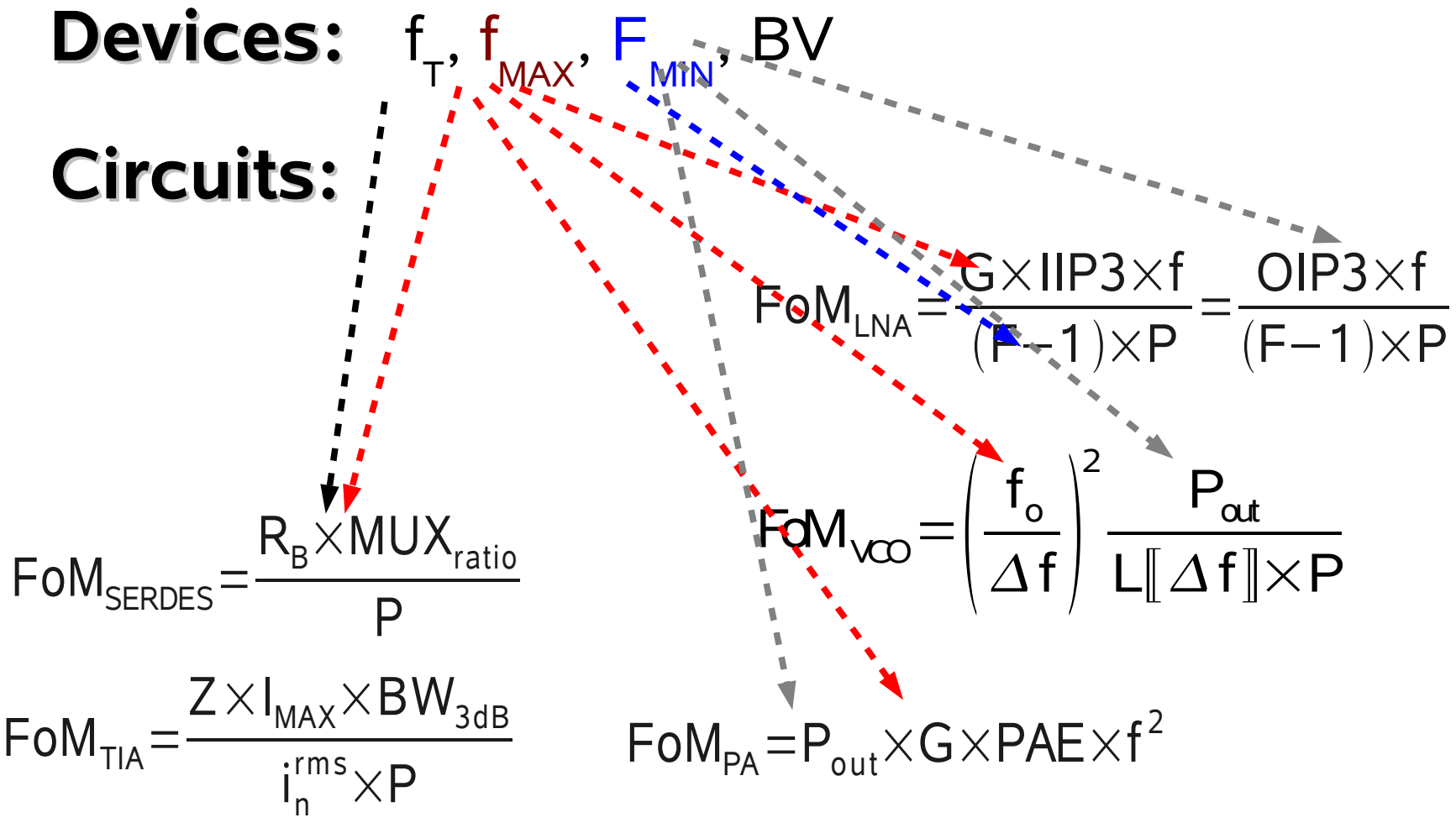


- Impact of $R_s(r_E)$ included in $R_{G(b)}$, g_m, f_T and $C_{gs}/C_{b\,e}$
- $R_G = R_g + R_s$ (can be used directly in $Z_{i\,\backslash n}$, NF_{MIN}, Z_{sopt})
- $Z_{in} = R_g + R_s - jf_T/(fg_{meff})$

Outline

- Microwave and mm-wave transistors
- High-frequency figures of merit

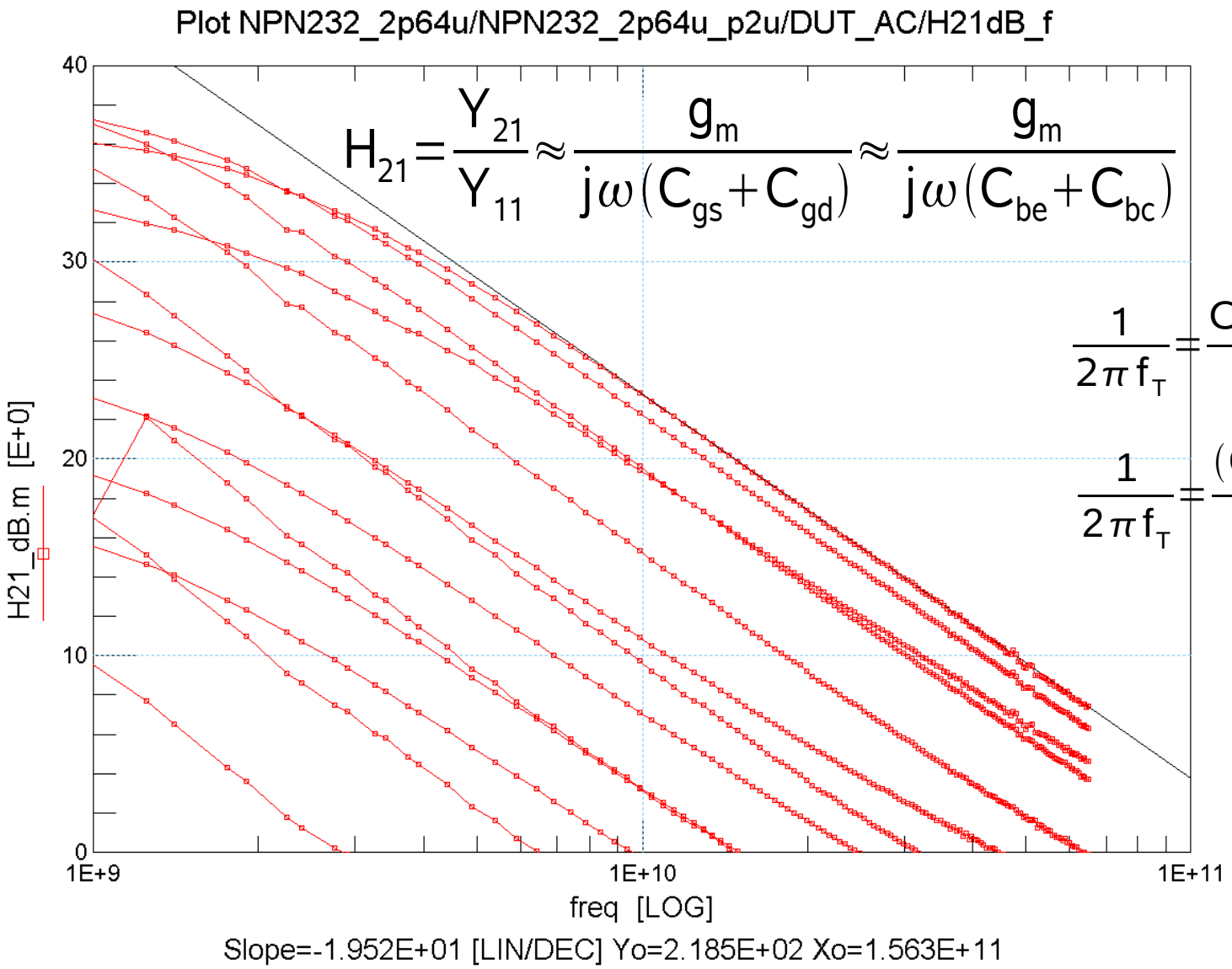
Figures of Merit (FoMs) for HF & High-Speed ICs



Device Figures of Merit

- Cutoff frequency definition
- Maximum oscillation frequency definition
- Minimum noise figure and noise parameters
- Intrinsic slew rate

f_T definition: $20*\log_{10}|H_{21}(f=f_T)| = 0$



$$H_{21} = \frac{Y_{21}}{Y_{11}} \approx \frac{g_m}{j\omega(C_{gs}+C_{gd})} \approx \frac{g_m}{j\omega(C_{be}+C_{bc})}$$

$$H_{21} = \frac{Y_{21}}{Y_{11}} \approx \frac{\omega_T}{j\omega}$$

$$\frac{1}{2\pi f_T} = \frac{C_{gs}+C_{gd}}{g_m} + C_{gd}(R_s+R_d)$$

$$\frac{1}{2\pi f_T} = \frac{(C_{be}+C_{bc})}{g_m} + (r_E+r_C)C_{bc}$$

f_{MAX} definition $MAG_{dB}(f) = 10*\log(MAG) = 0dB$

- f_{MAX} is defined as the x-axis intercept of the power gain vs. frequency plot.
- Both MAG(f) and U(f) intercept the x-axis at the same point
- $10*\log_{10}U(f)$ has constant slope (approx. 20 dB/decade) and is easier to extrapolate
- Both can be calculated from measured S or Y parameters

U as a function of transistor 2-port params
(Mason, 1953)

$$U = \frac{|y_{21} - y_{12}|^2}{4[\Re(y_{11})\Re(y_{22}) - \Re(y_{12})\Re(y_{21})]}$$

$$U = \frac{|z_{21} - z_{12}|^2}{4[\Re(z_{11})\Re(z_{22}) - \Re(z_{12})\Re(z_{21})]}$$

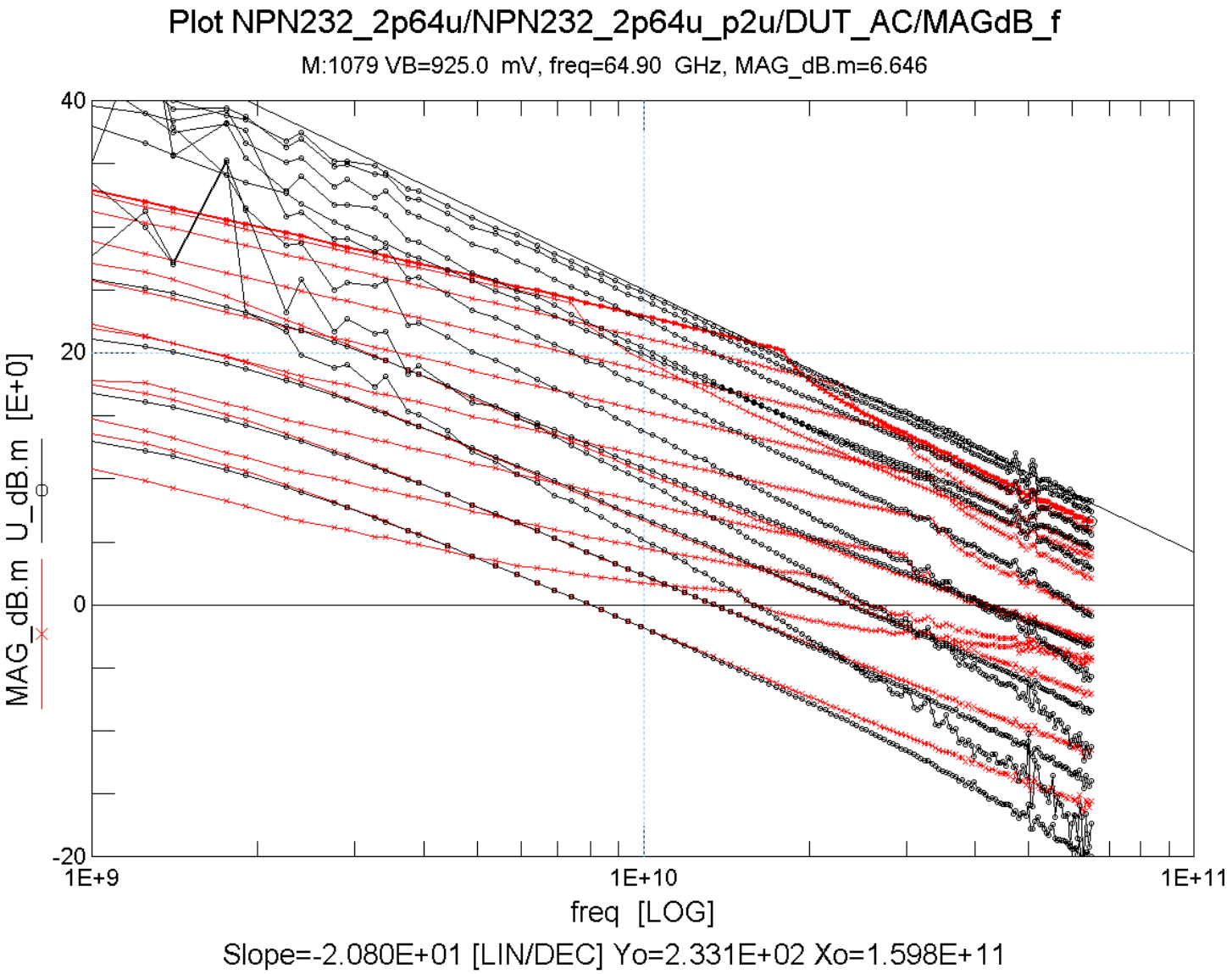
$$MAG = \left|\frac{S_{21}}{S_{12}}\right| \left(k - \sqrt{k^2 - 1}\right)$$

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |D|^2}{2|S_{12}||S_{21}|}$$

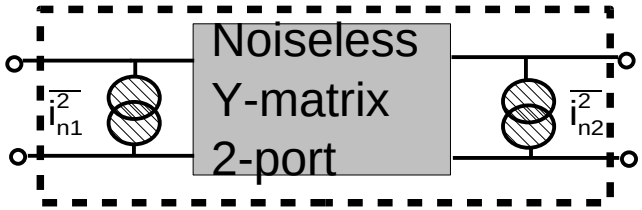
$$D = S_{11} \times S_{22} - S_{21} \times S_{12}$$

- f_{MAX} (unlike f_T) contains information about output impedance

f_{MAX} definition: U vs. MAG (same x-axis intcp.)



Noise params of intrinsic CE/CS transistor



$$R_n = \frac{\langle I_{n2}^2 \rangle}{4kT\Delta f \left|(y_{21})\right|^2}$$

$$G_u = \frac{\langle I_{n1}^2 \rangle}{4kT\Delta f} - \left| \frac{\langle I_{n1} I_{n2}^* \rangle}{4kT\Delta f R_n \left|Y_{21}\right|^2} \right|^2$$

$$G_{sopt} = \sqrt{\frac{G_u}{R_n} + G_{cor}^2}$$

$$Y_{cor} = y_{11} - \frac{\langle I_{n1} I_{n2}^* \rangle}{4kT\Delta f R_n y_{21}^*}$$

$$F_{MIN} = 1 + 2R_n(G_{cor} + G_{sopt})$$

G_u, G_{sopt} decrease with correlation, R_{sopt} increases

F_{MIN} decreases with correlation

Noise parameters of the CG/CB transistor

$$R_n = \frac{\langle I_{n2}^2 \rangle}{4kT\Delta f \left|(y_{21})\right|^2}$$

$$G_u = \frac{\langle I_{n1}^2 \rangle}{4kT\Delta f} - \left| \frac{\langle I_{n1} I_{n2}^* \rangle}{4kT\Delta f R_n \left|Y_{21}\right|^2} \right|^2$$

$$Y_{cor} = y_{21} + y_{11} + \frac{\langle I_{n1} I_{n2}^* \rangle}{4kT\Delta f R_n y_{21}^*}$$

Note: y-matrix is that of CG configuration
imag(Y_{21}+Y_{11}) in CG/CB ≠ imag(Y_{11}) in CS/CE

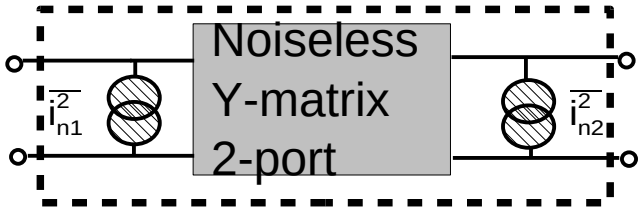
Important ramifications for LNA design

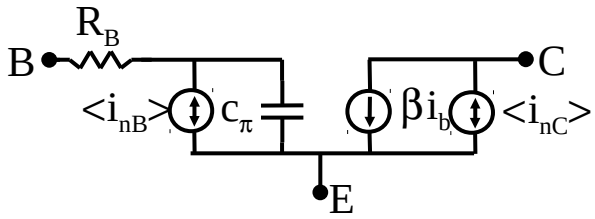
- R_n (CG) = R_n (CS)
- G_u (CG) = G_u (CS)
- G_{cor} (CG) = G_{cor} (CS)

$$F_{MIN} \text{ (CG)} \approx F_{MIN} \text{ (CS)}$$

If correlation is weak, Imag($Y_{cor,} Y_{sopt}$) = Imag (Y_{in}) and can be tuned out simultaneously

Noise equivalent circuit of intrinsic HBT





$$\langle i_{nB} i_{nB}^* \rangle = 2q\Delta f\left(I_B + \left|1 - e^{-j\omega\tau_n}\right|^2 I_C\right)$$

$$\langle i_{nC} i_{nC}^* \rangle = 2q\Delta f I_C$$

$$\langle i_{nB} i_{nC}^* \rangle = 2qI_C\left[\exp(j\omega\tau_n) - 1\right]$$

MESFET (MOSFET) Intrinsic Noise Currents (Pucel 1975)

$$\overline{|I_{nd}^2|} = 4kT\Delta f P g_m + K_f \frac{I_{DS}^{af}}{f}$$

$$\overline{|I_{ng}^2|} = 4kT\Delta f R g_m \frac{f^2}{f_T^2}$$

$$jC = \frac{\overline{I_{ng} I_{nd}^x}}{\sqrt{\overline{|I_{nd}^2|}\,\overline{|I_{ng}^2|}}}$$

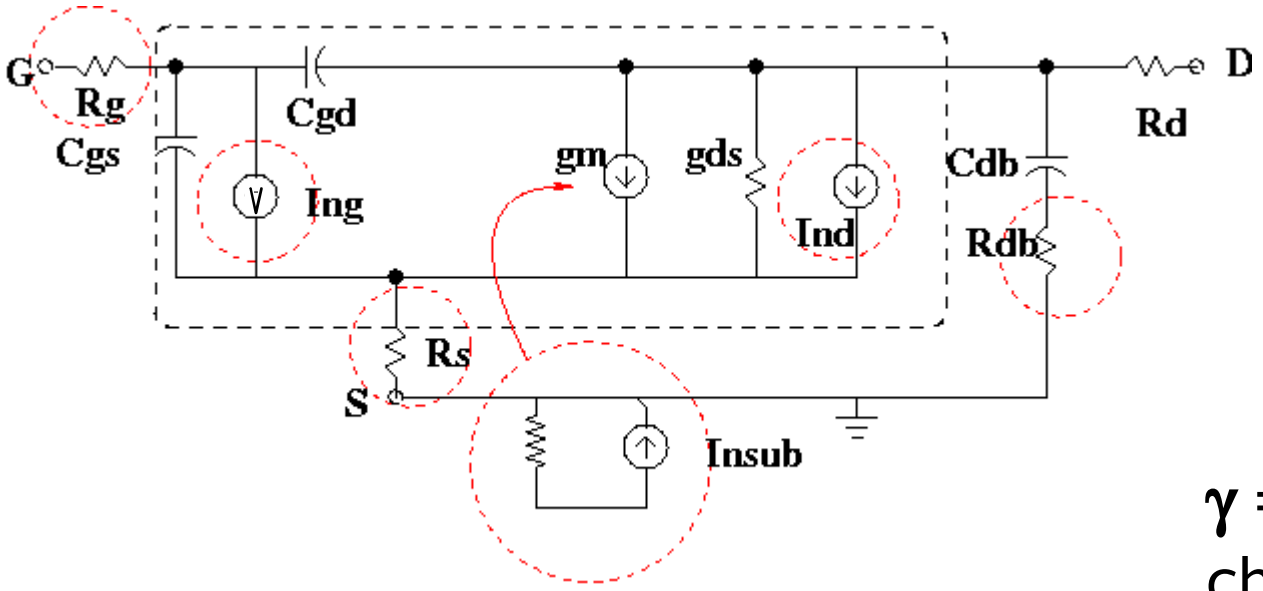
P (γ) = 2/3 (long channel)

R (β) = 4/15 (long channel)

jC = j0.4 (long channel)

Large noise signal model

FET Noise Sources (C. Enz MTT 2002)



$$\overline{|I_{nd}^2|} = 4kT\Delta f \gamma g_m + K_f \frac{g_m^2}{C_{ox} I_g W f^{af}}$$

$$\overline{|I_{ng}^2|} = 4kT\Delta f \beta \frac{(\omega C_{gs})^2}{g_m} \qquad jC = \frac{\overline{I_{ng} I_{nd}^x}}{\sqrt{|I_{nd}^2||I_{ng}^2|}}$$

γ = 2/3 (long channel)

β = 4/15 (long channel)

jC = j0.4 (long channel)

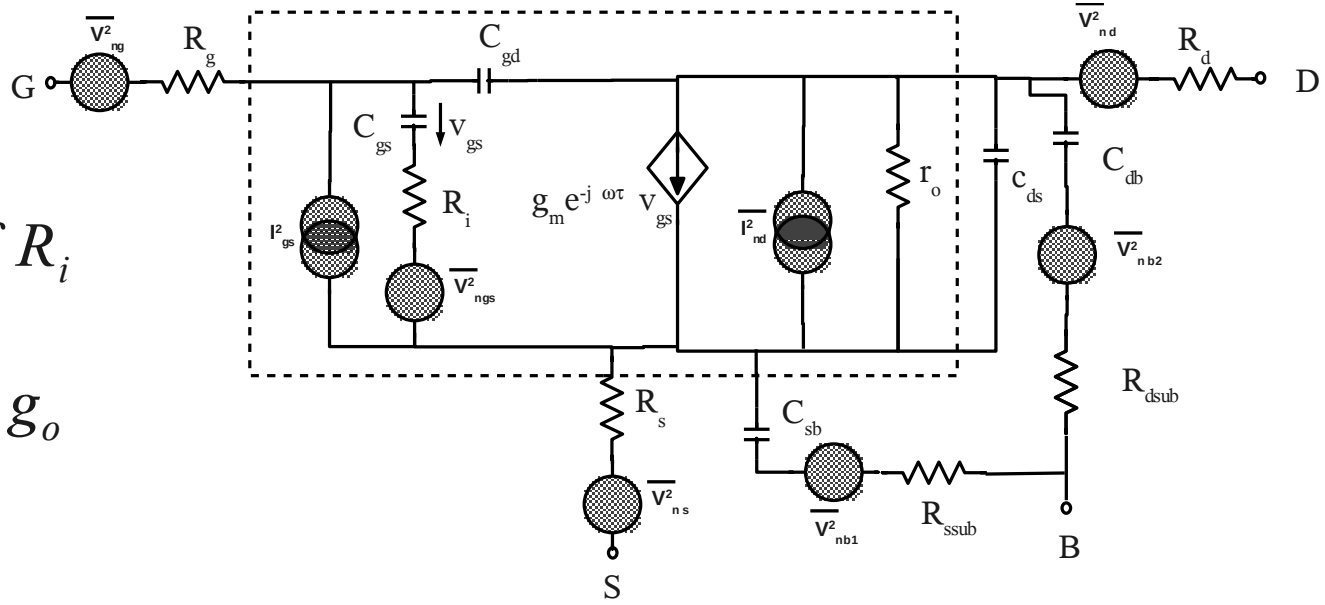
Pospieszalski T-dependent model (1989)

- V_{ng} , $T_{g,}$ at input due to thermal noise from R_i
- $I_{nd,}$ T_d, at output to describe drain current noise
- I_{nd} and V_{ng} are not correlated
- Not large signal model

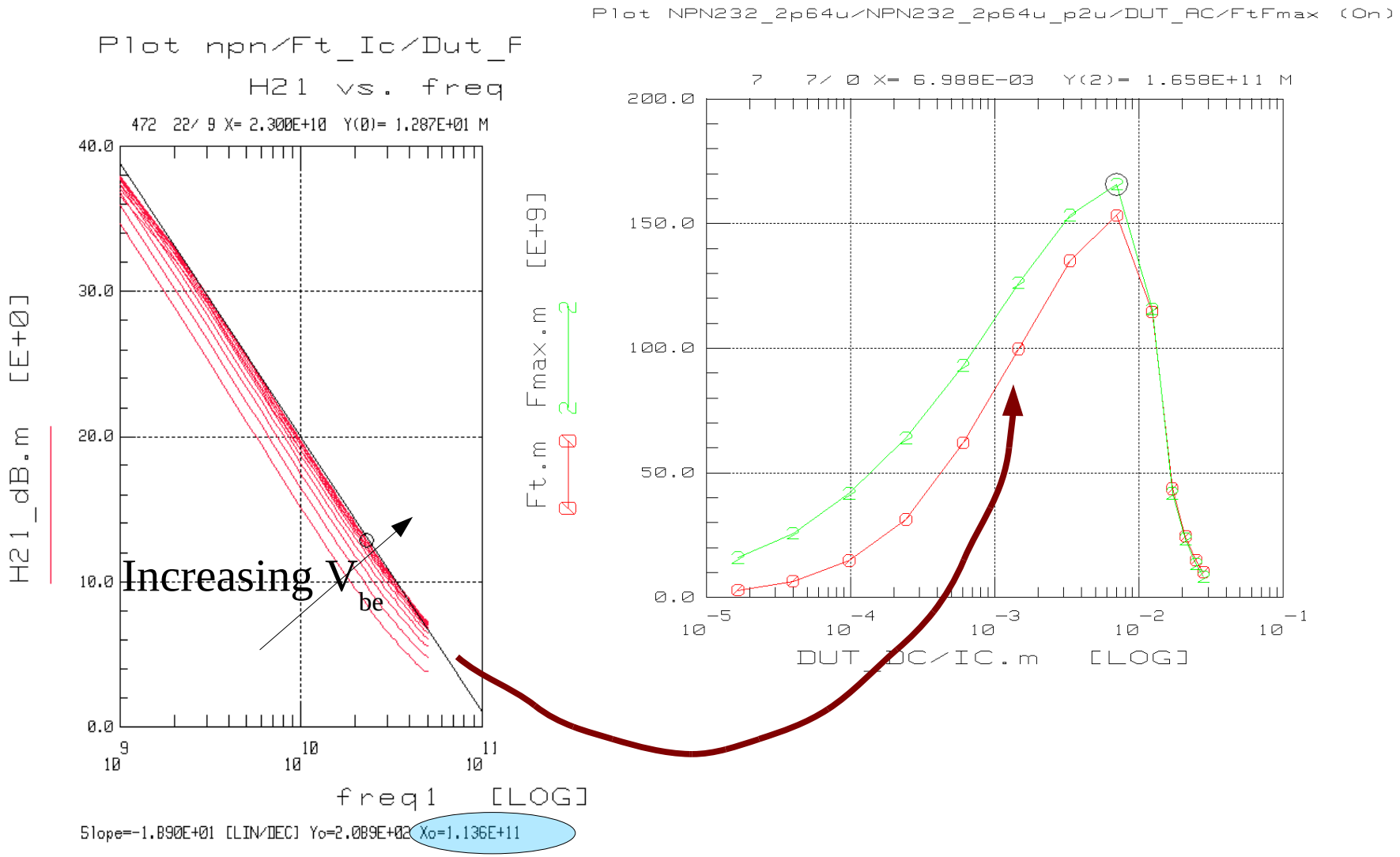
$$\overline{V_{ngs}^2} = 4kT_g \Delta f R_i$$

$$\overline{I_{nd}^2} = 4kT_d \Delta f g_o$$

$$\overline{I_{gs}^2} = 2q \Delta f I_g$$

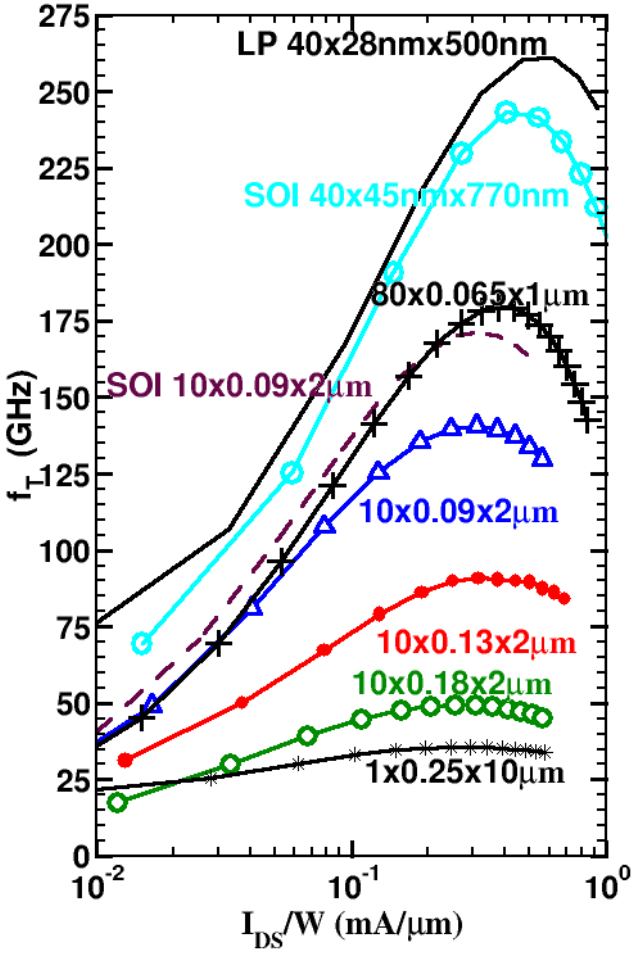


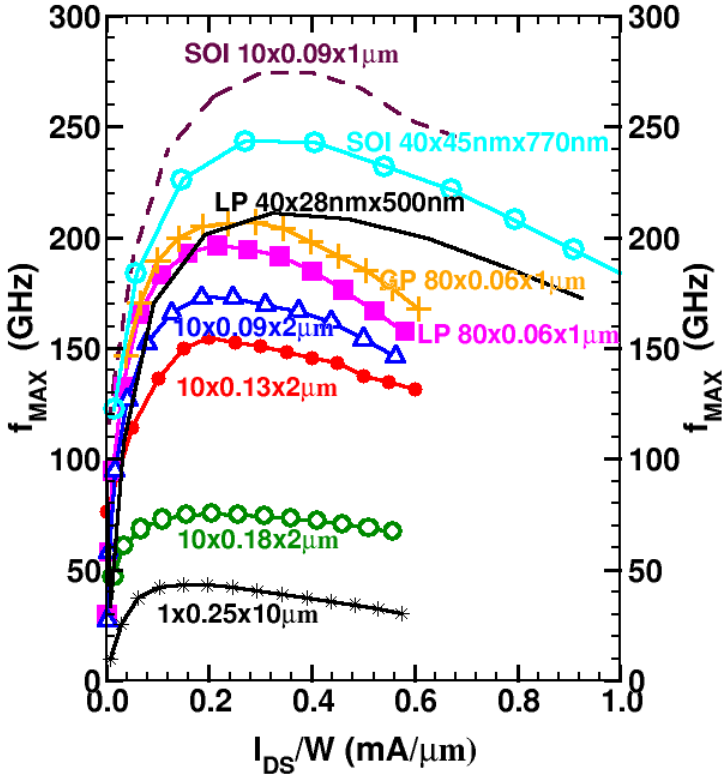
Generating f_T,f_{MAX} and NF_{MIN} vs. $I_{C/D}$ plots

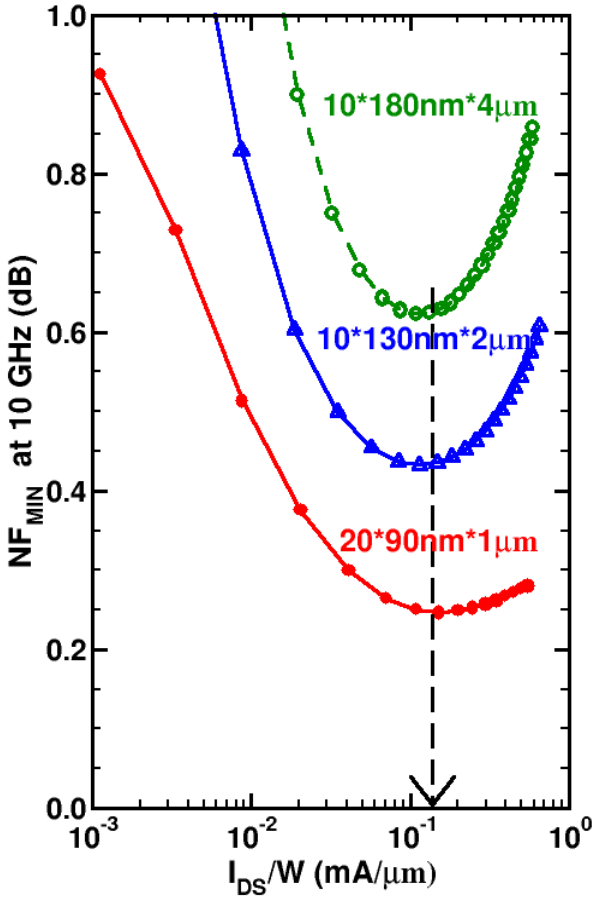


f_T is the intercept: 113 GHz.

n-MOSFET characteristic current densities invariant across nodes and foundries







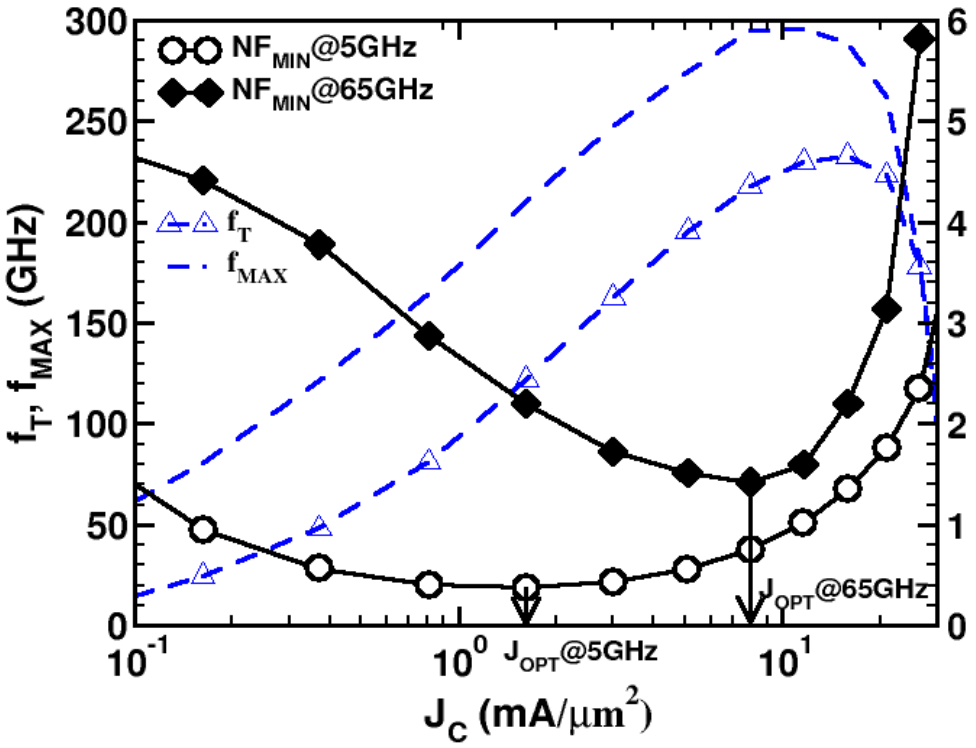
Characteristic current densities (ii)

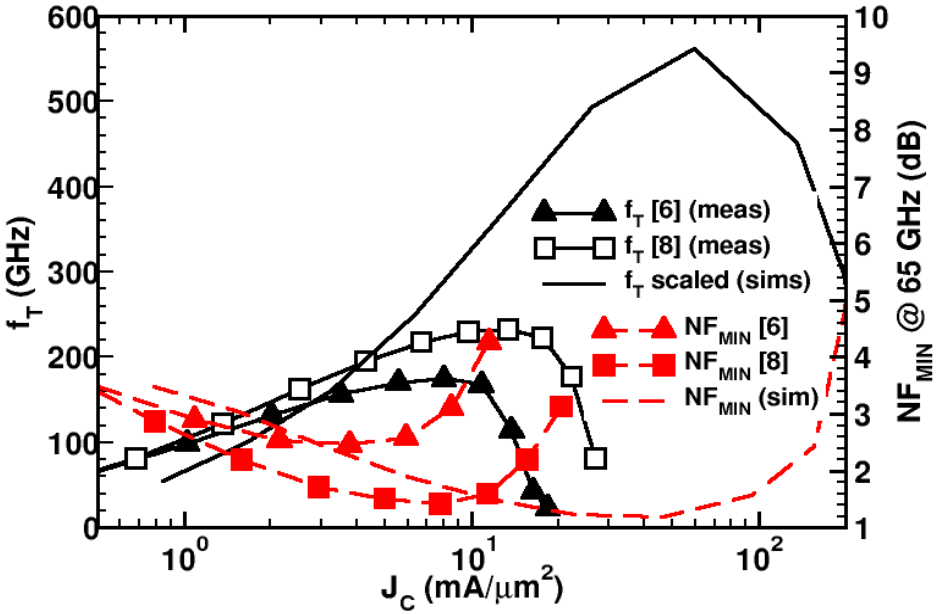
- J_{pfT} = where f_T reaches its max (n-FETs= 0.3-0.4 mA/μm)
- J_{pfMAX}=where f_{MAX} reaches its max (n-FETs= 0.2-0.3 mA/μm)
- J_{OPT}=where NF_{MIN} reaches its min (n-FETs=0.15-0.2 mA/μm)

- **Note:** All characteristic current densities have started to increase at the 45-nm node and beyond because of strain and lack of EOX scaling

Characteristic current densities (iii)

- In HBTs J_{OPT} is a function of frequency
- In HBTs J_{pfT}, J_{pfMAX} and J_{OPT} increase in every new node)





Impact of FET parasitic source/gate resistances

$$g_{me} \approx \frac{g_m}{1 + g_m R_s}$$

$$\frac{1}{2\pi f_T} \approx \frac{(C_{gs} + C_{gd})}{g_m} + (R_s + R_d) C_{gd}$$

- R_s has greater impact than R_g
- R_g is always accompanied by R_s
- Making R_g << R_s is not effective
- k_1 depends on correlation (approx. 0.5)

$$f_{MAX} \approx \frac{f_T}{2\sqrt{(R_i + R_s + R_g) g_o + 2\pi f_T R_g C_{gd}}}$$

$$F_{MIN} \approx 1 + 2 k_1 \frac{f}{f_T} \sqrt{g_m (R_s + R_g) + 1}$$

$$Z_{SOPT}(FET) \approx \frac{1}{\omega (C_{gs} + C_{gd})} \left[\sqrt{\frac{g_m (R_s + R_g)}{k_1}} + j \right] = \frac{f_{Teff}}{f g_{meff}} \left[\sqrt{\frac{g'_m (R'_s + W_f R'_g(W_f))}{k_1}} + j \right]$$

HBT f_T, f_{MAX}, NF_{MIN} vs. I_C characteristics

$$\frac{1}{2\pi f_T}=\tau=\frac{1}{\gamma}\underbrace{\left[\frac{W_B^2}{D_B}+\frac{W_B}{v_{exit}}\right]}_{\tau_F}+\frac{X_C}{2v_{SAT}}+\frac{kT}{qI_C}(C_{BE}+C_{BC})+(r_C+r_E)C_{BC}+r_C C_{CS}\approx\tau_F+\frac{C_{BE}+C_{BC}}{g_m}$$

$$f_{MAX}\approx\sqrt{\frac{f_T}{8\pi r_B C_{BC}}}$$

$$Z_{SOPT}(HBT)\approx\frac{1}{\omega(C_{be}+C_{bc})}\left[\sqrt{\frac{g_m}{2}(r_E+R_b)}+j\right]=\frac{f_{Teff}}{f\,g_{meff}}\left[\sqrt{\frac{g_m}{2}(r_E+R_b)}+j\right]$$

$$F_{MIN}(HBT)\approx 1+\frac{1}{\beta}+\frac{f}{f_{Teff}}\sqrt{2g_m(R_b+r_E)}$$

Intrinsic Slew Rate

$$SL_i = \frac{I_{pfT}}{C_{out}}$$

$$SL_i = \frac{I_{pfT}}{C_{bc} + C_{cs}}$$

$$SL_i = \frac{I_{pfT}}{C_{gd} + C_{db}}$$

Important for output drivers and digital circuits

Degraded by interconnect parasitics

Why do we need the HF FoMs?

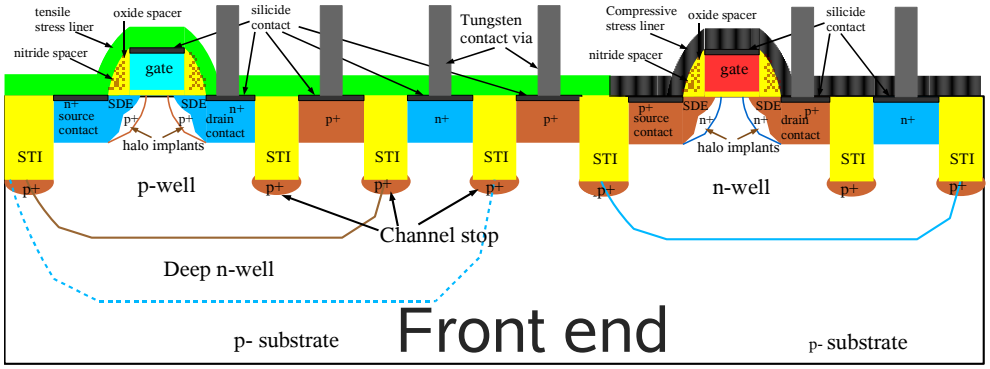
- Want to use the FOMs in circuit design
  - We have defined f_T, f_{MAX}, F_{MIN} and techniques to calculate them from the measured or simulated S parameters and noise measurements ($F_{MIN,}$ R_n, Γ_{opt} (G_{mIn} in Spectre)
  - We now want to find expressions that link f_T, f_{MAX}, F_{MIN} to device bias current and geometry

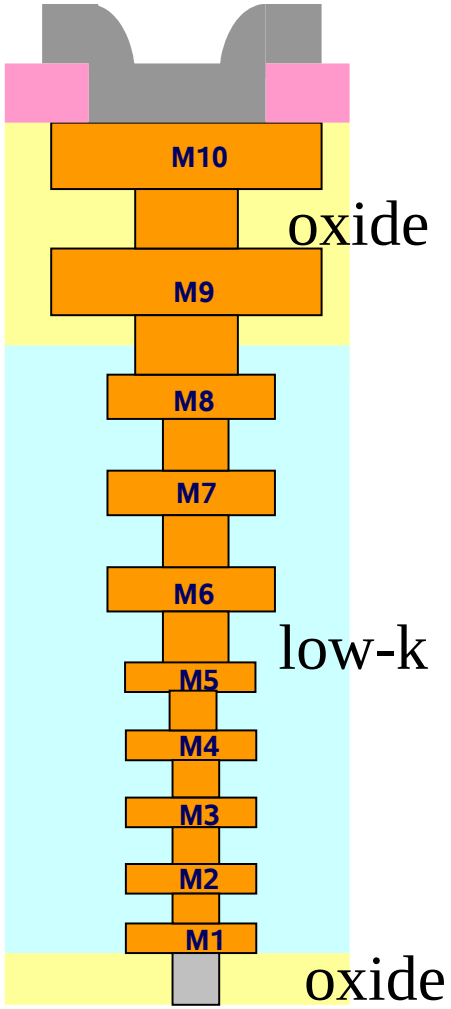
Outline

- Microwave and mm-wave transistors
- High-frequency figures of merit
- MOSFET structure & HF equivalent ckt.

Key nanoscale CMOS process features

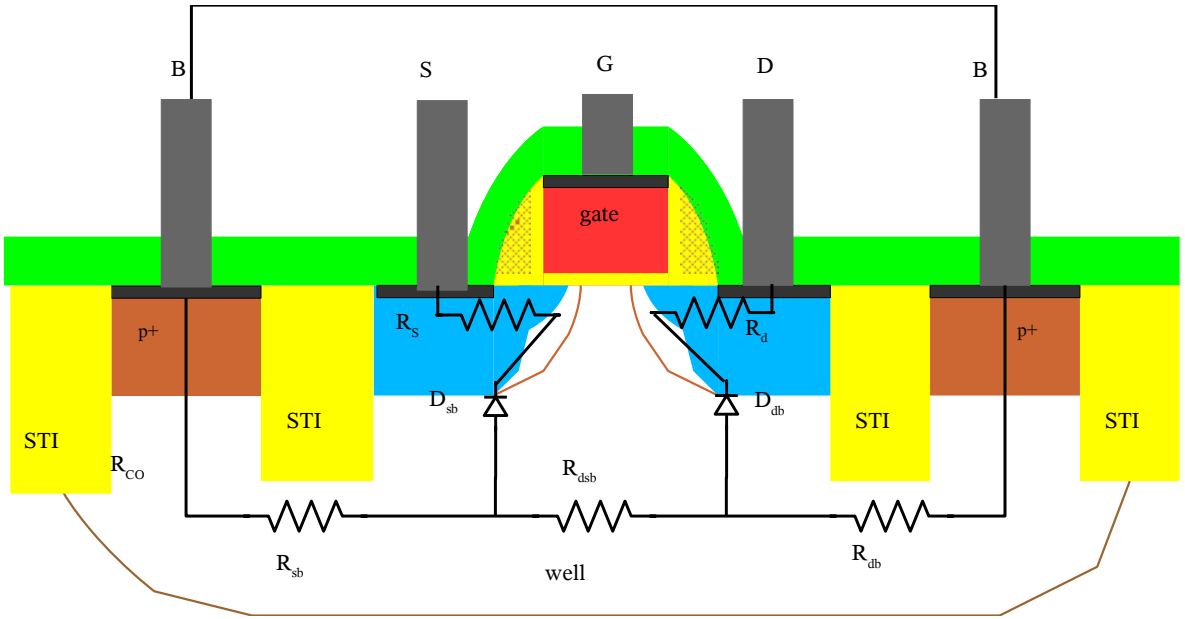
- STI to reduce active pitch
- Retrograde Twin wells (latch-up, device parasitics)
- Triple well (deep n-well) for isolating p-well
- Thick gate oxide devices for IO compatibility
- N+/P+ poly gate for symmetrical N/P-MOSFETs (HKMG in <=45nm)
- Self-aligned silicided D/S/G (low R_s, R_d, R_g)
- Tensile/compressive stress liners for mobility imprvmnt.
- Dual Damascene Cu interconnects



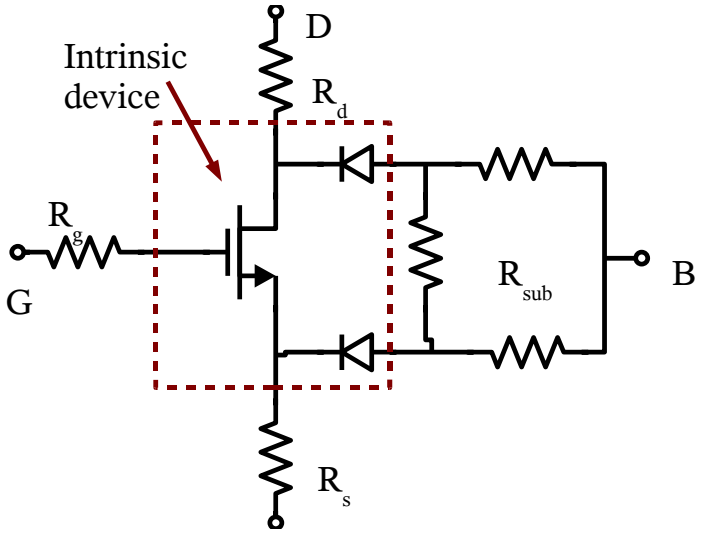


Back end

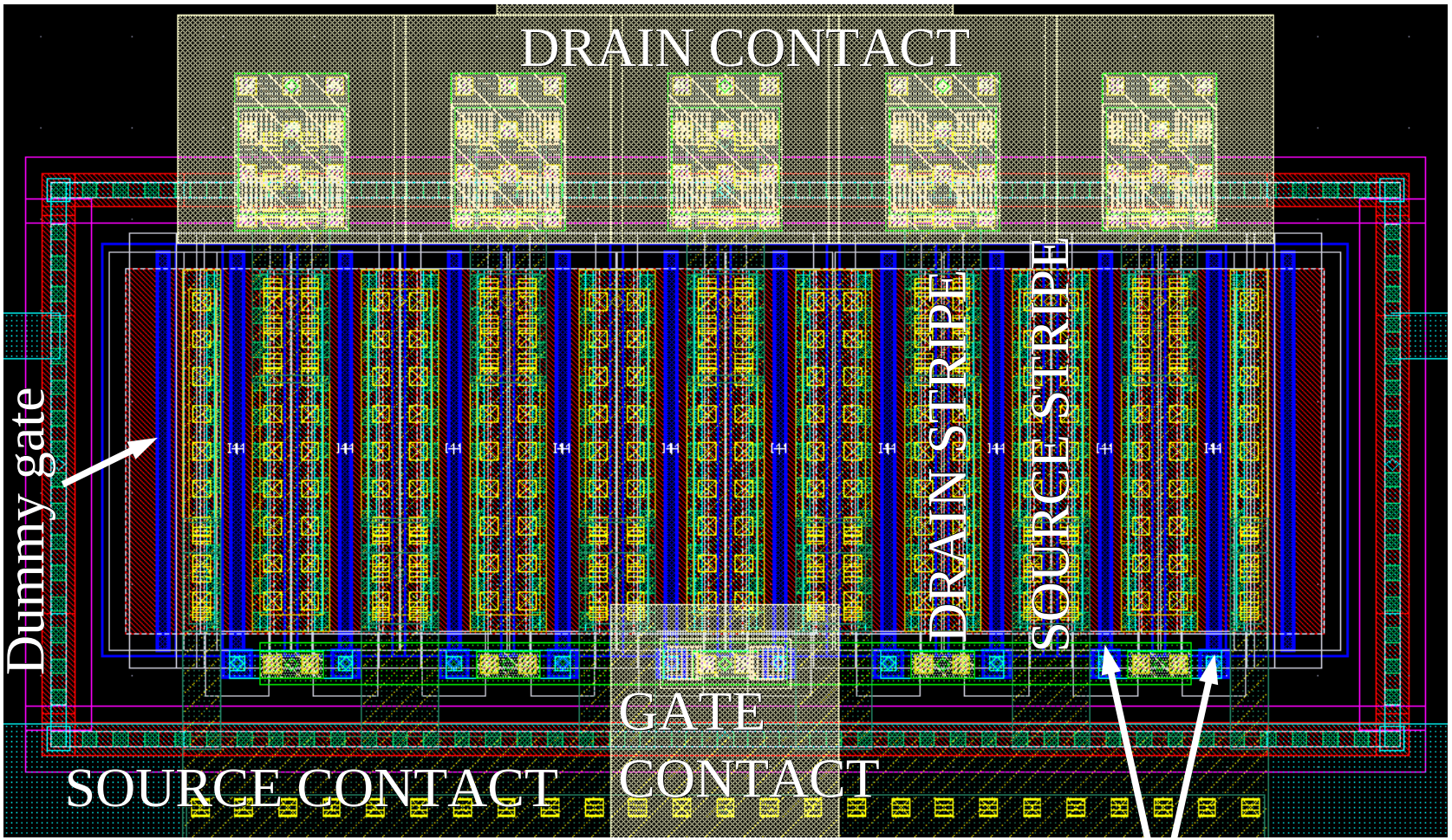
MOSFET structure and large signal circuit



- Intrinsic transistor
- Two pn junctions
- Parasitic resistances

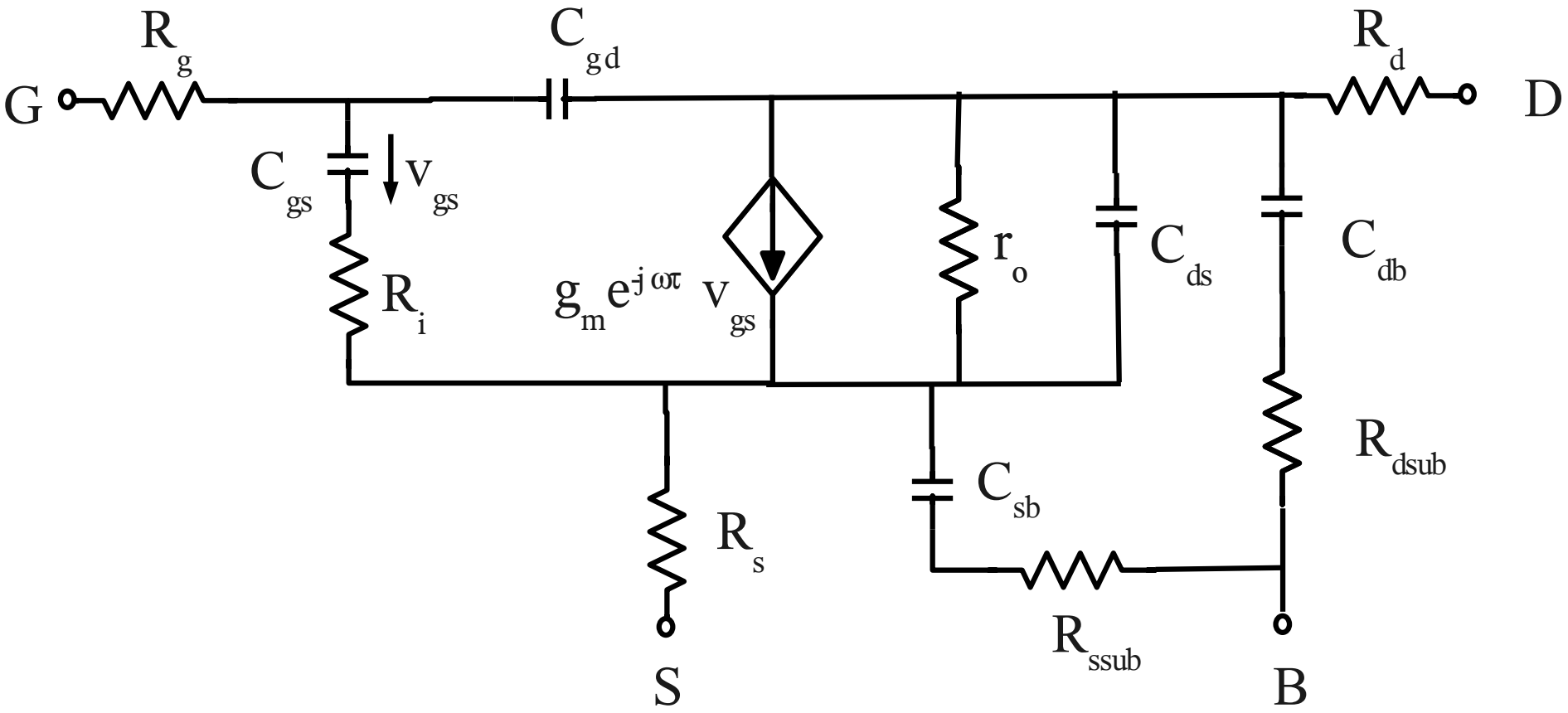


Typical MOSFET layout for high-frequency apps.



10 gate fingers

Complete CS mall signal equivalent circuit



Geometry dependence of equiv. ckt. params

$$g_m = g'_m W;\ \ g_{ds} = g'_{ds} W;\ \ C_{gs} = C'_{gs} W;\ \ C_{gd} = C'_{gd} W;\ \ C_{ds} = C'_{ds} W$$

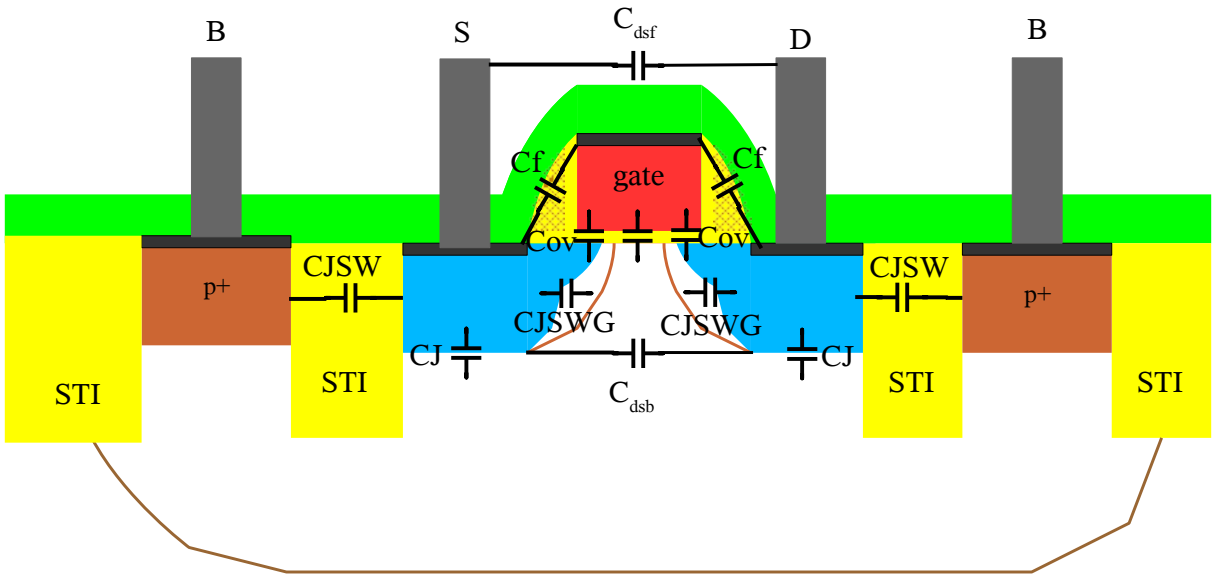
$$R_i = \frac{R'_i}{W};\ \ R_{gd} = \frac{R'_{gd}}{W};\ \ R_s = \frac{R'_s}{W};\ \ \ R_d = \frac{R'_d}{W};$$

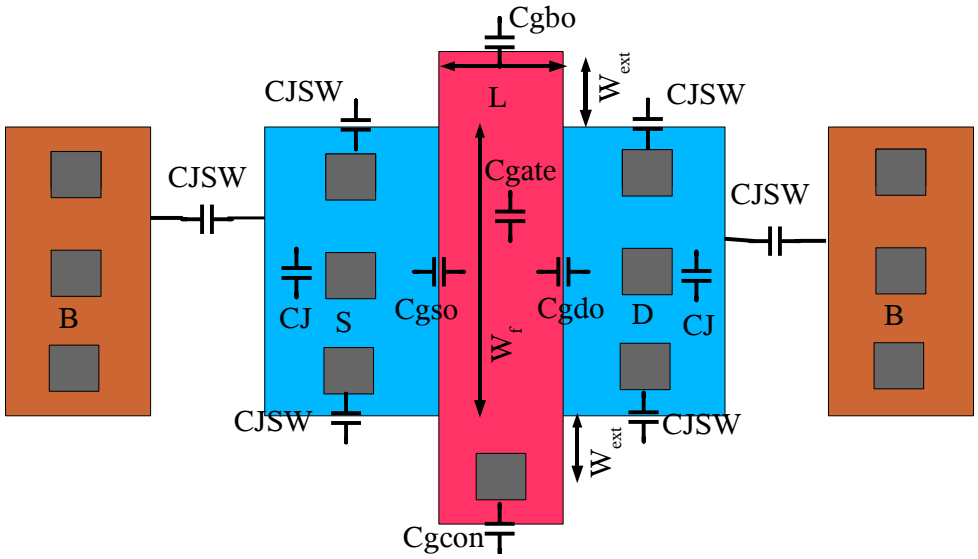
W_F is the unit gate finger width.

$W = N_f x W_f$ is the total gate finger width.

g'_m, g'_{ds}, C'_{gs}, C'_{gd}, C'_{ds}, R'_i, R'_{gd}, R'_d, R'_s are process-dependent params

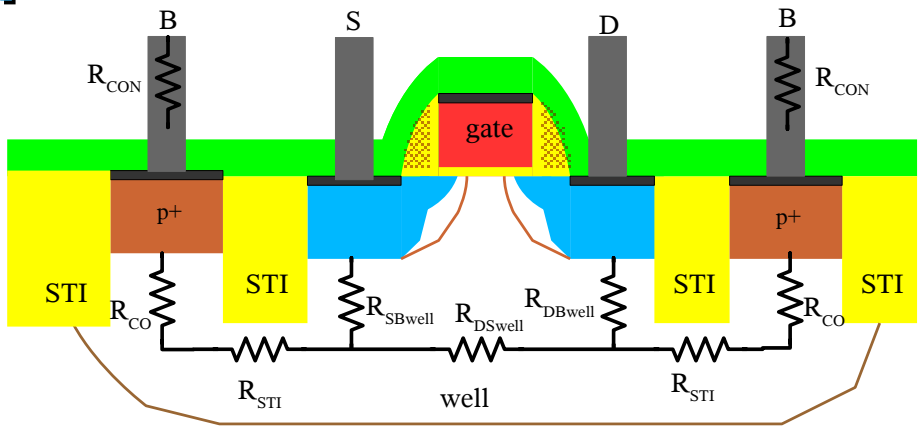
MOSFET Capacitances

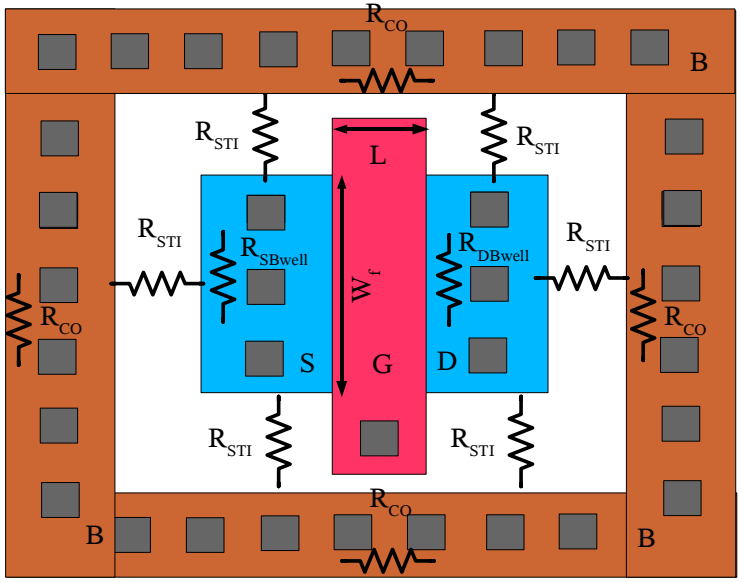




MOSFET substrate resistance network is layout dependent

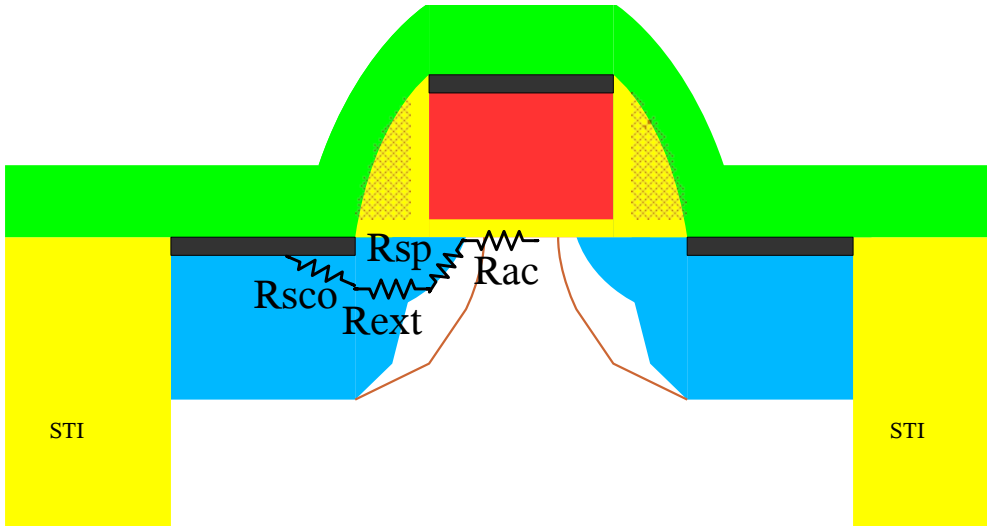
- Can be calculated based on layout geometry and doping/sheet resistance data





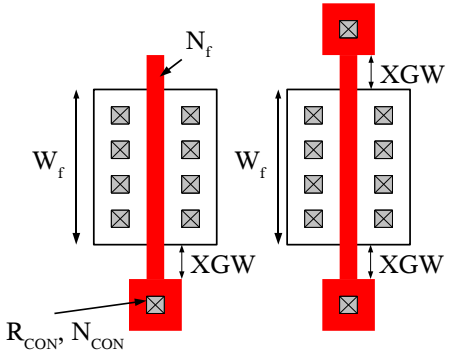
MOSFET source/drain resistance

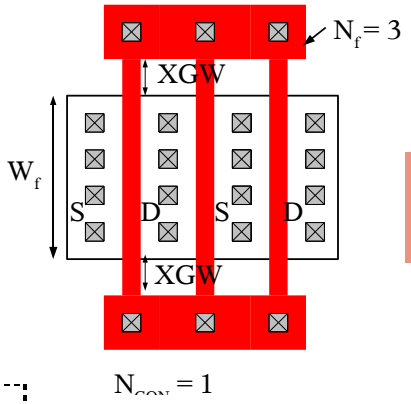
- Not layout dependent
- Depends on gate width W
- R_s/W remains practically constant at 200-300$\Omega \times \mu m$ across nanoscale nodes

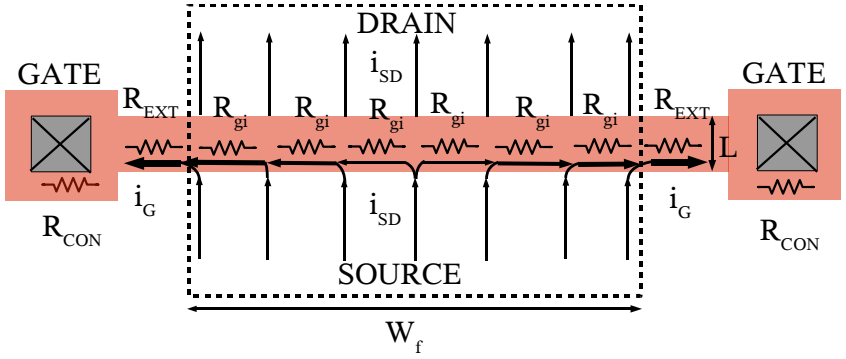


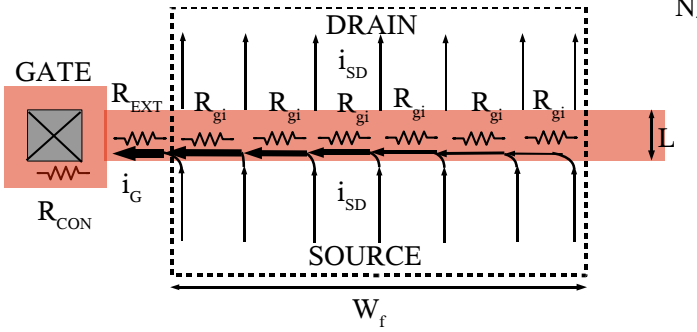
- Rac = accumulation region resistance
- Rsp = spreading resistance
- Rext = resistance of the SDE region
- Rsco = contact resistance

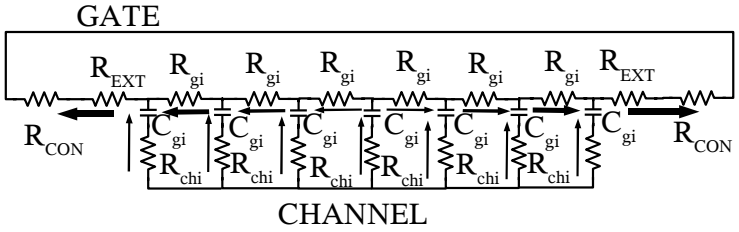
Gate Resistance: Layout dependent: W_f

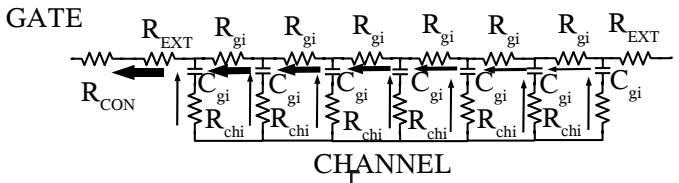












$$R_g = \frac{\left[\frac{R_{CON}}{N_{CON}} + \frac{RSHG}{L}\left(XGW + \frac{W_f}{3}\right)\right]}{N_f}$$

$$R_g = \frac{\left[\frac{R_{CON}}{N_{CON}} + \frac{RSHG}{L}\left(XGW + \frac{W_f}{6}\right)\right]}{2N_f}$$

Numerical Example

- 10μmx90nm device contacted on one side:
- RSHG = 10 Ohm, L=65nm, NCON=1, RCON=20 Ω, Wext =150 nm;
- a) W_f=1μm; N_f = 10,

$$R_g = \frac{\left[\frac{20}{1} + \frac{10}{0.065}\left(0.15 + \frac{1}{3}\right)\right]}{10} = \frac{20 + 74.3}{10} = 9.4\,\text{Ohm}$$

- b) W_f=2μm; N_f = 5,

$$R_g = \frac{\left[\frac{20}{1} + \frac{10}{0.065}\left(0.15 + \frac{2}{3}\right)\right]}{5} = \frac{20 + 126.15}{5} = 29.23\,\text{Ohm}$$

- R_s=R_d = (1/W)× 200 Ohm× μm = 20 Ohm in both cases.

Numerical Example (ii)

- 10μmx90nm device contacted on both sides:
- R_{SHG} = 10 Ohm, L=65nm, N_{CON}=1, R_{CON}=20Ω, W_{ext} =150 nm;
- a) W_f=1μm; N_f = 10,

$$R_g = \frac{\left[\frac{20}{1} + \frac{10}{0.065}\left(0.15 + \frac{1}{6}\right)\right]}{20} = \frac{20 + 48.71}{20} = 3.43\,\text{Ohm}$$

- b) W_f=2μm; N_f = 5,
-

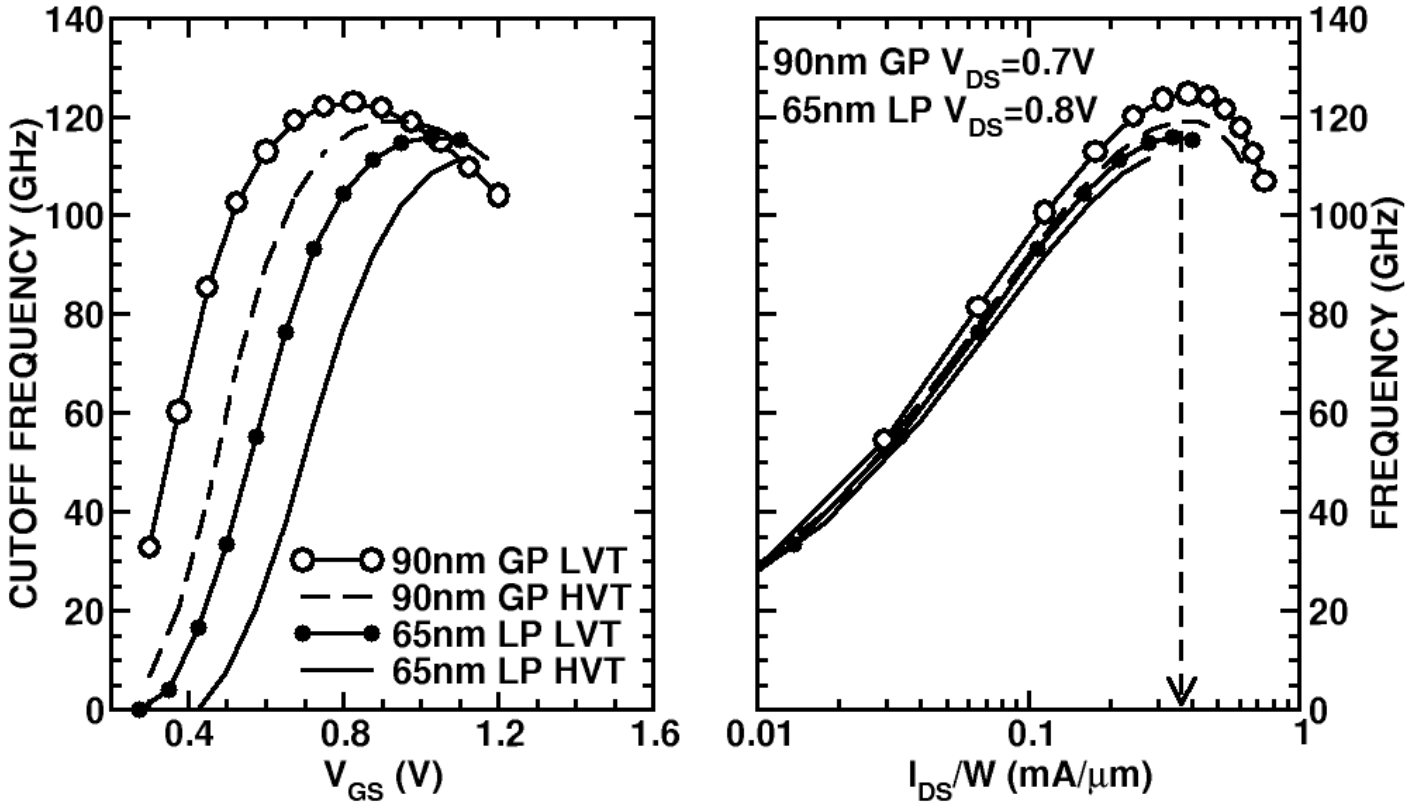
$$R_g = \frac{\left[\frac{20}{1} + \frac{10}{0.065}\left(0.15 + \frac{2}{6}\right)\right]}{10} = \frac{20 + 74.32}{10} = 9.4\,\text{Ohm}$$

- R_S=R_d =(1/W)× 200 Ohm× μm = 20 Ohm in both cases remain large while R_g can be minimized.
-

J_{pfT} invariant to V_T

130/90/65-nm MOSFETs f_T, f_{MAX} current density invariant over devices with

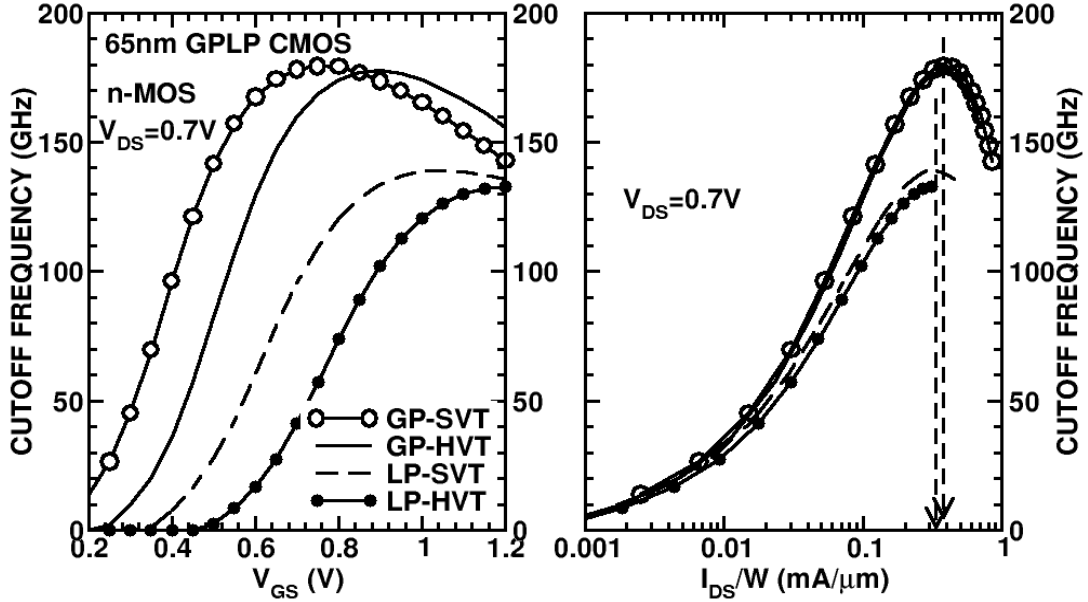
- low,
- standard,
- high V_T, and
- different nodes

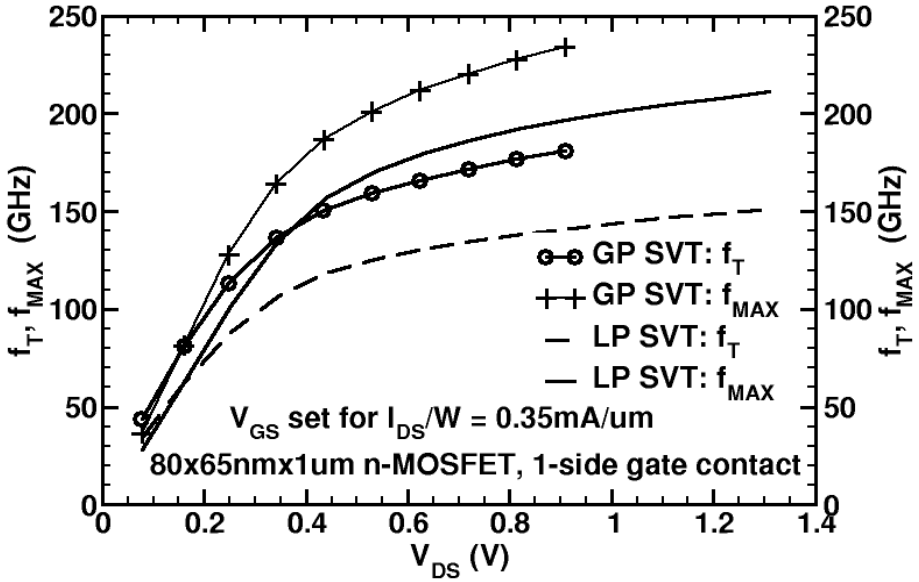


- Constant-current-density bias => designs more robust to V_T variation

GP vs. LP 65nm CMOS

- GP 30% faster than LP and 300mV lower V_{GS} => lower power!
- VT variation is large but mostly irrelevant
- Constant-current-density bias at 0.2-0.5mA/μm => robust to I_{DS}, V_T variation
- Need V_{DS}> 0.6 V



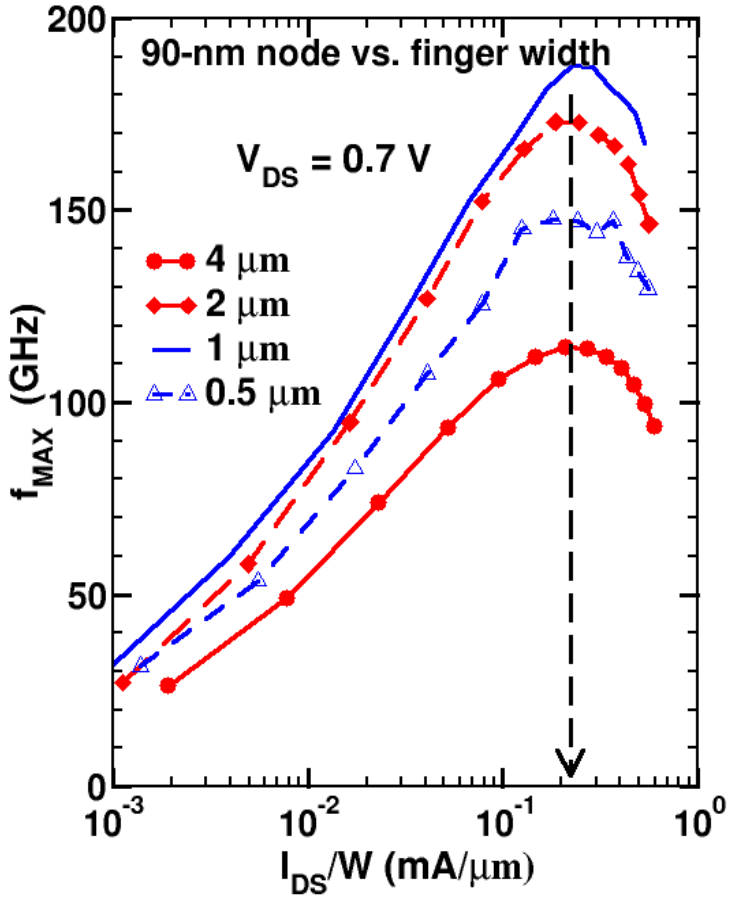


MOSFET f_{MAX} as a function of layout

$$f_{MAX} = \frac{f_T}{2\sqrt{(R_i + R_s + R_g)(g_{ds} + 2\pi f_T C_{gd})}}$$

$$f_{MAX} \approx \frac{f_T}{2\sqrt{\left(R_i' + R_s' + \frac{R_{SHG} W_f^2}{12(3) l_G}\right)(g_{ds}' + 2\pi f_T C_{gd}')}}$$

Impact of using minimum width devices on f_{MAX} and (likely) on NF_{MIN}



- In the 90-nm node f_{MAX} degrades by 25% as the unit finger width is reduced from 1 μm to 0.5 μm.
- Even though gate resistance improves, the degradation in f_T leads to f_{MAX} degradation.

MOSFET Impedance Noise Parameters

$$R_u = (R_s + R_g) + k_2 \frac{1 + (\omega R_i C_{gs})^2}{g_m} \qquad G_n = k_1 g_m \frac{f^2}{f_T^2}$$

$$Z_{cor} = (R_s + R_g) + k_3 R_i + \frac{k_3}{j\omega C_{gs}}$$

$$F_{min} \approx 1 + 2k_1 \frac{f}{f_T} \sqrt{g_m (R_s + R_g) + k_2 (1 + \omega^2 R_i^2 C_{gs}^2)}$$

$$k_1 = P + R - 2C\sqrt{PR}; k_2 = \frac{PR(1 - C^2)}{k_1}; k_3 = \frac{P - C\sqrt{PR}}{k_1}$$

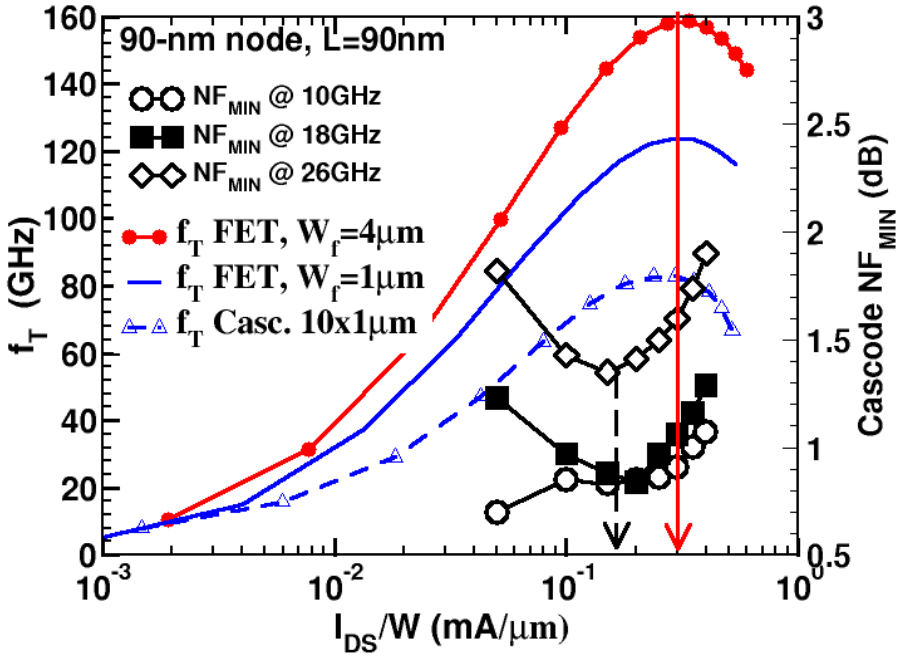
MOSFET noise parameters finger width and bias dependence

$$F_{MIN} \approx 1 + 2k_1 \frac{f}{f_T} \sqrt{g_m' R_s' + \frac{g_m' R_{SHG} W_f^2}{12(3) I_G}} + k_2 (1 + \omega^2 R_i^2 C_{gs}^2)$$

$$F_{MIN} \approx 1 + 2\,\mathrm{Const} \frac{f}{\sqrt{g_m'}} \approx 1 + 2\,\mathrm{Const} \frac{f}{\sqrt{V_{GS} - V_T}}$$

F_{MIN} is a (strong) function of W_f and I_G

F_{MIN} decreases as a function of V_{GS} until g_m (f_T) reaches its peak.



Scaling of MOSFET HF Performance

- C'_{gs}, C'_{gd}, C'_{db} and Z_{SOPT} approx. constant over nodes
- g'_m, g'_o, f_T, f_{MAX} increase
- F_{MIN}, R_n decrease
- RF & high-speed performance (except output swing) improves with scaling
- Leakage is not a problem at mm-waves and high-speed

Scaling is good for high-speed digital/wireline and mm-waves

Making Nano-CMOS Designs PVT Independent

- CMOS characteristic densities are largely invariant across nodes and foundries
- Constant-current-density biasing in analog/RF/mm-wave CMOS minimizes impact of L, I_{DS}, T, and V_T variation
- Characteristic current densities are invariant over topologies (CS, CG, cascode, CMOS inverter, TIA)
- In circuit design, one must fix W_f, L and scale only N_f

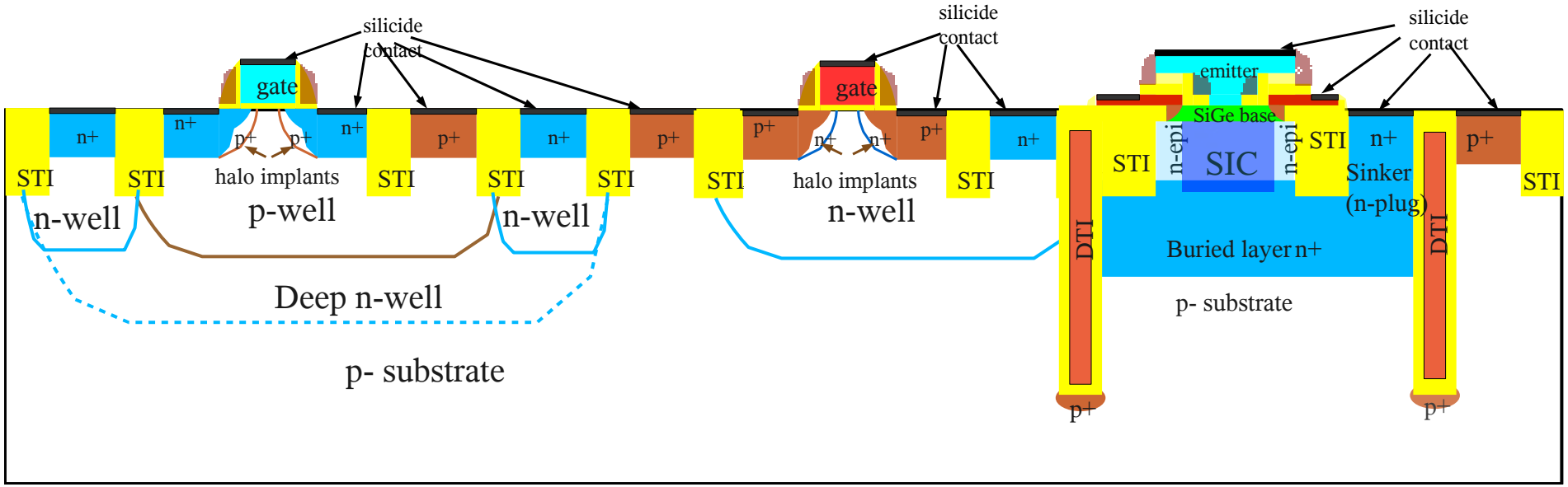
Implications for circuit design

- CMOS CML gates, LNAs, TIAs, VCOs, Mixers, PAs, Opamps and filters can be designed algorithmically and ported across nodes and foundries

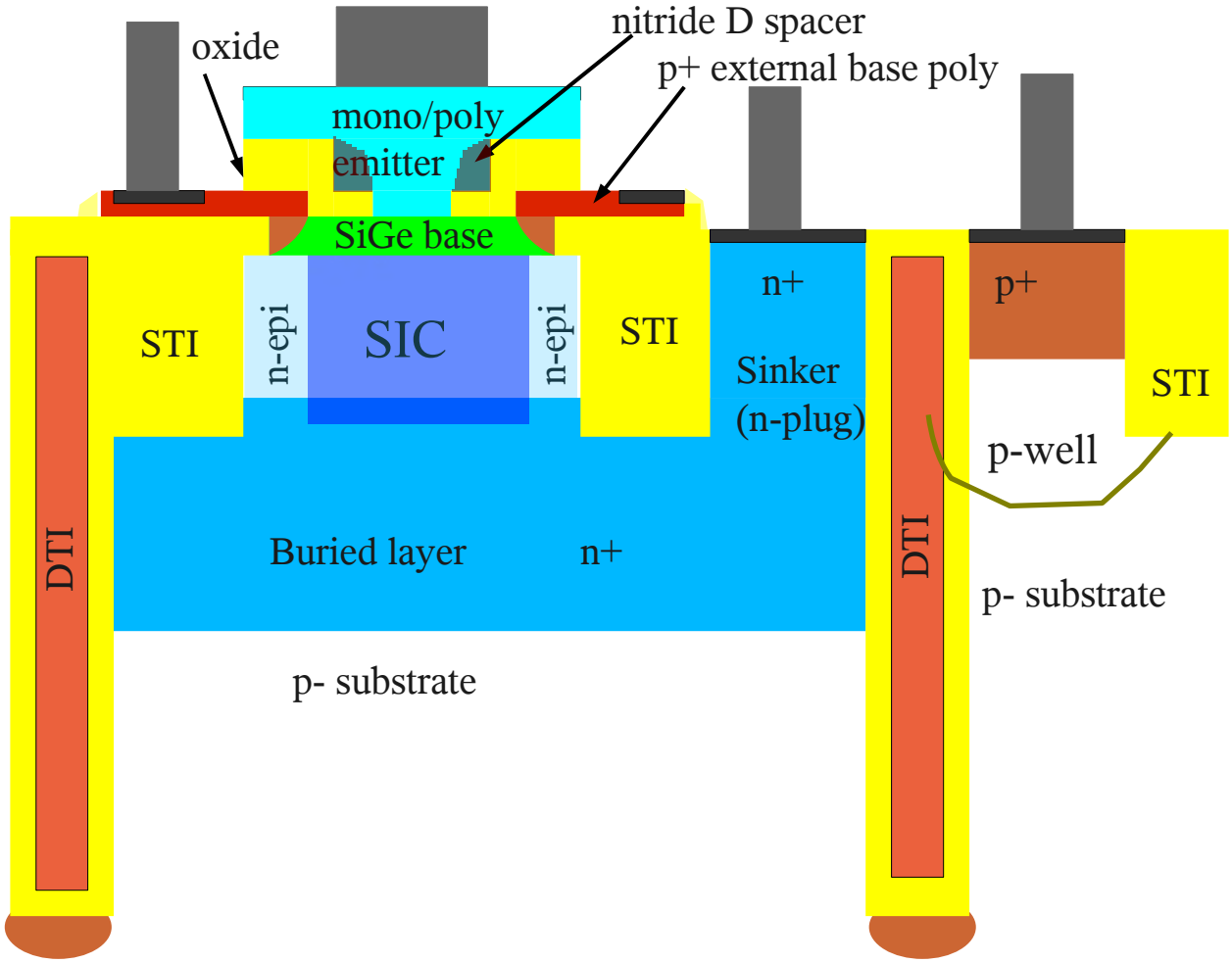
Outline

- Microwave and mm-wave transistors
- High-frequency parameter definition
- MOSFET structure & HF equivalent ckt.
- SiGe HBT structure & HF equivalent ckt.

SiGe BiCMOS Technology Cross-section

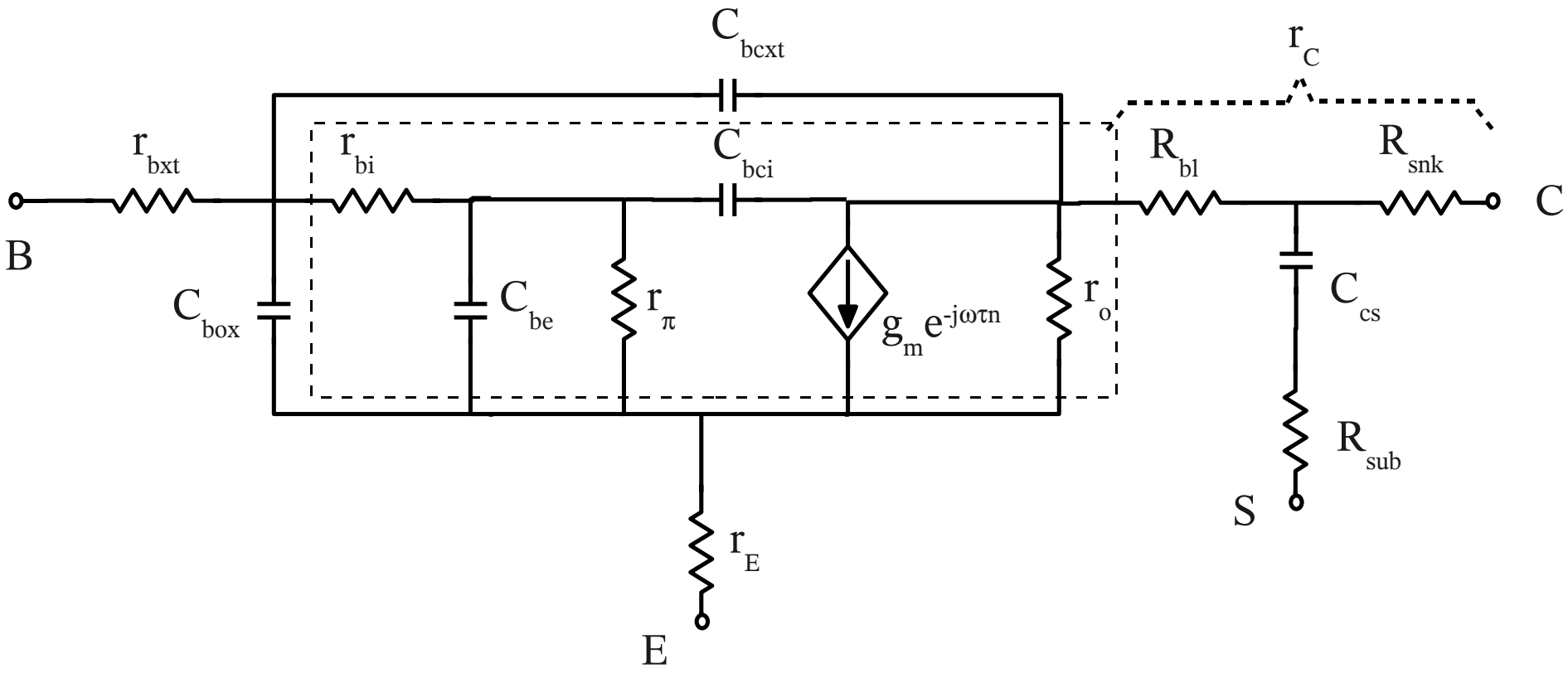


SiGe HBT Cross-section



- Deep trench isolation between devices. Reduces C_{cs}
- SIC collector
- Graded Ge base
- L/D-shaped spacer between emitter and external base contact
- Mono+poly emitter (low R_E)

SiGe HBT HF Equivalent Circuit



Geometry Dependence of Small Signal Params

$$I_C = J_C \cdot w_E \cdot l_E;\quad g_m = \frac{I_C}{V_T} = \frac{J_C}{V_T} \cdot w_E \cdot l_E;\quad g_o = \frac{I_C}{V_A} = \frac{J_C}{V_A} \cdot w_E \cdot l_E;\quad R_E = \frac{R_{Esq}}{l_E w_E};$$

$$R_{bx} = \frac{R_{SBX} \cdot w_{SP}}{2(w_E + l_E)};\quad R_{bi} = \frac{R_{sbio}}{12}\frac{w_E}{l_E} \quad \text{for double-base}$$

$$R_{bx} = \frac{R_{SBX} \cdot w_{SP}}{w_E + l_E};\quad R_{bi} = \frac{R_{sbio}}{3}\frac{w_E}{l_E} \quad \text{for single-base}$$

$$C_{be} = C_{be,diff} + C_{je} = \tau_F g_m + CJE \cdot w_E \cdot l_E;\quad C_{bep} = CJEP \cdot 2 \cdot (l_E + w_E)$$

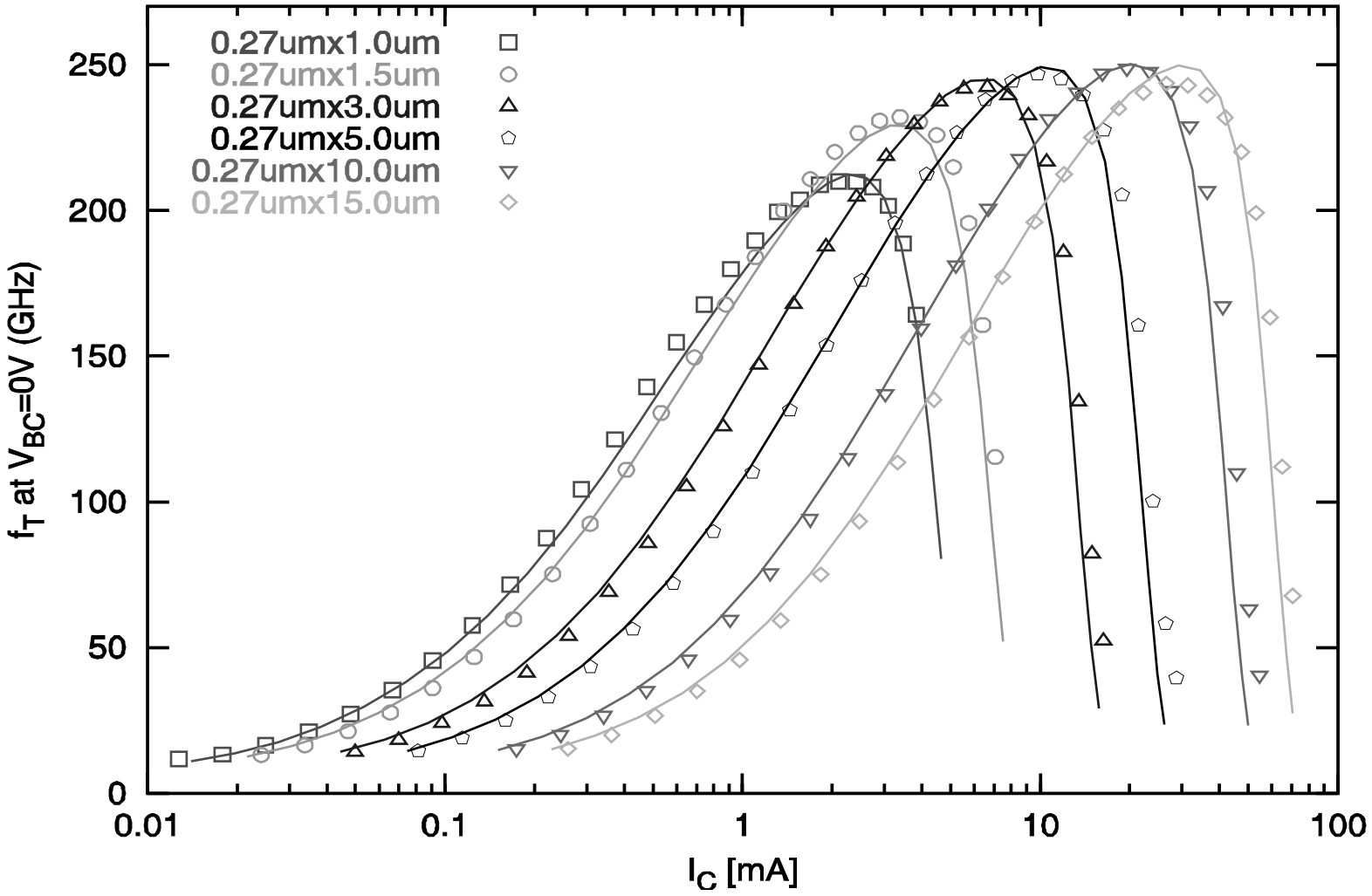
$$C_{bci} = C_{jCi} \cdot A_{BCi} = C_{jCi} \cdot l_E \cdot (w_E + 2b_{sic})$$

$$C_{bcx} = C_{jCX} \times A_{BCext} \approx C_{JCX} \times 2 \times w_{BCsp} \times (w_E + l_E + 2\,w_{BCsp})$$

f_T dependence on emitter length

- To first order, f_T is independent of emitter length because length dependence cancels out in $C \times R$
- As a second order effect, f_T depends slightly on I_E due to peripheral BE capacitance and R_c.

Typical HBT f_T-I_C plots for devices with different emitter lengths



SiGe HBT f_{MAX} layout dependence

$$f_{MAX} = \sqrt{\frac{f_T}{8\pi R_b C_{cb}}}$$

$$R_b \propto \frac{1}{I_E} \qquad C_{bc} \propto I_E$$

R_C, R_{sub}, C_{cs} affect (degrade) f_{MAX}

f_{MAX} is a (strong) function of w_E.

f_{MAX} is a weak function of I_E.

HBT noise parameters I_E dependence

$$R_n = \frac{n^2 V_T}{2 I_C} + (R_E + R_b) \text{ scales as } \frac{1}{I_E} \qquad n \approx 1 \text{ (ideality factor)}$$

$$Y_{sopt} \approx \frac{f}{f_T R_n}\left[\sqrt{\frac{I_C}{2V_T}(R_E+R_b)\left(1+\frac{f_T^2}{\beta f^2}\right)+\frac{n^2 f_T^2}{4\beta f^2}} - j\frac{n}{2}\right] \quad \text{scales as } I_E$$

$$F_{MIN} \approx 1 + \frac{n}{\beta} + \frac{f}{f_T}\sqrt{\frac{I_C}{2V_T}(R_E+R_b)\left(1+\frac{f_T^2}{\beta f^2}\right)+\frac{n^2 f_T^2}{4\beta f^2}}$$

F_{MIN} is weak function of I_E but a (strong) function of w_E

HBT noise parameters bias dependence

$$R_n = \frac{n^2 V_T}{2 I_C} + (R_E + R_b) \text{ scales as } \frac{1}{I_C}$$

$$Y_{sopt} \approx \frac{f}{f_T R_n}\left[\sqrt{\frac{I_C}{2V_T}(R_E+R_b)\left(1+\frac{f_T^2}{\beta f^2}\right)+\frac{n^2 f_T^2}{4\beta f^2}} - j\frac{n}{2}\right] \text{ increases with } I_C$$

$$F_{MIN} \approx 1 + \frac{n}{\beta} + \frac{f}{f_T}\sqrt{\frac{I_C}{2V_T}(R_E+R_b)\left(1+\frac{f_T^2}{\beta f^2}\right)+\frac{n^2 f_T^2}{4\beta f^2}}$$

F_{MIN} first decreases (due to drop in $R_b(I_C)$ – thermal noise is dominant) and then increases with I_C (shot noise dominates)

HBT Summary

- HBT characteristic densities increase in newer nodes
- In a given technology, J_{OPT} increases with frequency
- J_{OPT} increases if a series resistance is added to emitter or base
- Large f_{MAX} can be obtained at lower J_C and with higher BV_{CEO} than f_T.

Implications for circuit design

- Designs must be modified in each node/foundry, although, for a given peak f_T, J_C appears to be similar between foundries.

Outline

- Microwave and mm-wave transistors
- High-frequency figures of merit
- MOSFET structure & HF equivalent ckt.
- SiGe HBT structure & HF equivalent ckt.
- FETs vs. Bipolars

Noise Parameters: HBT VS. MOSFET (i)

HBT

$$R_n \approx \frac{1}{2g_m} + (r_E + R_b)$$

$$Y_{sopt} \approx \frac{f}{f_T R_n}\left[\sqrt{\frac{g_m}{2}(r_E + R_b)} - j\frac{n}{2}\right]$$

$$F_{MIN} \approx 1 + \frac{1}{\beta} + \frac{f}{f_T}\sqrt{\frac{g_m}{2}(r_E + R_b)}$$

MOSFET

$$R_n \approx \frac{P}{g_m} + (R_s + R_g)$$

$$Y_{sopt} \approx \frac{f}{f_T R_n}\left[\sqrt{P g_m (R_s + R_g)} - jP\right]$$

$$F_{MIN} \approx 1 + \frac{f}{f_T}\sqrt{P g_m (R_s + R_g)}$$

Noise Parameters: HBT VS. MOSFET (ii)

- At equal bias current and comparable f_T, the MOSFET has lower g_m and hence:
  - lower F_{MIN}
  - lower R_n (higher sensitivity to Z_{sopt} mismatch)
  - higher R_{sopt} (larger current for 50-Ω noise matching)
- In MOSFETs, the peak f_{MAX} and the optimum noise bias current density coincide. In HBTs the optimum noise current density increases with frequency but is significantly smaller than peak f_T current density.

Low-noise transistor design

Two steps:

- Bias transistor at optimal noise current density
- Size transistor (while keeping the optimal noise current density) to make the real part of the optimum noise impedance (R_{sopt}) equal to the desired value.

Sizing is achieved by increasing W_f (l_E) or connecting gate fingers (emitter stripes) in parallel.

CMOS Technology over Nodes

Param/node	*250nm*	*180nm*	*130nm:GP/LP*	*90nm:GP/LP*	*65nmGP/LP*	*45nm*
L (nm)	250	180	120/120	65/80	45/57	39/35
EOT (nm)	5	3.5	2.1/2.3	1.6/2.1	1.3/1.8	1.1/1.3
V_{DD} (V)	2.5	1.8	1.2/1.2	1.0/1.2	1.0/1.2	0.9/1
g'_m (mS/µm)	0.35	0.55	0.8/0.7	1.2/1	1.6/1.2	1.8?
g'_o (mS/µm)	0.03	0.05	0.08	0.13	0.18	0.17?
C'_{gs} (fF/µm)	1.4	1.4	1	1	0.7	0.6
C'_{gd} (fF/µm)	0.45	0.45	0.45	0.35	0.35	0.34?
C'_{db} (fF/µm)	1.5	1.5	1.5	1.1	0.8	0.6?
R'_s/R'_d (Ω*µm)	100	120	150	200	200	200
n-MOS f_T (GHz)	40	60	80/80	140/120	190/160	250?

Parasitic source and gate resistance scaling

Parameter	***65nm GP***	***65nm LP (GP)***	***45nm***
Physical L (nm)	45	57 (45)	35
EOT (nm)	1.3	1.8 (1.3)	1.3 (1 for HKMG)
W_f (μm)	1	1	0.7
N_{CON}	1	1	1
Contact on both sides	No	No	No
R_{CON} (Ω)	40	40	60
R_{SHG} (Ω/sq)	15	15	20
W_{ext} (nm)	120	120	100
N_f	1	1	1
R_G (Ω)	191	159 (190)	250.5